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Multilayered Sb-rich GeSbTe Phase-Change Memory for Best Endurance and Reduced Variability

G. Lama, M. Bernard, G. Bourgeois, J. Garrione, V. Meli, N. Castellani, C. Sabbione, L. Prazakova, D.-S. Fernandez Rodas, E. Nolot, M.C. Cyrille, F. Andrieu and G. Navarro*

***Abstract*— Sb-rich GeSbTe based Phase-Change Memories (PCM) were studied in the last years for their high switching speed to target Storage Class Memory (SCM) applications. In this work, we show the advantages of an engineered Multilayered Sb-rich GeSbTe stack compared to standard bulk reference materials. The studied Multilayer-based PCM devices feature a lower programming current with respect to the equivalent bulk ones, preserving a high programming speed. Furthermore, Multilayered Sb-rich GeSbTe brings better endurance performances for a wide programming current range and extremely reduced cycle-to-cycle (C2C) and device-to-device (D2D) variability along cycling verified in 4 kb PCM arrays. These results confirm the improved yield and reliability obtained thanks to Multilayered PCM solution.**

***Index Terms*— Phase-Change Memory (PCM), Multilayer deposition, Sb-rich GeSbTe, endurance, speed, Storage Class Memory (SCM)**

I. Introduction

Non-Volatile Memories (NVMs) play an important role in nowadays life since they enable the permanent storage of the growing amount of data generated per day [1]. Among the different innovative NVM technologies under development, Phase-Change Memory (PCM) already demonstrated its high maturity in both standalone [2] and embedded market [3]. PCM working principle is based on a reversible transition between a highly resistive amorphous phase (RESET state) and a crystalline phase (SET state) featuring a low resistance, made possible by the switching phenomenon discovered in in the 1960s [4]. The most common phase-change material family is the one based on GeSbTe (GST) alloys, however the research of the best phase-change material is still active [5], [6]. Indeed, the tuning of the stoichiometry or the addition of dopants such as C, N or Si, showed the possibility to enable the adoption of PCM in different applications [7]. Among the several developed alloys, Sb-rich GST is recognized for its high programming speed [8] (i.e. SET time in the ns range) and for its high endurance of 2×10^{12} [9]. In particular, these features make Sb-rich PCMs suitable for Storage Class Memory (SCM) to bridge the large gap in performances and cost between DRAM main memory and solid mass storage [10]. In recent years, another technique was explored to customize the performances of PCM that consists in the alternation of layers of different alloys (i.e. Multilayered structure), such as GeTe and Sb_2Te_3 in a superlattice configuration [11] or $Ge_2Sb_2Te_5$ and Sb [12]. The main achievement obtained with this solution is the low power consumption, likely attributed to the enhanced thermal properties of the stack [13] [14]. However, a comparison between Sb-rich GST Multilayer and equivalent bulk materials and the statistical analysis of the performances and electrical parameters of PCM devices based on Multilayers are still missing.

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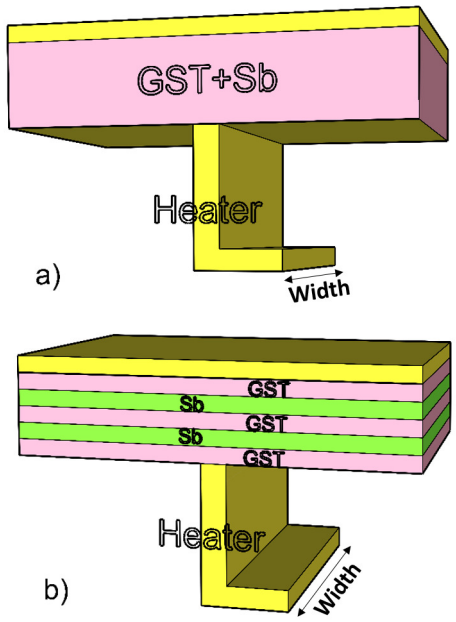

Fig. 1: Simplified representation of our "Wall" PCM device, based on a heater element that represents the bottom electrode, in bulk (a) and in Multilayer configuration (b).

In this work, different Sb-rich GST Multilayers deposited by alternative sputtering of GST and Sb targets are compared to bulk equivalent materials obtained by standard co-sputtering. First, material samples are investigated by four probe method to evaluate the resistivity in temperature and by Raman spectroscopy for structural analysis. Therefore, thanks to electrical characterization, we study the performances of the different stacks once integrated in 4 kb arrays based on PCM devices featuring a "Wall" structure [15] (**Fig. 1**). In particular, we

analyzed and compared at statistical level the programming current density, the programming speed and the data retention at high temperature in the different materials. Finally, we focus on the endurance performance of the best Multilayer stack developed, reporting about the highly reduced device-to-device (D2D) and cycle-to-cycle (C2C) variability with respect to bulk equivalent PCM devices. The results are supported as well by Transmission Electron Microscopy analyses (TEM) and Energy-Dispersive X-ray spectroscopy (EDX).

II. Materials Development and Analyses

Sb-rich GST Multilayer stacks were deposited alternating GST and Sb layers, tuning the layer thicknesses down to about 3 nm, and targeting two different stacks respectively with low and high total Sb content (i.e. low and high Sb thickness), both with a total amount of Sb in the range between 40 at.% and 70 at.%. In the following we will refer to the two different developed Multilayer stacks as ML1 (for the one with low Sb content) and ML2 (for the one with high Sb content). The corresponding standard bulk layers with equivalent global stoichiometry of the two Multilayers will be addressed as GST+Sb1 and GST+Sb2 respectively. N-doping was as well introduced in ML1 stack in order to observe the possible improvements thanks to N introduction compatibly with what previously reported [16]. This last stack will be addressed as ML1+N.

A. Resistivity-vs-Temperature

Sb-rich GST exhibits a growth-dominated crystallization mechanism, in which the crystallization is due to a fast crystal growth at the amorphous/crystalline interfaces [17]. **Fig. 2a-b** reports the resistivity as a function of temperature (RvsT) measured by four probes method in as-deposited materials. At the beginning, the materials are in the high resistive amorphous phase and at 200°C the resistivity remarkably decreases due to the transition to the crystalline phase. The crystallization temperatures of the Multilayers (ML1, ML2 and ML1+N) are slightly lower than the corresponding bulk ones (GST+Sb1 and GST+Sb2) (**Fig. 2c-d**), likely due to the heterogeneity induced by the several interfaces intrinsic of the multilayered structure. This is confirmed by the fact that amorphous Multilayers present a lower amorphous resistivity with respect to the equivalent bulk layers, due to the presence in their stack of highly conductive Sb layers reducing their total resistivity. Increasing the temperature, we observe an increase in resistivity before the crystallization step, likely related to the intermixing of GST and Sb layers that gives rise to an homogeneous phase. The resistivity curve evidences in each material a one-step transition from amorphous to hexagonal phase, typical of Sb-rich GST [8], [18], contrarily to other nucleation-dominated alloys such as $Ge_2Sb_2Te_5$, in which crystallization occurs more gradually and with intermediate phases from amorphous to cubic and

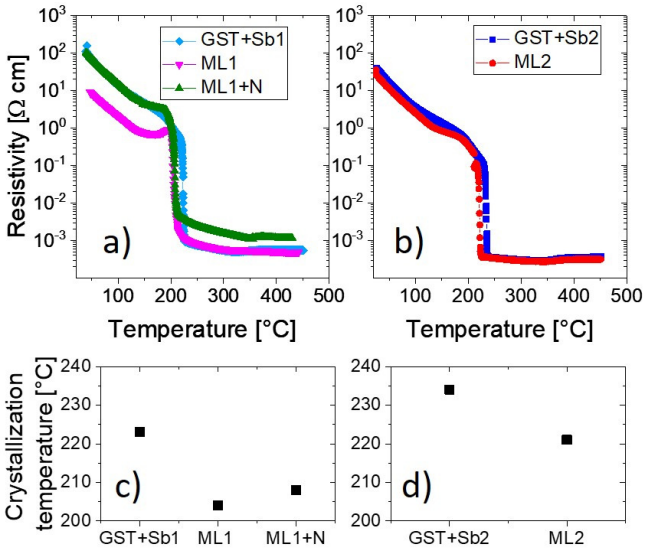

Fig. 2: Resistivity of as-deposited materials analyzed as a function of the temperature, measured during a ramp up of 10°C/min (a-b) and their crystallization temperature (c-d).

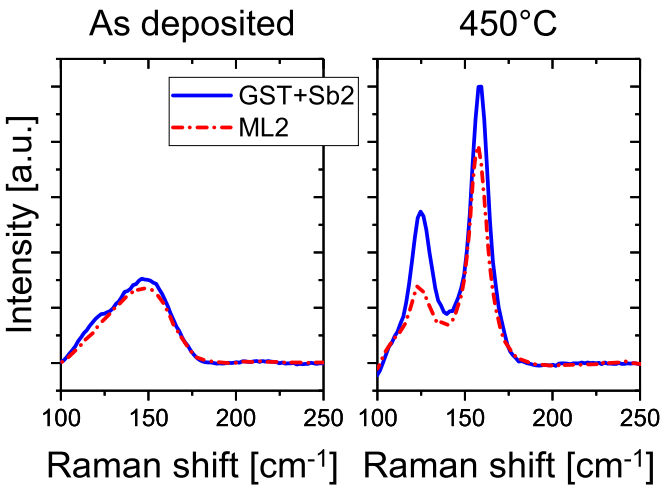

Fig. 3: Raman spectra obtained for GST+Sb2 and ML2 as-deposited (amorphous) and after annealing at 450°C (crystalline).

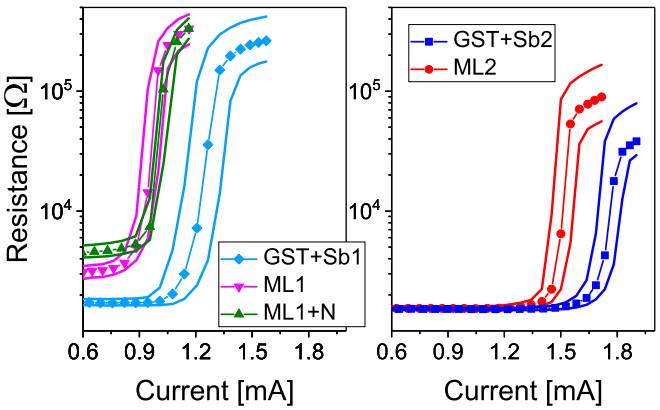

Fig. 4: Resistance as a function of current in 4 kb arrays of PCM devices with a heater width of 100 nm. Median and corresponding 1σ standard deviation for the 4 kb devices are represented.

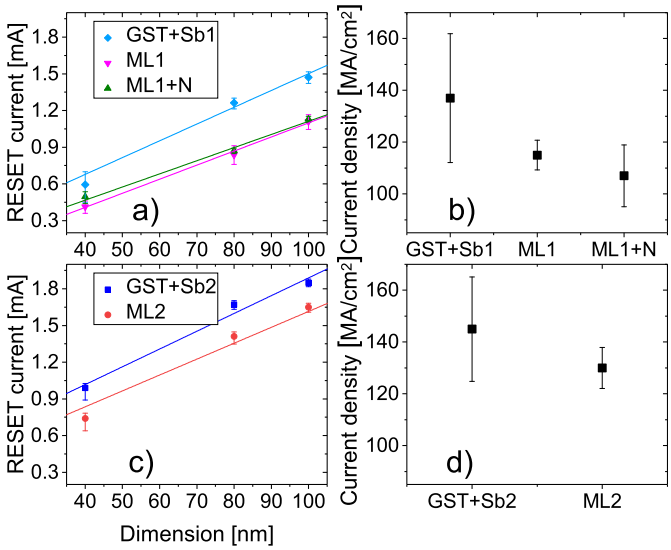

Fig. 5: RESET current measured in 4 kb arrays for different heater dimensions (width indicated in Fig.1). Median values and standard deviation are represented (a,c). RESET current density was extracted from the interpolation of the data in a and c for each composition (b,d).

finally to hexagonal phase [19]. Indeed, cubic phase requires a large amount of vacancies, that in Sb-rich samples are filled by Sb, inhibiting the formation of the cubic phase and leading to a crystallization possible only towards an hexagonal phase [20].

B. Raman spectroscopy

The high similarity between bulk and multilayered stacks is evidenced also by Raman spectra of amorphous and crystallized samples reported in **Fig. 3** for GST+Sb2 and ML2. The sharp peaks of both samples annealed at 450°C indicate a high crystalline degree in both samples. The peak positions have analogies with the ones found for other GST phases (e.g. $Ge_2Sb_2Te_5$ [21]). The peak at 125 cm^{-1} can be associated to $GeTe_{4-n}Ge_n$(n=1,2) tetrahedral groups, the most intense peak at 158 cm^{-1} can be attributed to the vibration modes of SbTe based groups and to Sb-Sb bonds [21]. The low intensity of the first peak compared to the second is linked to the low presence of Ge atoms in the Sb-rich GST crystallized phase. Slight differences in stoichiometry and Ge incorporation in the obtained crystalline phases after annealing, could be taken into account to explain the difference in the ratio between the two peaks intensities (i.e. different ratio between the two types of bonds).

From RvsT and Raman analyses we can observe the strong similarity of the crystallization dynamics between bulk and multilayered equivalent systems.

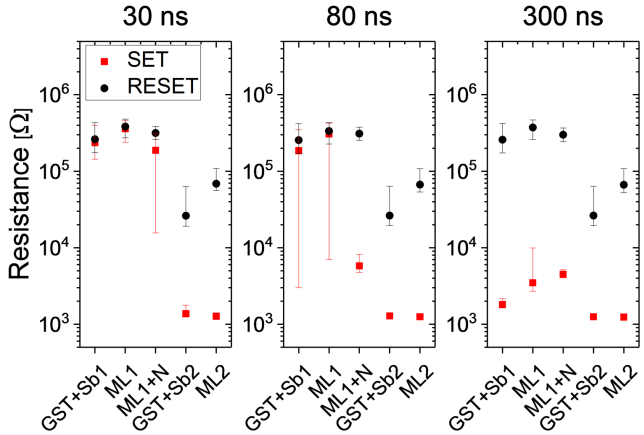

Fig. 6: Resistance achieved with a SET pulse of 30, 80 and 300 ns (respectively from left to right) for each stack analyzed. The starting RESET state resistance is reported as well for each test.

III. Electrical Characterization

The developed bulk and Multilayers have been integrated in "Wall" PCM devices (Fig. 1) with a heater thickness of 10 nm and a width going from 40 nm up to 100 nm, into the Back End of Line (BEOL) of LETI Memory Advanced Demonstrator (MAD) based on 130 nm CMOS technology. Electrical measurements were performed on 4 kb arrays for statistical analysis.

A. Programming characteristics

RESET current was measured pre-programming the devices in the SET state and applying a sequence of pulses with incremental voltage (i.e. AC based protocol). **Fig. 4** reports the resistance as a function of the current measured during the pulses application in 4 kb arrays. We observe a general reduction of the RESET current in Multilayer devices compared to the corresponding bulk devices. Considering the devices with low Sb content we observe a low RESET (at high current) resistance variability for both ML1 and ML1+N. The SET variability is extremely low for both high Sb content stacks (GST+Sb2 and ML2), however ML2 presents the highest RESET resistance value and then the highest resistance window with respect to the equivalent bulk GST+Sb2. RESET current was measured for three different heater sizes in 4 kb arrays (**Fig. 5a,c**) in order to extract the RESET current density (J_R) for each composition (**Fig. 5b,d**). Multilayer devices present a lower J_R compared to the corresponding bulk ones, statistically confirming a lower power consumption of Multilayer Sb-rich GST PCMs.

B. Programming speed analysis

The SET speed was evaluated pre-programming the 4 kb arrays in the RESET state and applying SET pulses with variable duration from 30 ns up to 300 ns (**Fig. 6**). All the compositions can be programmed in the SET state with a pulse of 300 ns. The highest speed is observed in compositions with the highest Sb content, GST+Sb2 and ML2, that are capable to crystallize in 30 ns. This is line with the growth-dominated crystallization mechanism in Sb-rich alloys that feature a high growth rate with a one-step phase-change transition

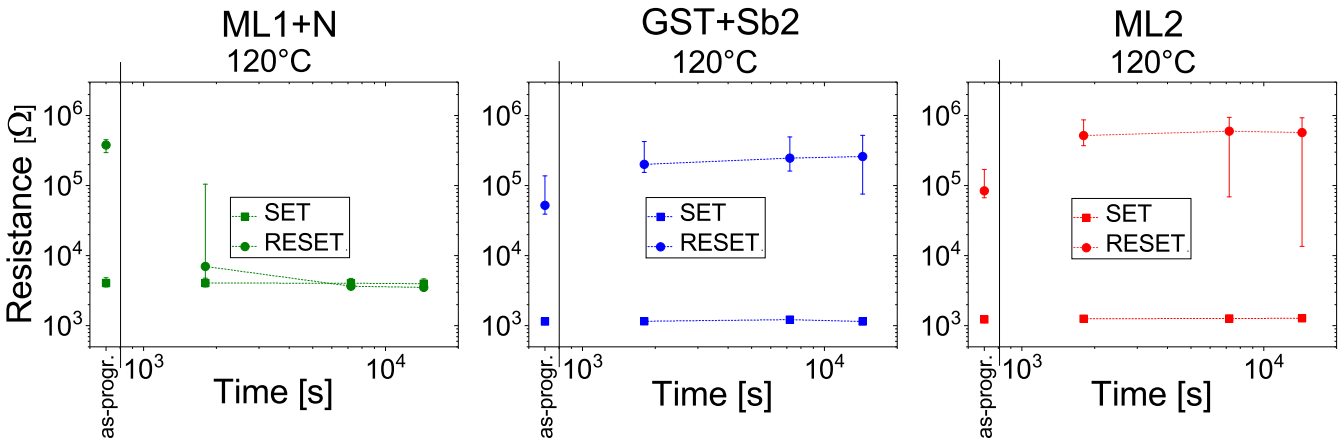

Fig. 7: Data retention evaluated at 120°C for the SET and the RESET states for ML1+N, GST+Sb2 and ML2 in 4 kb arrays. We report the starting SET and RESET distributions (as.-progr.) and after different annealing times up to 4 hours.

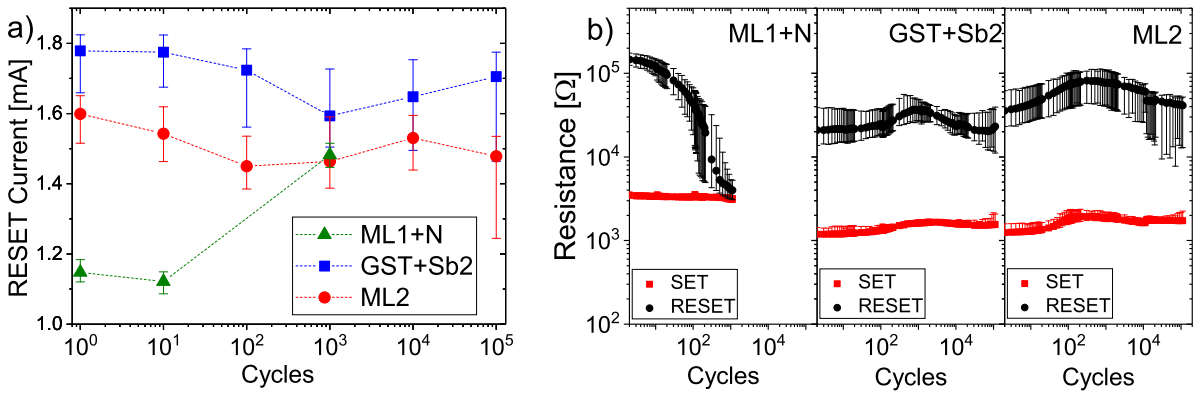

Fig. 8: a) RESET current evolution along endurance. Pulses of 10 µs width time were used to accelerate the degradation phenomena during cycling. b) SET and RESET resistance as a function of cycles number. For both graphs, median values and the standard deviation for populations of 100 devices are represented.

from amorphous to hexagonal phase as observed in RvsT measurements (Fig. 2). ML1+N is the only composition with low Sb content capable of SET programming in 80 ns. Indeed, Ge tends to bond with N [22] and GeN features could enhance the Sb enrichment in the active region, leading to a material with a higher crystallization rate. In the following the analyses will focus on such PCMs featuring high programming speed, nominally ML1+N, GST+Sb2 and ML2.

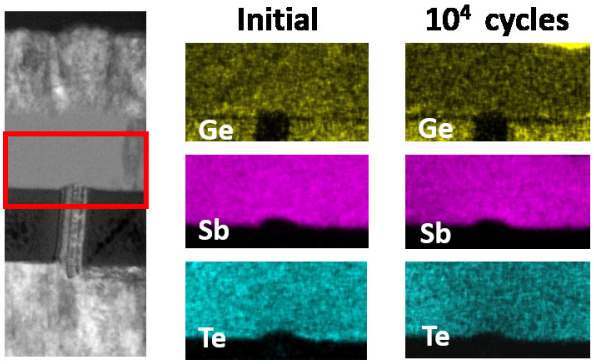

Fig. 9: TEM/EDX analyses performed on the active region of a ML2 PCM device before and after 10^4 cycles.

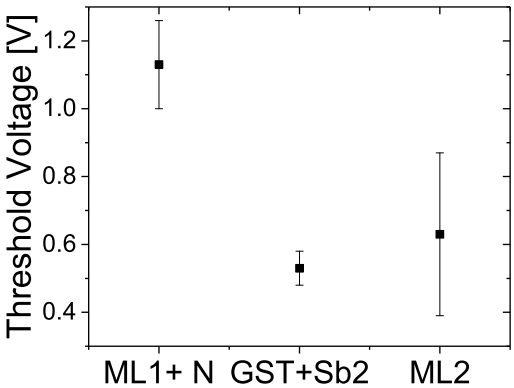

Fig. 10: Threshold voltage measured in 4 kb arrays for ML1+N, GST+Sb2 and ML2.

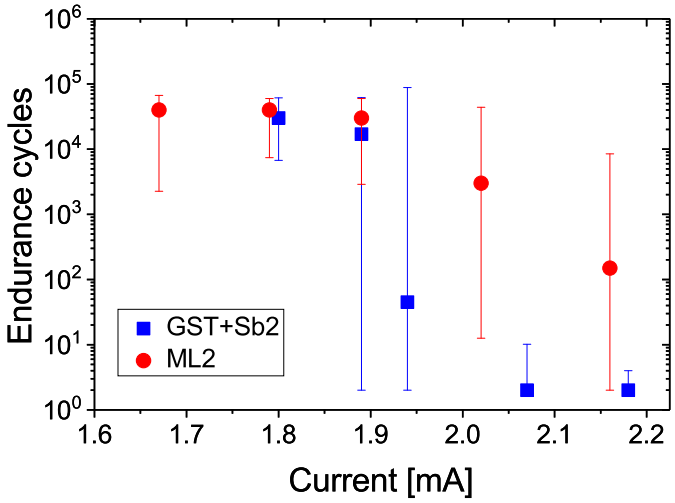

Fig. 11: Number of endurance cycles achieved applying RESET pulses with different current in GST+Sb2 and ML2 4 kb arrays. The endurance test has been executed with pulses with a duration of 200 µs to increase the stress during programming and to speed up the test sequence. We report the median values and one standard deviation.

C. Data retention

The data retention at 120°C of SET and RESET states was investigated in ML1+N, GST+Sb2 and ML2 (**Fig. 7**). Amorphous ML1+N crystallizes already after 30 min at 120°C. On the contrary, in GST+Sb2 and ML2 the RESET resistance exhibits only a drift towards higher resistance values after 30 minutes annealing. After 4 hours annealing we start to observe a starting of the crystallization of some devices in both materials. The SET state is extremely stable without exhibiting any resistance drift or variability increasing in each composition analyzed. The improved retention observed in high Sb content layers, is likely related to the low nucleation rate featured by this materials at low temperatures [8].

D. Endurance analysis

The RESET current has been measured along cycling until 10^5 cycles realized with pulses with a duration of 10 µs for SET and RESET operations (i.e. long pulses are used to accelerate material degradation phenomena) and the results are reported in **Fig. 8**. The RESET current measured in Fig. 4, reduced in ML2 with respect to GST+Sb2, appears stable along cycling in both materials. Indeed, in TEM/EDX analyses performed on ML2 devices we demonstrate that the elemental distribution remains uniform in the active region of the cell even after cycling (**Fig. 9**), without elemental or phase segregation appearing, similarly to what observed already for bulk highly Sb-rich GST [8].

Contrarily to ML2 and GST+Sb2, ML1+N shows a degradation of the programming characteristics (i.e. increasing RESET current) and a reduction of RESET resistance already after 10^2 cycles (Fig. 8b). In order to explore the origin of the different endurance performance, we measured the threshold voltage for ML1+N (V_{th}) and we compared it to the one of GST+Sb2 and ML2 (**Fig. 10**). V_{th} is the voltage necessary to achieve the switching event in the amorphous phase of the material [23]. We observe an increased V_{th} (of almost 100%) in ML1+N with respect to high Sb content compositions. The higher V_{th} in ML1+N is in line with the higher resistivity of the RESET state observed in Fig. 6, being V_{th} proportional to the mobility gap [24]. A higher threshold voltage is responsible for a higher stress in the device during the switching event, leading to a likely accelerated degradation of the material properties (i.e. elemental or/and phase segregation) [25].

The endurance has been further studied in GST+Sb2 and ML2, that demonstrated from previous tests the best performances. SET/RESET cycling was executed applying pulses with a duration of 200 µs and overloading the RESET current measured in Fig. 4 and Fig. 5 in order to evaluate the sensitivity of the devices to the programming current variations. The results are reported in **Fig. 11**. ML2 can be programmed with a higher current overload (more than 20%) than GST+Sb2 without affecting the maximum endurance.

C2C and D2D variability were statistically analyzed in 4 kb arrays before and after endurance tests (**Fig. 12**). The SET variability is extremely low in both materials, as expected from the high crystal growth speed and the high crystalline homogeneity in Sb-rich alloys. The RESET state of GST+Sb2 presents a large tail towards low resistance values with a high C2C variability (Fig. 12a). Such tail is present since the beginning of the life of the devices, and their resistance becomes more and more variable along cycling (Fig. 12b). On the contrary, ML2 features a very high stability of the RESET resistance values, with a low C2C and D2D variability before and after accelerated endurance test. This demonstrates the interest of Multilayer in providing at the out of the fabrication an important reduction of the D2D electrical parameters variability.

IV. Discussions and conclusions

Multilayer deposition in Sb-rich GST alloys shows its advantage in an improved layer quality demonstrated first of all by a reduction of the device-to-device variability since the out-of-fabrication (Fig. 12). This is achieved despite the intermixing of the Sb and GST layers composing the Multilayer stacks happening already at temperatures close to 200°C (Fig. 2), and likely to happen during the BEOL of the fabrication at even higher thermal budget (i.e. several hours at 400°C). Indeed, the intermixing is not itself a problem, on the contrary it is favoring the crystallization of the layer (and even orienting it), as demonstrated by the reduced crystallization temperature observed in Multilayers with respect to equivalent bulk layers in RvsT measurements. We think that the reduction of the stochasticity of the crystalline grains size and orientation is the key for a reduced variability in the final devices, still preserving the advantageous properties of the target stoichiometry. High SET speed in tens of ns range (Fig. 6), data retention (Fig. 7), and endurance performances (Fig. 8) show the good alignment between Multilayer ML2 and bulk equivalent GST+Sb2, thanks to the matched composition obtained in the active volume of the device. Even the high

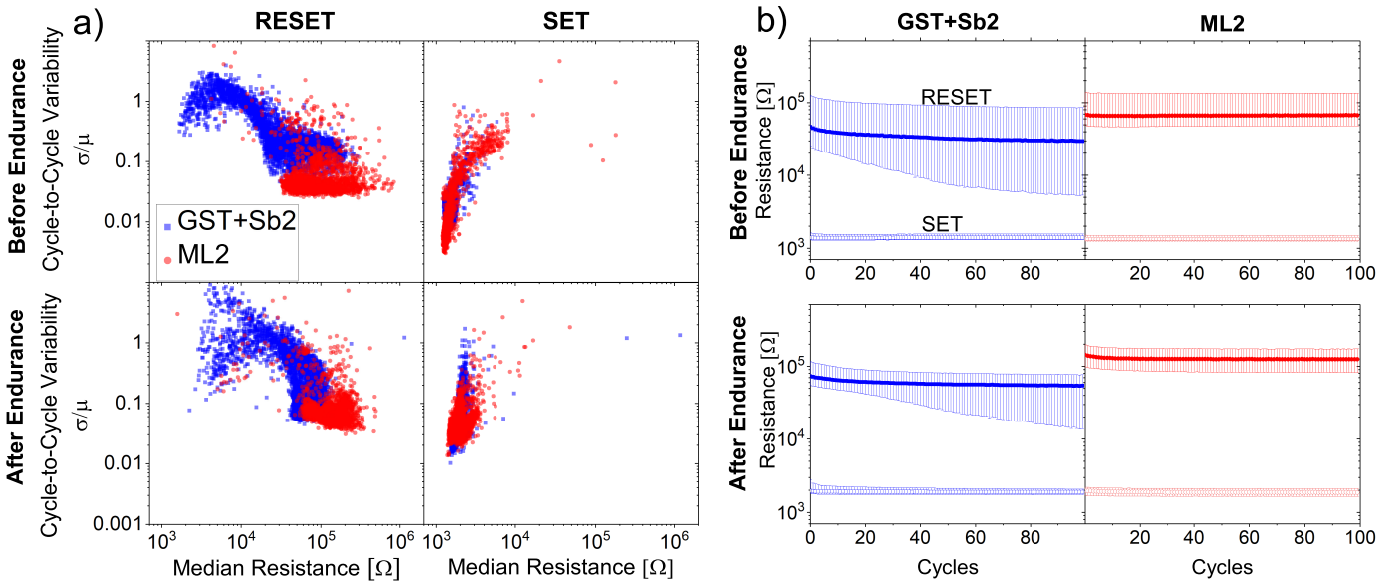

Fig. 12: Variability of the SET and RESET states evaluated along 100 programming cycles (SET/RESET pulses of 50 ns) in 4 kb arrays, before and after an sequence of 10^3 cycles (performed with 10 µs SET/RESET pulses for an accelerated aging of the devices). a) cycle-to-cycle: each point in the graphs represents the variance of the resistance value (for both RESET and SET state) of a single device normalized with respect to its median resistance along 100 cycles. b) device-to-device: median and standard deviation for the 4 kb devices resistance values along the 100 cycles.

compositional stability after cycling, previously observed in Sb-rich GST, is confirmed for Multilayer (i.e. ML2 in Fig. 9). We think that this is directly linked to a reduced impact of the switching operation in high Sb content materials thanks to the reduced switching voltage V_{th} (Fig. 10).

While the optimal speed and endurance performances of Sb-rich GST alloys are preserved in Multilayer stacks, in these latter we observed in general a reduction of the RESET programming current statistically demonstrated in 4 kb arrays (Fig. 4 and Fig. 5). This reduction is confirmed even after array cycling (Fig. 8). It could be likely related to the higher in-plane thermal conductivity expected in Multilayers due to a more uniform and oriented crystalline morphology. Such property is beneficial for the reaching of a uniform temperature distribution over the heater, reducing the programming current needed to achieve the complete amorphization of the phase-change material [26]. In addition, Multilayer Sb-rich GST revealed a lower sensitivity to current overload (Fig. 11), and it could be as well due to the enhanced thermal conductivity of the layer, better dissipating the overheating that such overload could generate. This is fundamental to reduce the sensitivity of the PCM devices to variations of the controlled programming current caused by parameters related to the design/layout of the array.

Finally, Sb-rich GST Multilayers enable a high reduction of the device-to-device variability that is intrinsic of the uncontrolled crystallization of bulk PCM layers happening during the fabrication process. This result enables high yield in high density memory arrays and nm scaled devices, targeting SCM applications and next generation of PCM for DRAM replacement.

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