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***Abstract*—In this work, we present the extensive electrical characterization of 4kb Phase-Change Memory (PCM) arrays based on "Wall" structure and Ge-rich GeSbTe (GST) material, integrating a SiC dielectric with low thermal conductivity surrounding the heater element for enhanced cell thermal efficiency. We investigate the effects of the introduction of such dielectrics on the electrical performances of the device and we provide a promising path to achieve energy-efficient PCM cells supporting our results by electro-thermal TCAD simulations.**

I. Introduction

Phase-Change Memory (PCM) is a non-volatile, scalable and mature memory technology, that has proven to be of great interest for embedded applications. In order to target automotive requirements, memory devices need to demonstrate good data retention in high temperature environment and low power consumption. The first requirement was achieved in PCM by material engineering, thanks to the introduction of Ge-rich GeSbTe (GGST) chalcogenide alloys, which provide great retention capability of more than 10 years at 185°C [1]. Thanks to this breakthrough, PCM became a suitable candidate, introduced in advanced CMOS technology nodes such as 28 nm and even 18 nm [2]. The programming current reduction to target portable and low power applications remains an important goal to reach and the main development axes are scaling [3, 4], material engineering [5], and thermal optimization [6]. Indeed, the perfect PCM cell would exploit adiabatically all the power generated during the heating of the chalcogenide layer, necessary to perform the phase change transition from the amorphous (highly resistive i.e. RESET) to the crystalline phase (lowly resistive i.e. SET). On the contrary, a significant part of this power is lost, and in particular through the dielectrics surrounding the heating element of the device [7]. In previous studies, it was demonstrated that replacing the dielectric encapsulating the PCM layer by an optimized one featuring low thermal conductivity can lead to a reduction of the programming current, as well as an improved reliability [8, 9]. However, in a heater-based "Wall" architecture (**Fig. 1**), recognized as a PCM cell solution with a great optimization potential [4], most of the heat is generated inside the heater itself, hence the dielectrics surrounding this element should be carefully optimized. In this work, we study the effects of the introduction of a SiC dielectric presenting a low thermal conductivity around the heater of a "Wall" PCM structure to enhance its thermal isolation. Through electrical characterization, we analyze the programming characteristics, the endurance and the retention at statistical level in 4kb arrays and the results are compared to the ones obtained from standard SiN-based devices. Electro-thermal TCAD simulation is used to support our observations and our solutions for further device optimization. Despite some process challenges to be overcome, we present promising paths for next-generation thermally-optimized PCM cells.

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II. SiC vs SiN-based 4kb PCM Electrical Characterization

We integrated GGST materials in "Wall" PCM devices fabricated in the Back-End-of-Line (BEOL) of CEA-LETI Memory Advanced Demonstrators (MAD) based on 130 nm CMOS technology, for single device analysis and 4kb statistical electrical parameters evaluation. The critical dimension (unless specified differently) corresponding to the width (w) of the heater element is 80 nm. The heater is surrounded by three dielectrics, namely A and B as reported in Fig. 1, and the encapsulation dielectric layer that covers up the sides of the entire device as described in [9]. We considered devices with encapsulation and dielectric B based on standard SiN, and varying the dielectric A fabricated either with SiN or SiC. We will address in the following the PCM devices with respect to the material integrated as dielectric A. Our SiC dielectric has a low thermal conductivity (k_{th}) of about 0.4 $Wm^{-1}K^{-1}$, while for SiN it is close to 1.4 $Wm^{-1}K^{-1}$ as measured in [8]. The heater element has a resistance of about 1 kΩ.

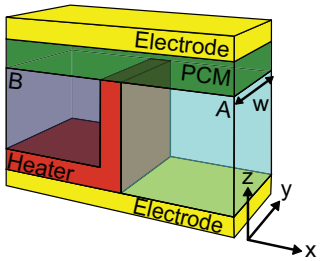

Fig. 1. Description of a "Wall" PCM device. The dielectrics integrated on the two sides of the heater are named respectively A (SiN or SiC) and B (SiN).

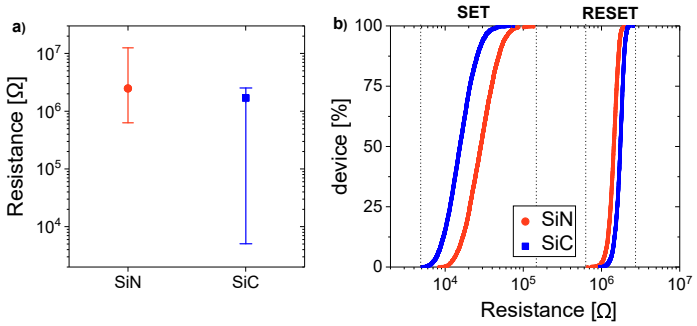

Fig. 2. a) Median virgin resistance with error bars defined as minimum and maximum values. b) Cumulative distributions in the 4kb array of the SET and RESET resistance states after initialization, for both SiC and SiN-PCM.

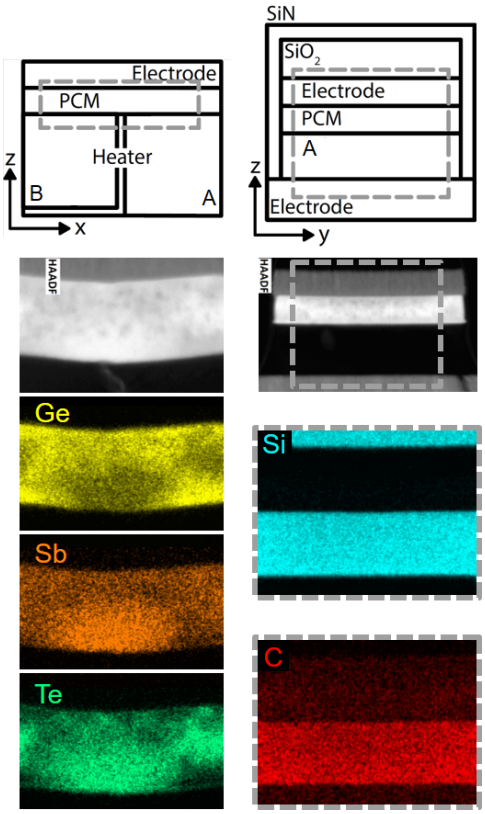

Fig. 3. Left: schematic view of a cross-section orthogonal to the heater width (z,x-plane) with High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) and Energy Dispersive X-Ray (EDX) maps of the active volume of a SiC device (with w = 300 nm), showing a Ge enrichment at the edges of the active volume and increased Sb and Te concentrations compatibly with previous observations [1]. Right: description and HAADF-STEM image of a cross-section parallel to the heater width (z,y-plane), along with EDX images of the silicon and carbon distributions.

A. Programming characteristics

The virgin resistance of the devices measured after fabrication is reported in **Fig. 2a**. We can deduce from the spread of the resistances in SiC devices a likely crystallization of the GGST layer already triggered during the BEOL fabrication. After an initialization protocol to bring the cells into a stable SET state, we programmed the matrices in the RESET state using a sequence of pulses with increasing voltage amplitude

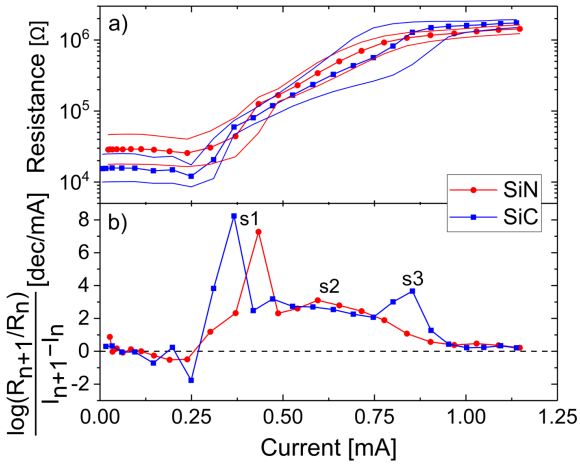

Fig. 4. RI characteristics for both SiN and SiC 4kb PCM arrays, obtained with staircase protocol (pulse width = 300 ns, fall-time = 10 ns). Median resistance with 15%-85% confidence interval is reported as a function of the programming current (a), associated with the evolution of the slope s of each curve (b).

(i.e. staircase protocol). We obtained the cumulative distributions of the SET and RESET states presented in Fig. 2b. For both SiN and SiC based devices a good functionality is achieved in the whole 4kb array, with a wider resistance window for SiC, mainly related to its capability to achieve a lower SET resistance. The HAADF-STEM analyses coupled to EDX maps on a SiC device after programming are reported in **Fig. 3.** The Si and C maps show the successful integration of SiC dielectric in the PCM device. Moreover, we observe an elemental segregation in the active volume of the cell [1] leading to a Ge accumulation outside of the active volume, expected in GGST-based PCM.

Resistance versus current (RI) characteristics for both SiC and SiN 4kb arrays are reported in **Fig. 4** with the associated derivative that was correlated to the thermal properties of the material surrounding the PCM cell [9] (i.e. $s = \Delta logR/\Delta I \propto 1/\sqrt{k_{th,eff}}$ with $k_{th,eff}$ the effective thermal conductivity of the materials surrounding the active volume). We observe three current ranges corresponding to different values of s. In the first one (*s1*), the heat is mainly generated inside the GGST layer. As soon as the current increases, the chalcogenide layer becomes extremely conductive and the heater element starts to have the highest resistive contribution, leading to a gradual displacement of the maximum temperature from the GGST layer to the heater element itself (*s2*). The effect of the presence of low thermal conductive SiC can be visible only at higher current values (*s3*), with an increase of s parameter in SiC devices that is not present in SiN.

In order to investigate the effect of the presence of SiC dielectric around the heater element on the SET performances of the device, we performed SET resistance cartographies as a function of the programming current and of the fall-time of the SET pulse (i.e. the duration of the falling edge of the pulse). The devices were pre-programmed in the RESET state before each SET pulse and the results are reported in **Fig. 5**. Confirming previous results, the SiC PCM devices present a

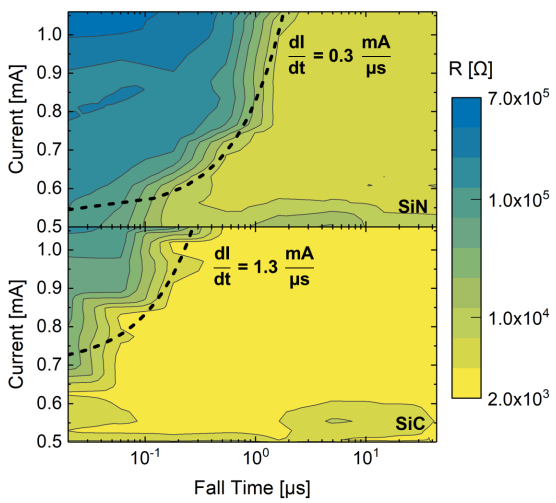

Fig. 5. SET resistance cartographies as a function of the programming current and of the duration of the falling edge of the SET pulse (pulse width kept constant at 300 ns). Median values from 30 cells with 100 nm heater width are reported. Dashed lines represent the current over fall-time rate necessary to achieve the SET state in both SiC and SiN (SET state = 10% of the Resistance window).

faster crystallization as their resistance decreases already for short fall-times. This can be quantified by calculating from the graphs (dashed lines) the minimum current over time rate necessary to reliably SET the cells. We find a 4× difference in the minimum falling edge slope necessary to crystallize SiC with respect to SiN PCM.

Combining the already presented results, we observe an enhanced crystallization in SiC PCM with respect to SiN even during BEOL fabrication, i.e. independently from programming operations (Fig. 2a). We think that the lower density of SiC could increase the surface roughness and enhance the oxidation propensity of SiC with respect to SiN. This could favor heterogeneous crystallization phenomena at the chalcogenide/SiC interface already at BEOL-like temperatures (i.e. 300°C-400°C) [10]. If these phenomena can also contribute to the higher SET capability of SiC devices, we should consider that the improved thermal isolation can induce a different behavior of the device during the initialization step (i.e. called "forming"). In particular, we expect a higher temperature reached in the case of SiC with respect to SiN, leading to a reduced Ge content in the active volume (i.e. higher Ge expulsion towards the edges). A lower Ge content is then compatible with an improved SET capability (Fig. 5). Moreover, the increased thermal resistance of the device thanks to the SiC introduction is responsible for a slower cooling (i.e. higher thermal time constant) that contributes to enhance crystallization even for short SET fall-times (Fig. 5). Such improved crystallization in SiC PCM can also explain the limited effect observed on the programming current reduction in our devices. Indeed, since the crystallization is favored in SiC PCM in the range of currents compatible with *s2* (Fig. 4), the benefit from a higher thermal isolation that should lead to a higher amorphized volume with respect to SiN (i.e. higher resistance) is compensated by a reduction of the final effective

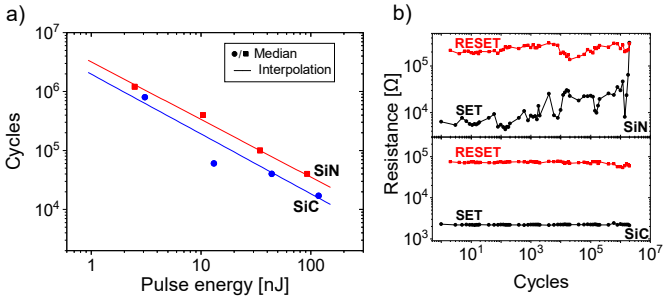

Fig. 6. a) Median (based on 25 devices) of the number of cycles until failure as a function of the total energy of the SET+RESET programming, modulated by varying the width of the SET and RESET combination of pulses. Lines are linear regressions of the data. b) Example of endurance tests performed with same programming conditions for SiN and SiC PCM.

amorphized volume due to the enhanced crystallization during the falling edge of the applied RESET pulse. Only at high current (range *s3*) the thermal isolation improvement is visible, when current decrease rates at the falling edge are sufficiently low to avoid any unwanted crystallization.

B. Endurance and Data Retention

We compared endurance of both SiC and SiN devices using combination of SET and RESET pulses with increasing duration (i.e. increasing energy). In **Fig. 6a**, we report the maximum endurance achieved for a given combination of SET and RESET duration. Although the endurance of SiC devices seems slightly lower, we consider the difference insignificant as we usually compare orders of magnitude. On the contrary, we can observe the reliable resistance window achievable (without any smart programming protocol) up to more than 10^6 cycles, likely favored by the enhanced SET capability in these devices (Fig. 6b). Hence, the SiC does not seem to severely affect the endurance performance of GGST.

Data retention tests performed on 4kb arrays by isochronal annealing of one hour at increasing temperatures are reported in **Fig. 7**. As expected from programming characteristics analyses, SiC PCM exhibits a slightly lower data retention with respect to SiN. Indeed, SiC RESET (and SET) population shows a more advanced re-crystallization at 240°C, still preserving good retention performances.

III. PCM Device Thermal Optimization

We reported on the effects of the introduction of SiC in our "Wall" PCM to enhance the thermal isolation of the heater element. The electrical/thermal optimization of the PCM cell should preliminarily consider the matching of the heater resistance with the chalcogenide layer resistance in order to maximize the efficiency of the heating as previously reported in [11]. Such matching is responsible for a localization of the heating at the heater/chalcogenide material interface reducing the losses and the power needed to completely amorphize the active volume in the PCM. To further investigate how the thermal conductivity of the dielectric A in Fig. 1 can change the cell behavior, we performed 3D TCAD electro-thermal simulations using a PCM dedicated tool relying on Sentaurus

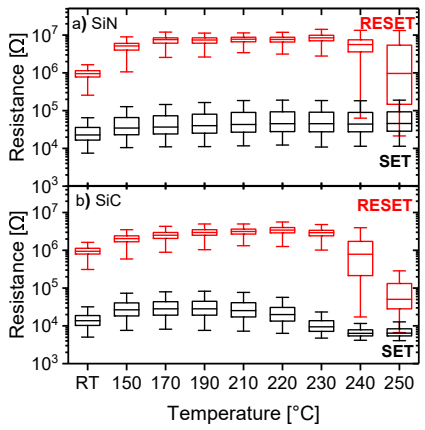

Fig. 7. Data retention tests performed by isochronal annealing of 1 hour at increasing temperatures for SiC and SiN devices.

Device [12]. Our electro-thermal model considers a PCM material whose electrical conductivity depends on temperature (based on electrical data fitting). To study the role of the heater resistance, we considered two structures, with a heater resistance of 1 kΩ (like in our electrical tests) and 5 kΩ respectively. In **Fig. 8a**, we observe that lowering the thermal conductivity of dielectric A from 2.5 $Wm^{-1}K^{-1}$ to 0.5 $Wm^{-1}K^{-1}$ induces an increase of the maximum temperature inside the chalcogenide of about 8% for the low resistive heater and more than 15% for the highly resistive heater. Dielectric B (Fig. 1) replacement by SiC would enhance even more such gain (not reported). Moreover, we think that phenomena related to electric field activated conduction in the chalcogenide (not considered in the used tool), would contribute to an even higher gain from the heater thermal isolation on the thermal efficiency of the PCM cell [13]. Finally, we report in Fig. 8b the temperature profile comparison achieved for both 1 kΩ and 5 kΩ heater resistances, with a high and a low thermal conductivity simulated for dielectric A ($k_{th,A}$). Note that the low resistive heater exhibits bigger melted volume inside the PCM layer, which is expected since the heat is generated directly inside the chalcogenide. However, the required power to melt this zone is also higher. Therefore, here, we are only interested in the benefit from an improved thermal isolation of the heater element, which is higher in 5 kΩ device.

IV. Conclusions

We analyzed the electrical performances of a thermally optimized "Wall"-based PCM in 4kb arrays. We could evidence the effects of the integration of a SiC dielectric featuring low thermal conductivity on one side of the heater element. SiC PCM showed high SET speed and higher general propensity to crystallization, likely due to both interface and thermal related phenomena that contribute to reduce in such devices the effective gain on programming current reduction. We highlighted in RI characteristics analyses, how the higher thermal isolation in low resistive heater-based cells becomes interesting at high current, when the heating is mainly localized inside the heater.

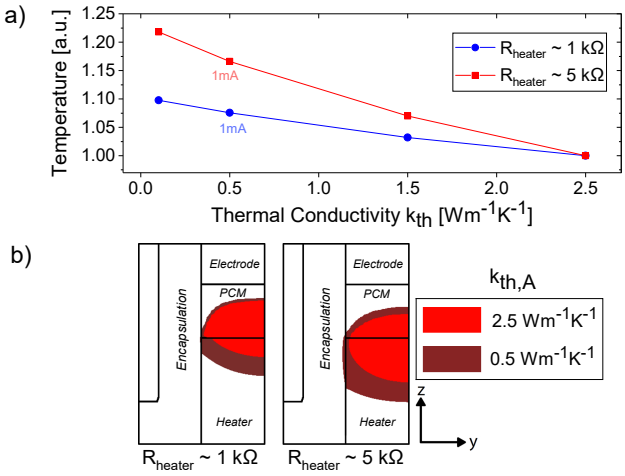

Fig. 8. a) Evolution of the maximum temperature reached inside the chalcogenide material in the PCM cell, depending on the thermal conductivity of the dielectric A ($k_{th,A}$) and for two different values of heater resistance. Temperature is normalized and is obtained from equivalent programming currents. b) Temperature profile (region that during RESET current application achieves a temperature higher than 930 K) achieved in the two devices for a low and a high thermal conductivity dielectric A. Based on the same maximum temperature obtained for $k_{th,A}$ = 2.5 $Wm^{-1}K^{-1}$

Finally, thanks to 3D TCAD simulations, we showed how coupling SiC dielectric integration demonstrated in our PCM cells with an optimized heater resistance can lead to better thermal efficiency in future generations of PCM technology.

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