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Pedro Fernandes Paes Pinto Rocha, Laura Vauche, Blend Mohamad, William Vandendaele, Eugénie Martinez, et al.. Impact of Post-Deposition Anneal on ALD Al₂O₃/etched GaN Interface in Gate-First MOSc-HEMT Process Flow. GaN MARATHON, Jun 2022, Venise, Italy. cea-03846232

HAL Id: cea-03846232

<https://cea.hal.science/cea-03846232v1>

Submitted on 10 Nov 2022

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Impact of Post-Deposition Anneal on ALD Al₂O₃/etched GaN Interface in Gate-First MOSc-HEMT Process Flow

P. Fernandes Paes Pinto Rocha, L. Vauche, B. Mohamad, W. Vandendaele, E. Martinez, T. Spelta, N. Rochat, R. Gwoziecki, B. Salem, V. Sousa

Abstract— In this work, we investigate the impact of Post-Deposition Anneal (PDA) of Atomic-Layer Deposited (ALD) Al₂O₃ on etched GaN for MOS-channel High Electron Mobility Transistors (MOSc-HEMTs) Gate-First process flow using C-V measurements carried out on MOS capacitors (MOSCAPs). For PDA up to 500°C, a reduction of the flat-band voltage hysteresis (ΔV_{FB}) is reported and explained by the reduction of Ga-O bonds and O-H groups observed by Hard X-Ray Photoelectron Spectroscopy (HAXPES) analysis, the latter being confirmed by Fourier Transform Infrared Spectroscopy (FTIR). For a 600°C PDA, Grazing Incidence XRD (GIXRD) analysis shows a small crystallized κ -Al₂O₃ signal on etched GaN, which is absent for as-grown GaN. This beginning of crystallization could explain the degradation in ΔV_{FB} and breakdown field for PDA above 500°C observed on MOSCAPs after the Gate-First process flow overall thermal budget.

I. INTRODUCTION

THE MOS-channel HEMT (MOSc-HEMT) with its fully recessed MOS architecture is an attractive solution among normally-off HEMTs for power conversion systems. However, the threshold voltage (V_{TH}) strongly depends on the gate dielectric Al₂O₃/etched GaN interface properties [1]. Post-Deposition Anneal (PDA) of Al₂O₃/GaN has been reported to increase the threshold voltage (V_{TH}) and reduce its hysteresis (ΔV_{TH}) [2], [3]. However, most of these reports are for Al₂O₃ deposited on as-grown GaN for Gate-Last process flow. Since our process flow is Gate-First [4], we study the impact of Al₂O₃ PDA deposited on etched GaN for the Gate-First process flow.

II. EXPERIMENTAL

30nm Al₂O₃ was deposited by Atomic Layer Deposition (ALD) at 300°C using TMA and H₂O on dry etched nGaN/Si MOCVD wafers ($N_D=5.10^{17}$ cm⁻³) to simulate the MOSc-HEMT gate processing. PDA was performed under N₂ 1) for 4 min at 400, 500, and 600°C on samples or 2) for 5 min at 400, 500, and 550°C on 200mm wafers. MOSCAPs test structures were fabricated: 1) on 1.5 cm × 1.5 cm GaN samples with Ni/Au

metal contact (MOS-1) and 2) on 200 mm GaN wafers with TiN metal contact (MOS-2). The MOS-2 devices were annealed after metal deposition to simulate the Gate-First thermal budget. C-V measurements were carried out at 1 kHz with a voltage sweep from -4V to 6V and back to -4V. I-V measurements were performed from 0V to 60V. 15nm Al₂O₃/etched GaN samples were analyzed by Hard X-Ray Photoelectron Spectroscopy (HAXPES) (Cr K α =5414.7eV) and Grazing Incidence XRD (GIXRD). For Fourier Transform Infrared Spectroscopy (FTIR), 30nm Al₂O₃/p-Si samples were analyzed.

III. RESULTS

For MOS-1, we observe a reduction of Flat Band voltage hysteresis (ΔV_{FB}) (Fig. 1, 2). This trend is correlated to O-H groups reduction observed both by FTIR (Fig. 4) and HAXPES analyses (Fig. 5), and to Ga-O bonds reduction observed by HAXPES (Fig. 5), in agreement with literature [5], [6]. For MOS-2, the impact of PDA is minimized with low ΔV_{FB} (Fig. 1, 2) and similar Flat Band voltage (V_{FB}) (Fig. 1, 3), which we attribute to a beneficial impact of the final thermal budget. Hence, PDA until 500°C seems beneficial. However PDA above 500°C seems detrimental, with a decrease of V_{FB} for MOS-1 (Fig. 1, 3), an increase of ΔV_{FB} for both test structures (Fig. 2), and a degradation of breakdown field for MOS-2 with two populations (Fig. 6). The latter effect could be explained by the beginning of Al₂O₃ crystallization at 600°C observed by GIXRD (Fig. 7), and not seen for Al₂O₃ on as-grown GaN, further consolidating the detrimental impact of PDA above 500°C on etched GaN. Therefore, we demonstrate that the impact of PDA is influenced by the overall thermal budget and the GaN prior processing; these parameters should be taken into account when optimizing the PDA for the Gate-First approach.

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This abstract was submitted the 08 march 2022. This work was funded by the PSPC French national program “G-Mobility” and partly supported by the French RENATECH network through the PTA technological platforms.

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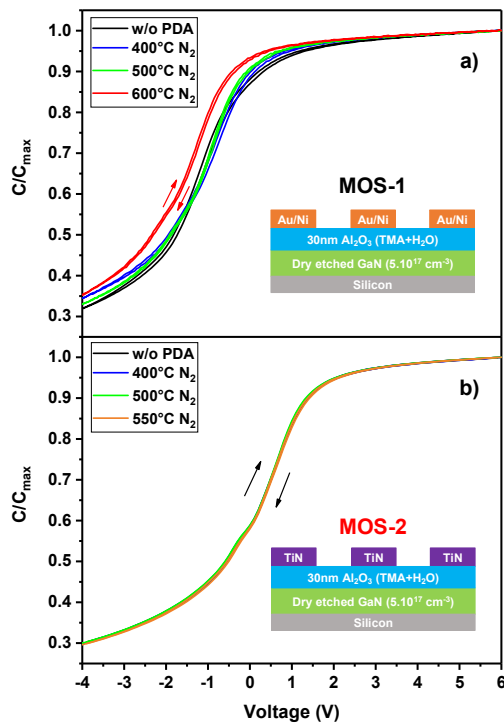


Fig. 1: Normalized C-V characteristics at 1 kHz for a) MOS-1 devices (median of five measurements) and b) MOS-2 devices (median of nineteen measurements) at different PDA temperatures.

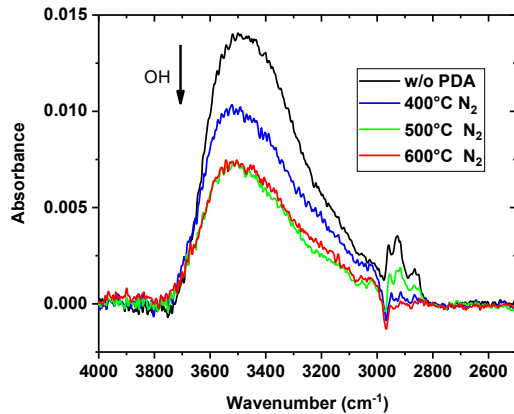


Fig. 4: FTIR O-H absorbance spectrum for 30nm Al₂O₃ on p-Si with different PDA temperatures and without final thermal budget. A manual correction of base line was done.

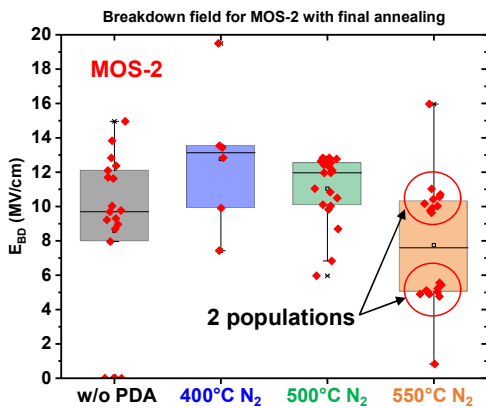


Fig. 6: Breakdown field obtained from I-V measurements of MOS-2 devices after the final thermal budget. 550°C has a degradation of E_{BV} with two populations.

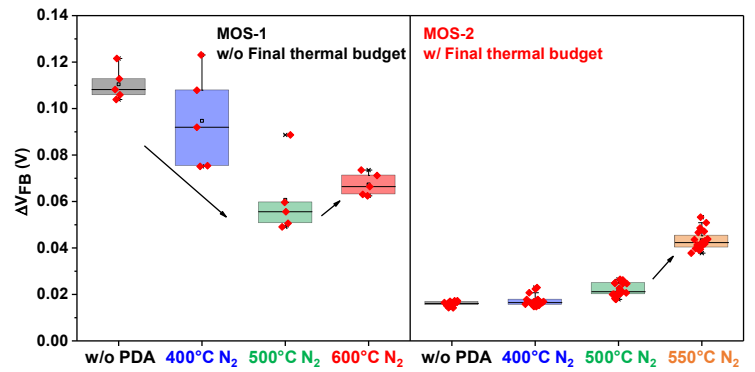


Fig. 2: Clockwise ΔV_{FB} for MOS-1 and MOS-2 extracted from Fig. 1. For PDA until 500°C, a reduction of ΔV_{FB} is noticed for MOS-1, but absent for MOS-2. After 500°C, ΔV_{FB} increases for both test structures.

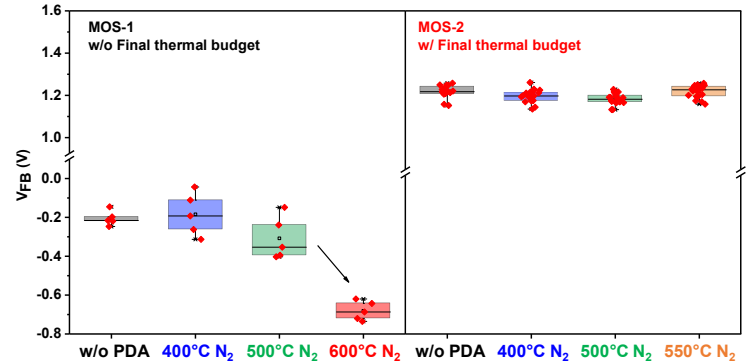


Fig. 3: V_{FB} for MOS-1 and MOS-2 extracted from Fig. 1. A minimized impact of PDA is noticed for MOS-2. After 500°C, V_{FB} decreases for MOS-1.

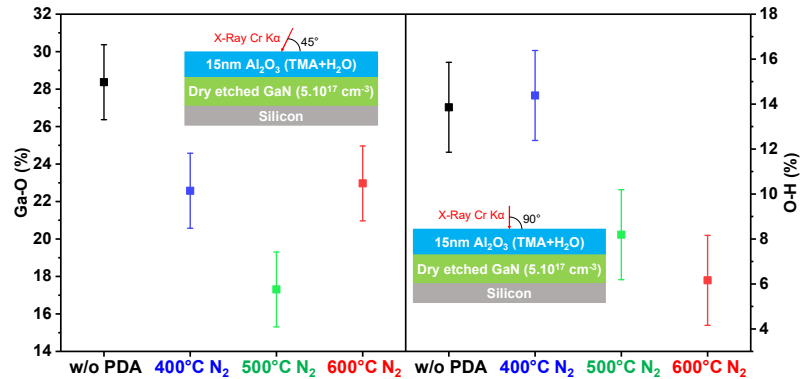


Fig. 5: HAXPES extracted chemical environment on dedicated samples with 15nm Al₂O₃ on etched GaN for different PDA temperatures and without final thermal budget. The take-off angle was 45° for Ga 2p_{3/2} and 90° for O 1s analysis.

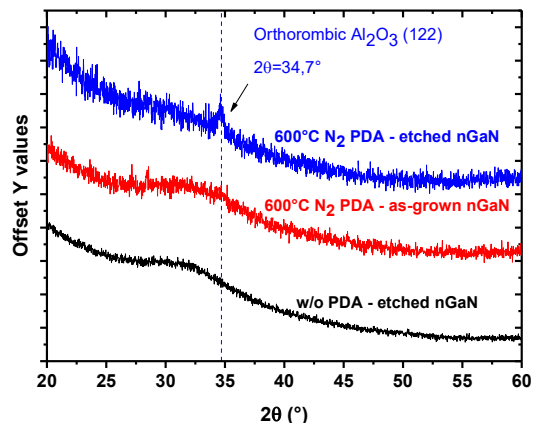


Fig. 7: GIXRD analysis with grazing angle of 2° for 15nm Al₂O₃ on etched GaN with and without 600°C PDA, and for 15nm Al₂O₃ on as-grown GaN with 600°C PDA. A small signal of orthorhombic κ -Al₂O₃ (122) is observed.