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# High power 2.5D integrated thermoelectric generators combined with microchannels technology

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## Abstract

We have developed high power integrated thermoelectric generators ( $\mu$ TEGs). These  $\mu$ TEGs are CMOS compatible, i.e. based on polycrystalline SiGe materials. These  $\mu$ TEGs have been processed directly on a silicon interposer. Even if poly-SiGe exhibits low thermoelectric performances at room temperature, the specific design and proposed architecture enable  $\mu$ TEGs to deliver up to 680  $\mu$ W for a temperature difference at 15.5 K. To reach such high power, an original 2.5D structure has been developed and  $\mu$ channels technology has been associated, below the  $\mu$ TEG, to dissipate heat coming from the hot side.  $\mu$ TEGs have been tested in real environment, located below a hot test chip. Such  $\mu$ TEG performances overtake those from similar state-of-the-art CMOS compatible devices, and pave the way for a potential use in different applications such as sensors power supply or battery charger.

## 1. Introduction

The need in energy in integrated circuit (IC) systems is considerable. For example, it can be used to supply sensors, or load battery. Due to obvious sizing considerations, only thermoelectric (TE) thin film technology can be used in this field. Standard bulk technology is usually made of millimetric legs integrated between two ceramics plates, making them incompatible for an optimized integration in IC environment.

In TE thin films technology, where compactness seems compatible with integration in IC systems, only stand-alone micro-thermoelectric generators ( $\mu$ TEG) have been commercially

available, mainly developed by  $\mu$ Pelt and Laird Technologies. For both suppliers, the proposed  $\mu$ TEG microarchitecture is called 3D, i.e. made from cubic TE legs: n and p-type materials are deposited and etched separately on two different wafers, which are then bonded and the final device is obtained after dicing steps. Typical value for such  $\mu$ TEGs is a power density of 24 mW/cm<sup>2</sup> at a temperature difference  $\Delta T$  of 5 K [1]. If these  $\mu$ TEGs propose high electrical performances, they have some drawbacks. These devices are based on Bi<sub>2</sub>Te<sub>3</sub> materials, the best TE material at room temperature, with a figure of merit  $ZT$  around 1 at 300 K [2]. But these materials are rare and expensive, and not compatible with CMOS and in-IC processes due to contamination, regulation and ROHS (Restriction of the use of certain Hazardous Substances in electrical and electronic equipment) issues. Moreover the presence of two substrates adds parasitic thermal resistances, decreasing the effective thermal gradient at the extremities of the active TE materials, and therefore the overall performance. Finally, these devices are stand-alone, and so cannot be integrated. Considering in-IC compatible  $\mu$ TEGs, it has been reported in literature some devices, mainly planar polysilicon based  $\mu$ TEGs or silicon nanowires based  $\mu$ TEGs. In the first case, they can exhibit power equal to 12.3  $\mu$ W/cm<sup>2</sup> for  $\Delta T$  at 31.5 K [3], 1.3  $\mu$ W/cm<sup>2</sup> for  $\Delta T$  at 5 K [4], 4.5  $\mu$ W/cm<sup>2</sup> for  $\Delta T$  at 5 K [5] or 320  $\mu$ W/cm<sup>2</sup> for  $\Delta T$  at 17 K [6]. In the second case, they can exhibit power equal to 1.88  $\mu$ W/cm<sup>2</sup> for  $\Delta T$  at 70 K [7]), 1.5 mW/cm<sup>2</sup> for  $\Delta T$  at 300 K [8], or 12  $\mu$ W/cm<sup>2</sup> for  $\Delta T$  at 5 K [9].

In this paper, we developed  $\mu$ TEGs based on polycrystalline SiGe materials. Even if this material exhibits poor TE performances (figure of merit  $ZT$  around 0.1 at 300 K [10]), it is fully compatible with CMOS environment.

To compensate low SiGe performances at the materials level, our  $\mu$ TEGs are based on two main technological bricks: the use of microfluidic channels and a specific 2.5D architecture.

For the first brick, the effective integration of commercially available  $\mu$ TEGs into an IC environment is mainly hindered by the absence of an efficient cold source, which is absolutely needed to achieve significant temperature gradients across  $\mu$ TEGs, and so high power. The presence of microfluidic at the interposer level bears the promise of an efficient thermoelectric energy harvesting. This technology that we have patented [11] enables to spread the heat coming from the  $\mu$ TEG hot side (typically electronics chips) and to obtain higher temperature differences.

Moreover, the use of microfluidic technology is already used in CMOS application [12] underlining that this concept is compatible with IC environment.

For the second brick, we developed an optimized 2.5D architecture, specifically designed to concentrate the heat from chips to the hot part of TE legs.

Indeed, as represented in Figure 1, classical TEGs architectures are planar (2D) or orthogonal (3D). In 2D architecture,  $\mu$ TEGs are made of p-type and n-type lines, with both planar heat flow and electrical current (Figure 1a). In 3D architecture (case of  $\mu$ TEGs from the state-of-the-art),  $\mu$ TEGs are made of p-type and n-type cubes, with both cross-plane heat flow and electrical current (Figure 1b). In 2.5D architecture,  $\mu$ TEGs are made of segmented lines, each line alternating p-type and n-type segments, with a cross-plane heat flow and a planar electrical current (Figure 1c). As summarized in Table 1, the 2.5D architecture offers many advantages compared to the two others. With 2D architecture, lines enable achieving higher temperature differences than 3D as the two extremities can be away from each other (until few millimeters), but leading to an increase of the electrical resistance. On the contrary, for 3D structures, the temperature difference is generated at the extremities of the TE film thickness (until few tens of microns). It leads to low electrical resistance but low temperature difference. Moreover, as TE films are deposited directly on metal contacts (see Figure 1b), monocrystalline materials cannot be used in these  $\mu$ TEGs. The 2.5D architecture, thanks to its original configuration, enables achieving higher  $\Delta T$  than 3D. Indeed, the 2.5D architecture converts the cross-plane thermal flow at the system level in an effective planar one at the thermoelectric level. Figure 2 represents schematically a cross view of our optimized 2.5D architecture. As it can be shown, TE materials are directly deposited on a silicon interposer. From the hot side, the chip is thermally “connected” to the  $\mu$ TEG via metal micro-pillars (only few microns separate the micro-pillars from the  $\mu$ TEG to avoid electrical short circuits). These  $\mu$ pillars enable to concentrate the heat on the TE junctions’ hot side. From cold side, the integration of air gap microchannels below the  $\mu$ pillars leads the heat flow to go in the direction of TE junctions’ cold side. The heat flow is finally spread thanks to the water channels located below the air gap.

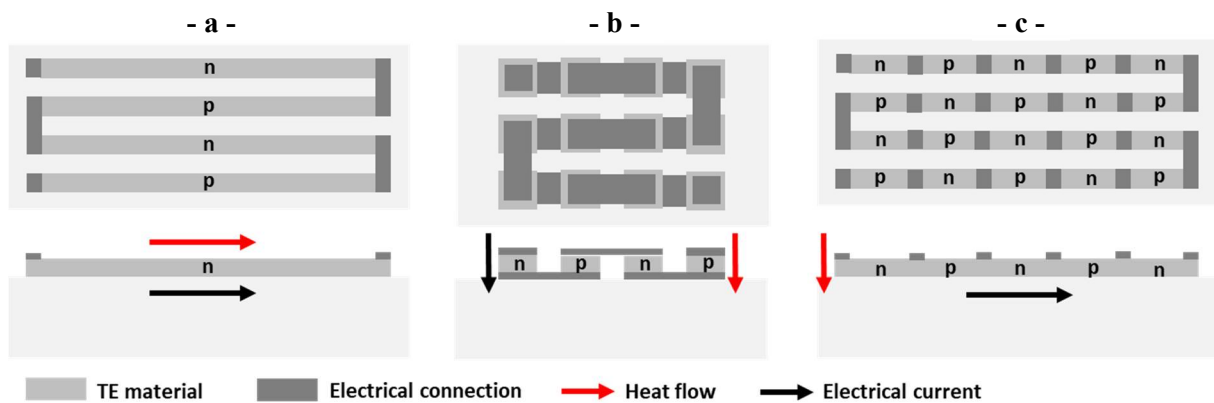


Figure 1 – Schematic top view and cross view of 2D (a), 3D (b) and 2.5D (c) architectures.

Table 1 – Main advantages and drawbacks of the three architectures.

Main parameters	2D	3D	2.5D
Temperature difference $\Delta T$	***	*	**
Electrical resistance $R_{int}$	*	**	**
Number of junctions N	*	***	***
Nature of materials	***	*	***

\* low values; \*\* intermediate values; \*\*\* high values.

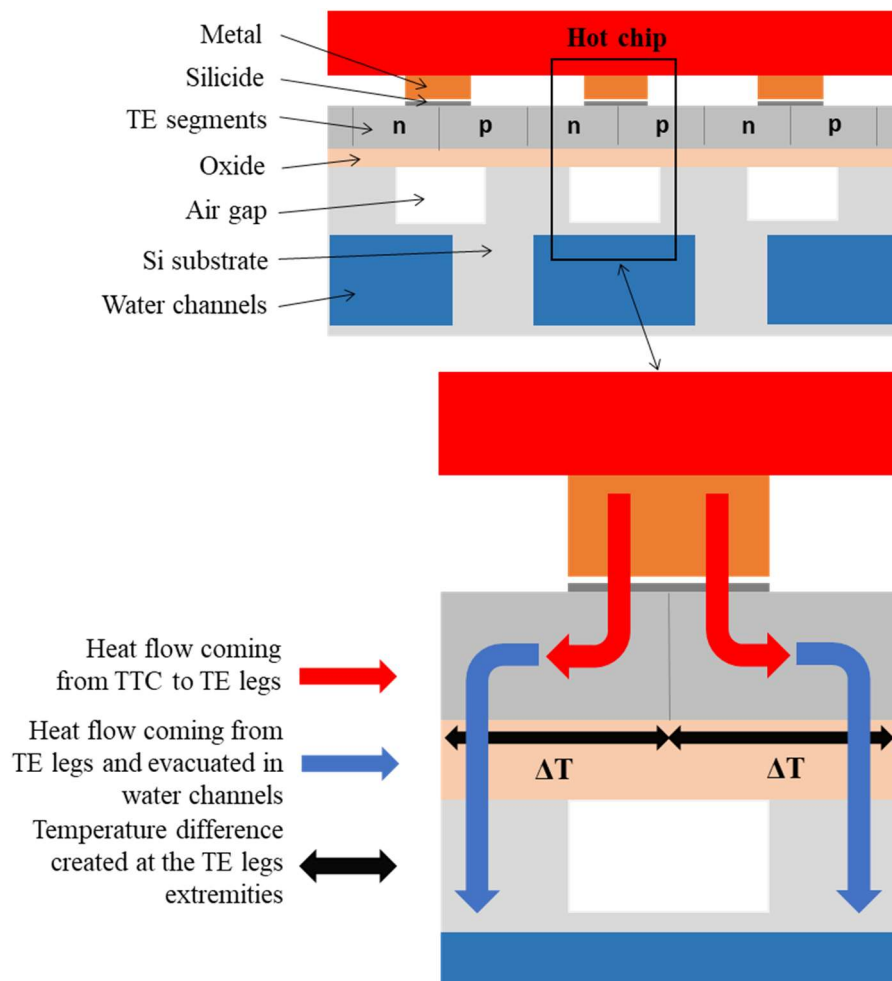


Figure 2 – Schematic cross view of our optimized 2.5D structure, underlining the heat path: from the heat concentration on TE hot junctions to the heat spreading with the channels.

This 2.5D architecture has already been reported in literature [3] but very rarely and only for stand-alone devices. It is the first time that this architecture will be applied to  $\mu$ TEGs in in-IC environment. The main electrical  $\mu$ TEGs characteristics are the power and voltage generated. The useful electrical power  $P_u$  generated by a standard  $\mu$ TEG is given by:

$$(1) P_u = V_{oc}^2 / 4 R_{int}$$

with  $V_{oc}$  the open circuit voltage and  $R_{int}$  the internal electrical resistance of  $\mu$ TEG, defined by:

$$(2) V_{oc} = N \times S_{np} \times \Delta T = N \times (S_p - S_n) \times \Delta T$$

$$(3) R_{int} = N \times (\rho_n + \rho_p) \times L / A + R_{met} + R_c$$

with  $S_p$ ,  $S_n$ ,  $\rho_p$ ,  $\rho_n$  the Seebeck coefficient and the electrical resistivity of p-type and n-type TE materials, respectively,  $N$  the number of junctions,  $L$  and  $A$  the length and area of TE legs,  $R_{met}$  the total resistance of metal connections between legs,  $R_c$  the total contact resistance and  $\Delta T$  the temperature difference between the extremities of the  $\mu$ TEG.

To maximise  $\mu$ TEGs performances, it is first necessary to optimize their geometry.

## 2. $\mu$ TEGs sizing and design optimisation

As introduced in the previous section and as it will be described in section 3,  $\mu$ TEGs are positioned on the interposer and under the hot sources, i.e., the thermal test chips (TTCs). In Figure 3, the main geometric parameters of a  $\mu$ TEG are shown: length  $L_{TEG}$  and width  $W_{TEG}$  of the  $\mu$ TEG, length  $L_{seg}$ , number  $N_{seg}$  of n/p segments and width  $W_{np}$  of the lines, line spacing  $d$  and the number of lines  $N$ . Table 2 summarizes the optimized values used for the  $\mu$ TEGs geometry.

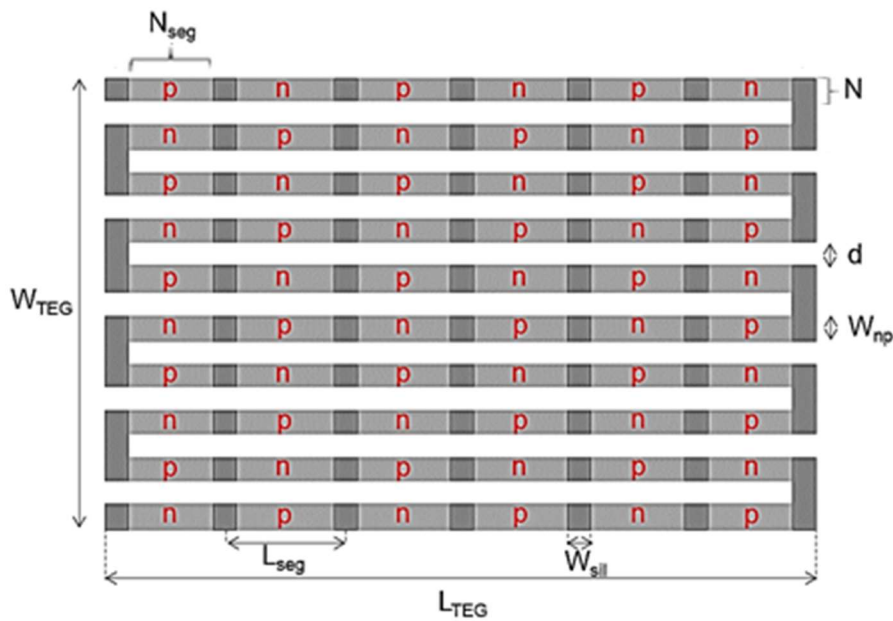


Figure 3 – Schematic top view of the main geometric parameters for a 2.5D  $\mu$ TEG.

In our case, the dimensions of hot chips are 5,8 x 5,2 mm<sup>2</sup>. Thus, the dimensions of  $\mu$ TEGs have to be very close to these values. TE lines' width  $W_{np}$  and number  $N$ , segments' length  $L_{seg}$  and number  $N_{seg}$ , and lines spacing  $d$  have been determined to reach simultaneously the highest  $V_{oc}$  and the lowest  $R_{int}$  possible.

In 2.5D configuration, equations (2) and (3) become:

$$(4) V_{oc} = (N \times N_{seg} / 2) \times S_{np} \times \Delta T = (N \times N_{seg} / 2) \times (S_p - S_n) \times \Delta T$$

$$(5) R_{int} = (N \times N_{seg} / 2) \times (\rho_n + \rho_p) \times L_{seg} / (t_{np} \times W_{np}) + R_{met} + R_c$$

with  $t_{np}$  the thickness of TE layers.

The thermoelectric properties of poly-SiGe used in  $\mu$ TEGs are 160  $\mu$ V/K and -200  $\mu$ V/K for the Seebeck coefficient,  $2.8 \cdot 10^{-5} \Omega \cdot m$  and  $2.4 \cdot 10^{-5} \Omega \cdot m$  for the electrical resistivity, and 4.7 W/m/K and 4.2 W/m/K for the thermal conductivity, for p and n-type, respectively. These values have been previously measured on dedicated structures integrated on the interposer, and are close to values from literature [10].

As shown in Table 2, optimized  $\mu$ TEGs consist of 98 lines, each line containing 128 TE segments. It results that  $\mu$ TEGs are made of 12544 TE legs (6272 junctions).

Table 2 – Optimized values used for the  $\mu$ TEGs geometry.

Main geometric parameters	Name	Values
Lines length (mm)	$L_{TEG}$	5.76
Segments number / line	$N_{seg}$	128
Segment length ( $\mu m$ )	$L_{seg}$	45
Lines number	$N$	98
Lines width / thickness ( $\mu m$ )	$W_{np} / t_{np}$	50 / 1.6
Lines spacing ( $\mu m$ )	$d$	3
Total width (mm)	$W_{TEG}$	5.19
Silicide width / thickness ( $\mu m$ )	$W_{sil} / t_{sil}$	5 / 0.04

Table 3 presents the calculated  $\mu$ TEG performances when all lines are connected in series (classical configuration) for different temperature gradients. The electrical resistance is stabilized at 183 k $\Omega$  (independent from  $\Delta T$ ). Voltages and powers increase from 11.2 V to 33.6 V and 0.17 mW to 1.5 mW, for  $\Delta T$  increasing from 5 to 15 K, respectively. As shown, voltages generated by  $\mu$ TEGs can achieve very high values (33.6 V for  $\Delta T = 15$  K). These values are too high to be compatible with classical power management unit (PMU). Indeed, PMUs are generally integrated with  $\mu$ TEGs to deliver a continuous and stable voltage at the input of power storage system (like batteries), while transmitting the maximum power generated by  $\mu$ TEGs. But such circuits accept maximum input voltage around 3 V [13]. In order to decrease the  $\mu$ TEGs output voltage while keeping the same power, the 6272 TE junctions have been grouped in 20 blocks connected in parallel: 18 blocks made from 5 lines connected in series and 2 blocks made from 4 lines connected in serie, each line containing 128 TE segments (the 6272 TE junctions have not been grouped into 20 equivalent blocks for technological issue). The calculated results are presented in the second part of Table 3. As shown, the power generated in this configuration is exactly the same than in the previous case, but resistance (458  $\Omega$ ) and voltages generated strongly decreased, from 11.2 V to 0.56 V ( $\Delta T = 5$  K) and from 33.6 V to 1.68 V ( $\Delta T = 15$  K). These voltages are now low enough (i.e. < 3V) to be compatible with PMU, or other electronic circuits.

Table 3 – Calculated  $\mu$ TEG performances for both series and parallel configurations at 300K.

<b><math>\mu</math>TEG configuration</b>	<b>Main electrical parameters</b>	<b><math>\Delta T = 5</math> K</b>	<b><math>\Delta T = 10</math> K</b>	<b><math>\Delta T = 15</math> K</b>
Series connections	$V_{oc}$ (V)	11.2	22.4	33.6
	$R_{int}$ (k $\Omega$ )	183	183	183
	$P_u$ (mW)	0.17	0.68	1.5
20 blocks connected in parallel	$V_{oc}$ (V)	0.56	1.12	1.68
	$R_{int}$ ( $\Omega$ )	458	458	458
	$P_u$ (mW)	0.17	0.68	1.5



### 3. $\mu$ TEGs process flow

The manufacturing of  $\mu$ TEGs on a silicon interposer can be divided in five main process bricks: (1) thermal insulation, (2) thermoelectrics, (3) contacts, (4) RDL (ReDistribution Layer) and (5)  $\mu$ -channels backside.

#### 3.1. Thermal insulation

The process flow describing the thermal insulation brick is given in Figure 4 below.

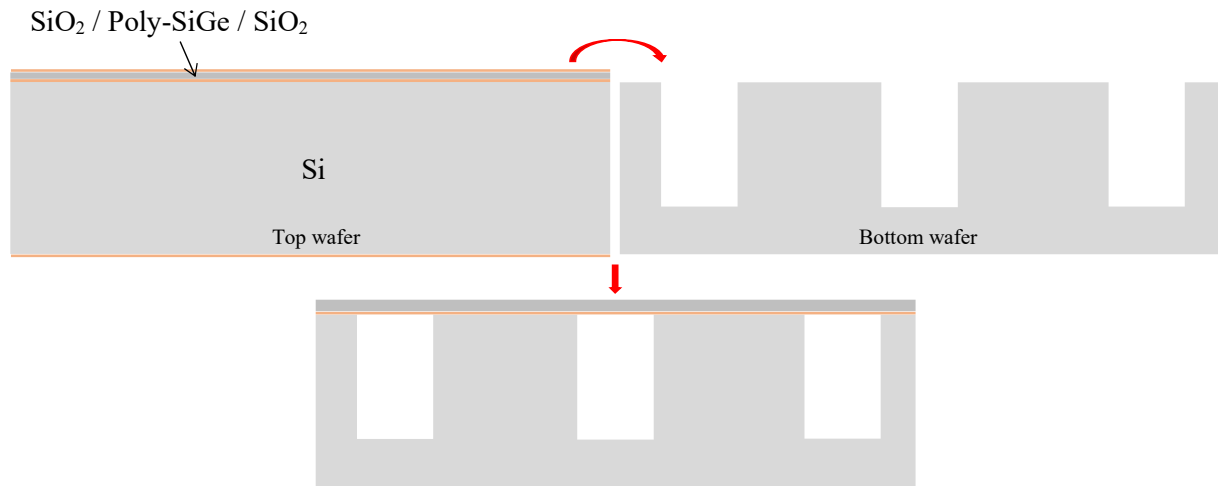


Figure 4 – Thermal insulation process brick.

The process flow on the bottom wafer begins with an oxide hard mask, then the lithography and etch of the alignment marks, and finally the lithography and etch of the insulation channels of 30  $\mu\text{m}$  width and 50  $\mu\text{m}$  depth.

The top wafer starts with the thermoelectric layer already deposited on a 500 nm oxide layer. It consists of a 2  $\mu\text{m}$  poly-SiGe layer which has been deposited by Chemical Vapor Deposition (CVD). A chemical mechanical polishing (CMP) step is realized to ensure a flat surface, which is mandatory for wafer direct bonding, decreasing the SiGe thickness to 1.6  $\mu\text{m}$ . We then add a thick oxide of 1.5  $\mu\text{m}$  on top of the thermoelectric layer and a new CMP step. Roughness is controlled with an Atomic Force Microscope (AFM) measurement, and an average roughness  $R_a$  equal to 5 nm has been obtained which corresponds to requirement to have few nanometers at the most. The direct bonding of the two wafers is then realized on an EVG bonder under vacuum followed by a annealing step at 1100  $^{\circ}\text{C}$ . The bonding quality is then monitored with acoustic scan. No major defects was detected. The bulk silicon of the top wafer is then removed by grinding and wet etch steps. The final step of this brick is the removal by wet etch of the oxide on top of the thermoelectric material.

### 3.2. Thermoelectrics

The thermoelectric brick begins with a lithography and etch of the poly-SiGe in dedicated areas in order to clear the alignment marks. Then the lithography and etch of the thermoelectrics are realized, followed by n/p-areas photolithography and implantation as described in Figure 5. The dopants, boron for p-type and phosphorous for n-type, are then activated with an annealing step at 1050 °C. The  $\mu$ TEG is a serpentine made up of segments of thermoelectric material implanted p and n covering an area of 5.19x5.76 mm<sup>2</sup>, which corresponds to the entire chiplet surface.

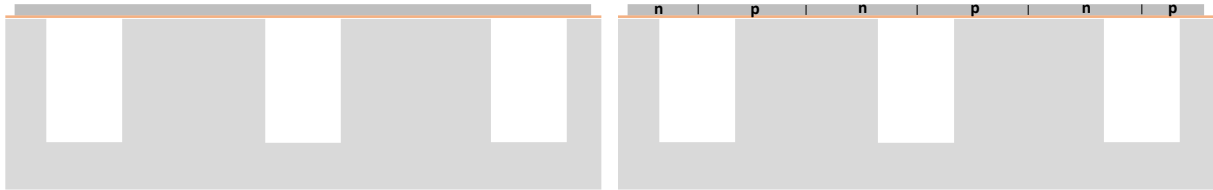


Figure 5 – Thermoelectric materials etch and implant.

### 3.3. Contacts

A TiSi<sub>2</sub> silicide is realized between n and p junctions and for the electrical contacts as shown in Figure 6 below. The corresponding process steps are first a 200 nm-thick oxide deposition followed by a lithography and etch to define the areas where the thermoelectric material will be silicided. The second step is the silicide itself: deposition of Ti/TiN of 50/10 nm, followed by a first annealing step at 700 °C and etch of the unreacted metal. A second annealing step at 850 °C is then realized to reduce the resistivity of the silicide. The last step is the deposition of a protection oxide of 500 nm and its patterning for future electrical contacts (not illustrated here).

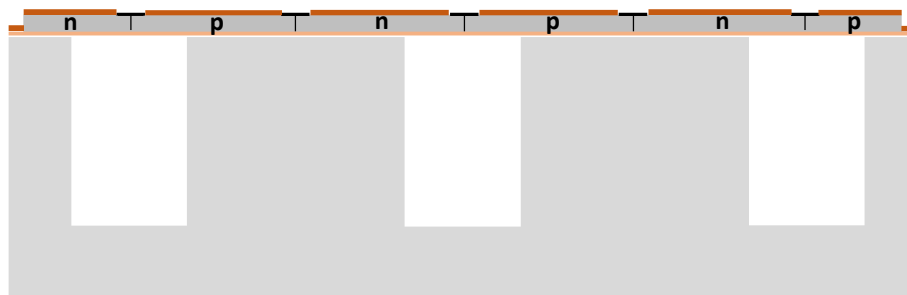


Figure 6 – Silicide and contact process brick.

### 3.4. RDL

The RDL layer serves two purposes: it ensures the electrical interconnects and routing, and it also provides a thermal path between the hot chip and the hot junctions of the  $\mu$ TEG with  $\mu$ -pillar structures as illustrated in Figure 7 below.

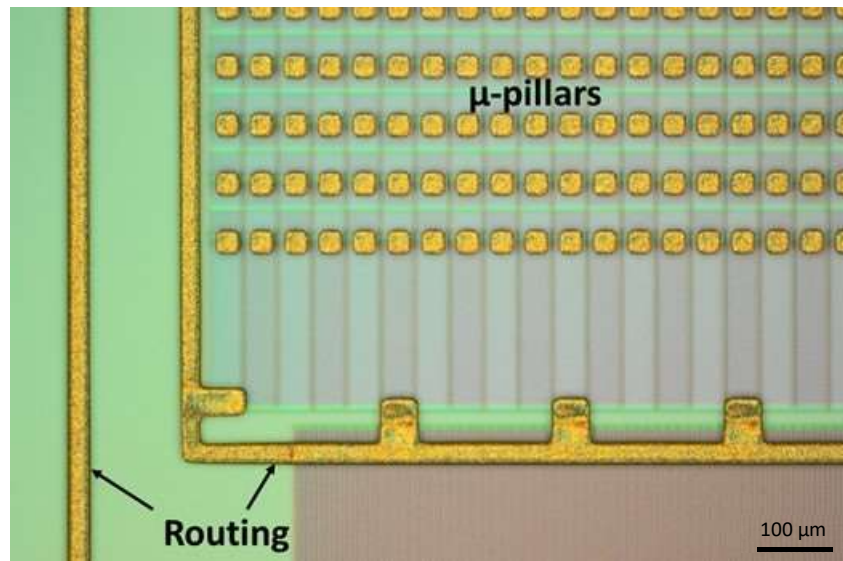


Figure 7 – RDL optical top view microscope image.

The process steps are first a seed/barrier deposition (Titanium 100 nm and Copper 400 nm), then the photolithography followed by an electrochemical deposition of 30  $\mu\text{m}$  of copper capped by 5  $\mu\text{m}$  of nickel. The seed/barrier layers are then removed by wet etch.

In Figure 7, it can also be observed the routing lines used for paralleling the 20 blocks.

Figure 8 presents a Focused Ion Beam (FIB) / Scanning Electron Microscopy (SEM) cross section pictures of a  $\mu\text{TEG}$  with  $\mu$ -pillars (a), TE segments between  $\mu$ -pillars and insulation trenches (b) and a cross-section ionic picture of one TE junction with its  $\mu$ -pillar and insulation trench (c).

### 3.5. $\mu$ -channels backside

The micro-channel fabrication process is relatively simple. In first, a temporary bonding is carried out onto a temporary carrier wafer in order to access the wafer backside as described in [14]. Then the  $\mu$ -channel fabrication consists in three steps: lithography, etch and stripping. The photolithography defines the  $\mu$ -channels length, width and spacing:  $> 5\text{ mm}$ ,  $100\text{ }\mu\text{m}$  and  $50\text{ }\mu\text{m}$  respectively. The etch process is a well-known Bosch process using alternatively an  $\text{SF}_6$  chemistry for etching and  $\text{C}_4\text{F}_8$  for passivation. It defines the  $\mu$ -channel depth:  $200\text{ }\mu\text{m}$ . Then the stripping uses a  $\text{CF}_4\text{-O}_2$  plasma followed by HF. The wafer is then debonded and singulated. The chips are then epoxy-glued onto a 3D-printed flow distributor in ABS (Acrylonitrile Butadiene Styrene) as shown in Figure 9 (a). Figure 9 (b) shows a SEM picture of the  $\mu$ -channel and the ABS flow distributor can be seen in Figure 11.

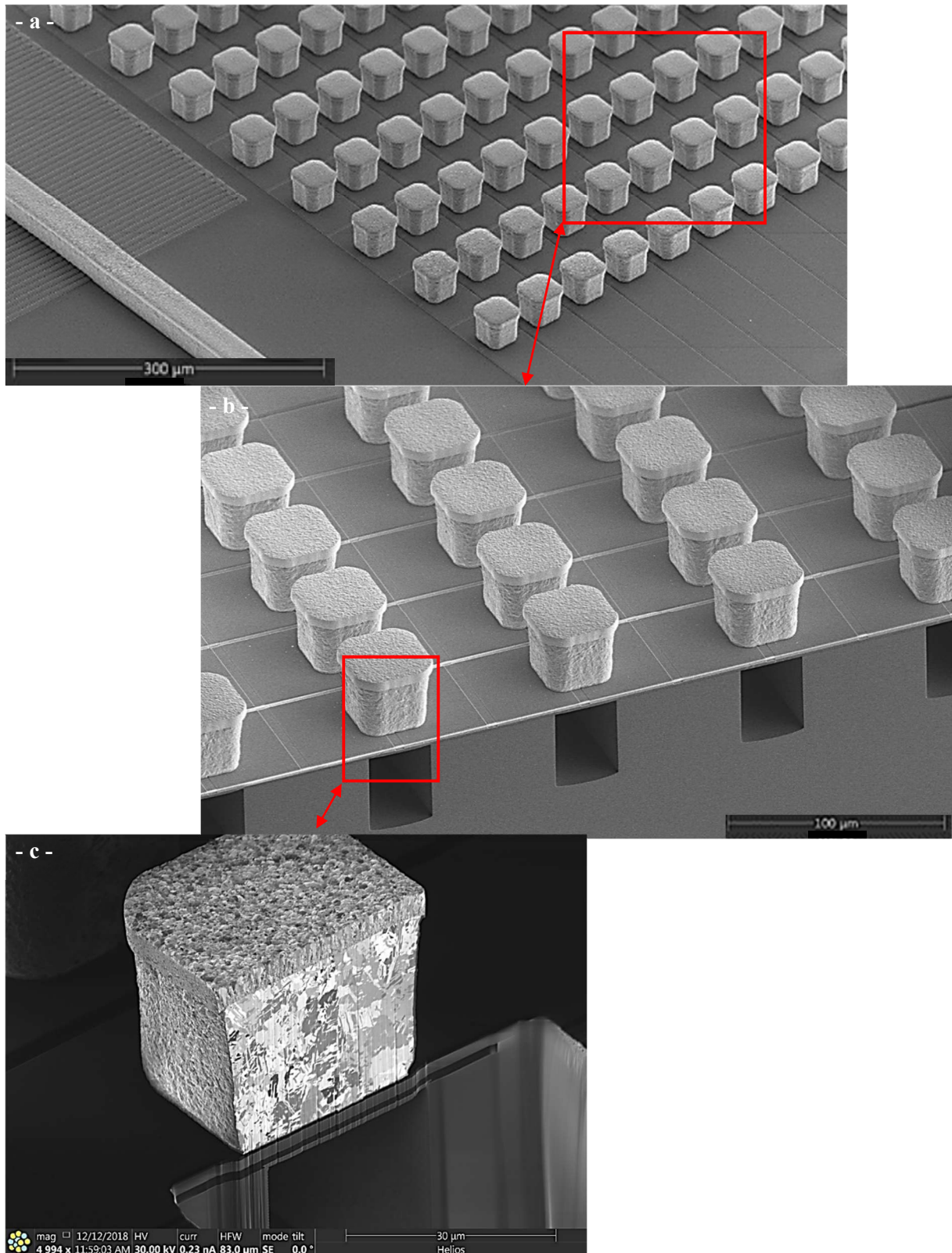


Figure 8: FIB/SEM cross section pictures of a  $\mu$ TEG with  $\mu$ -pillars (a), TE segments between  $\mu$ -pillars and insulation trenches (b) and a cross-section ionic picture of one TE junction with its  $\mu$ -pillar and insulation trench (c).

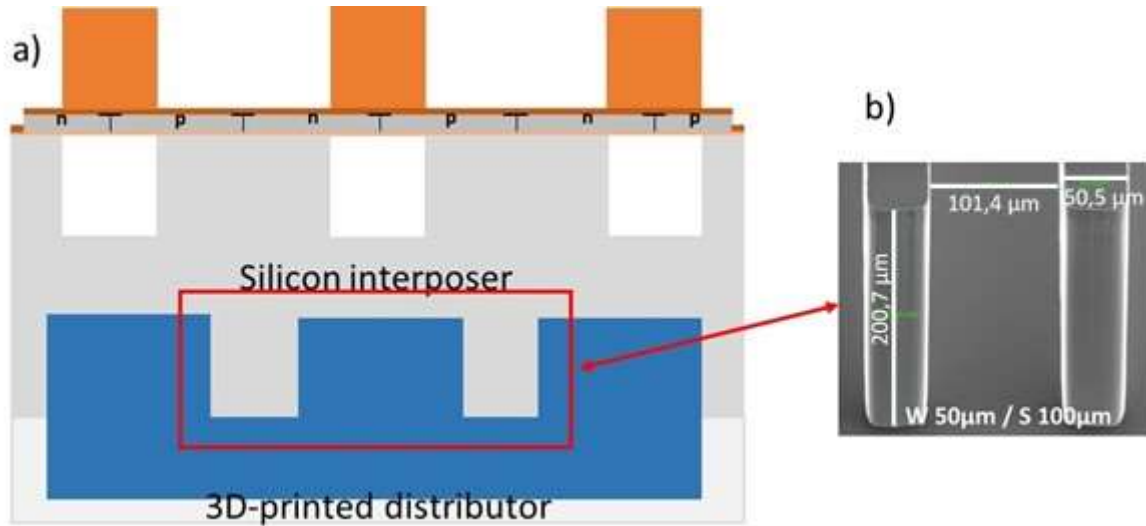


Figure 9 –  $\mu$ channels backside process brick (a) and cross-plane SEM picture of the  $\mu$ -channels (b).

#### 4. Results

The thermal test chip TTC, used as hot chip, is glued on the  $\mu$ -pillars. TTC enables an accurate control of the chip's temperature. It is made of two heaters, one central (CH) and one peripheral (PH), as shown in Figure 10. They can heat up to 15 W. More details about the TTCs are described in [15]. From the cold side, the oil temperature in microchannels has been set at 1 °C. Oil has been used instead of water to avoid condensation effect. Figure 11 illustrates the interposer with the TTC glued on the  $\mu$ TEG, the inlet and outlet used for the oil cooling connected to the ABS flow distributor and the probes used for the characterization. The total  $\mu$ TEG electrical resistance  $R_{int}$  is measured at 1.1 k $\Omega$ , corresponding to a resistance at 22 k $\Omega$  for one block. This value is higher than the simulated value (458  $\Omega$ ), probably due to contact resistances issue. Indeed, SiGe and metal electrical resistivity have been measured thanks to specific test structures (based on the 4 probes method) implemented also on the wafer. Measured values correspond to those presented previously in section 2. Considering Equation 3, it results that such  $R_{int}$  high value is due to contact resistances (not measured specifically, because no dedicated structure was implemented) and a diffusion of silicide through SiGe layer. Indeed, the electrical resistivity of poly-SiGe has been measured and is coherent with expected values. So this increase in resistance should come from contact resistances but no dedicated structure was integrated to measure them and validate this hypothesis.



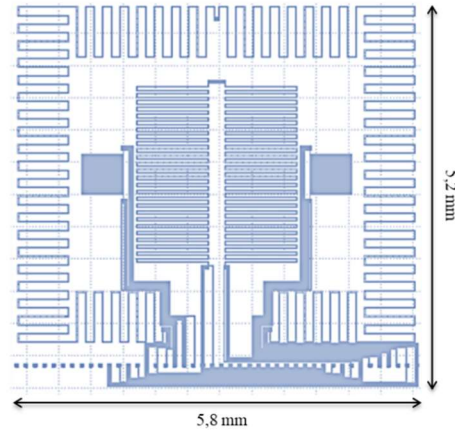


Figure 10 – Schematic layout of a thermal test chip showing the central and peripheral heaters.

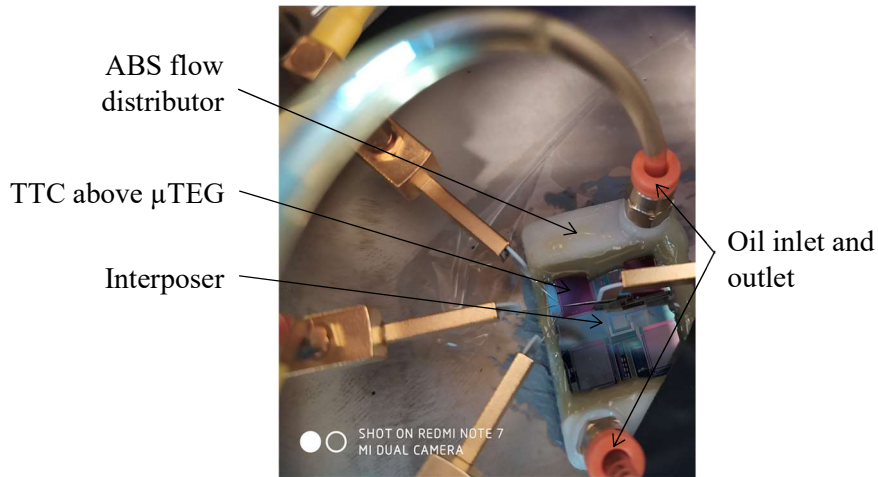


Figure 11 – Picture of the interposer showing the probes used to control the TTC and measure the  $\mu$ TEGs performances, and the inlet and outlet for the oil cooling.

Figure 12a presents the TTC heating power dependence  $P_{\text{heater}}$  of  $\mu$ TEG voltage  $V_{\text{oc}}$  when the central heater (CH) or peripheral heater (PH) is activated. Note that all experiments have been performed 5 times and that error bars represent the total variation (the central point corresponds to the average). As shown, the voltage increases logically with the heating power. Values are very low up to around 5 W then increase quite similarly for both heating cases. From these measured values, and using equation (4), corresponding temperature gradients  $\Delta T_{\mu\text{TEG}}$  across  $\mu$ TEG can be calculated. For example,  $\Delta T_{\mu\text{TEG}} = 15.5$  K, 8.9 K and 6.7 K are obtained for  $P_{\text{heater}} = 11.2$  W, 9 W and 7 W, respectively.

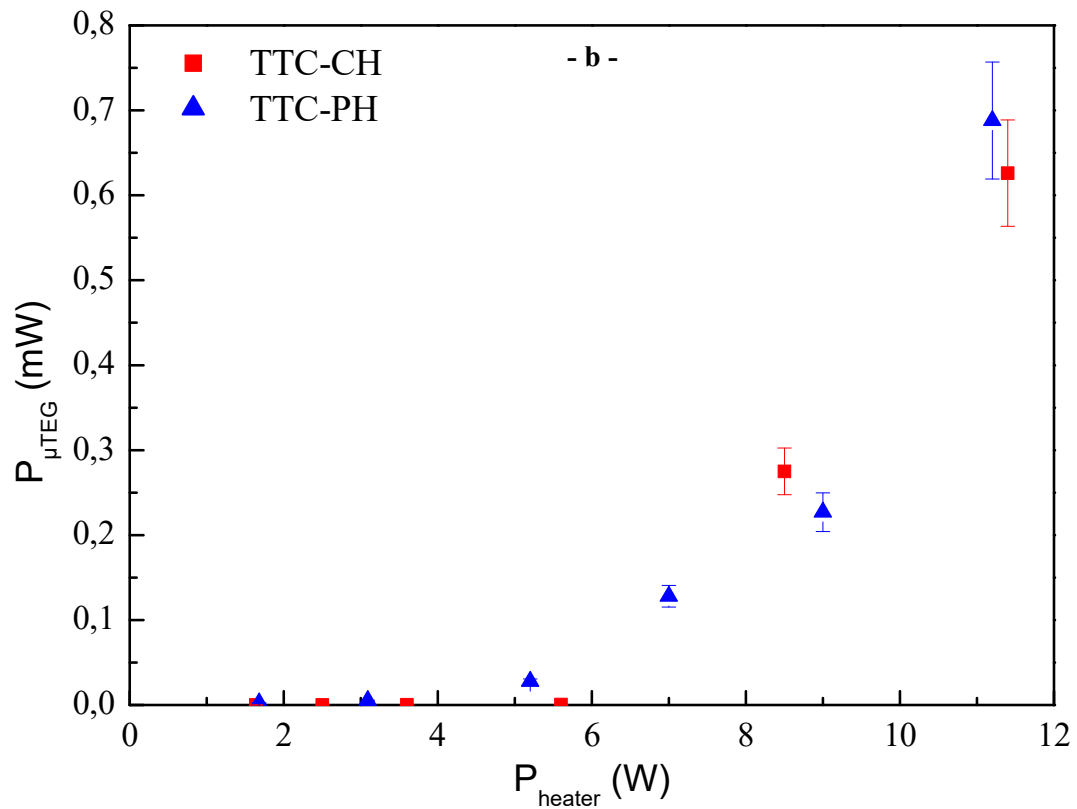
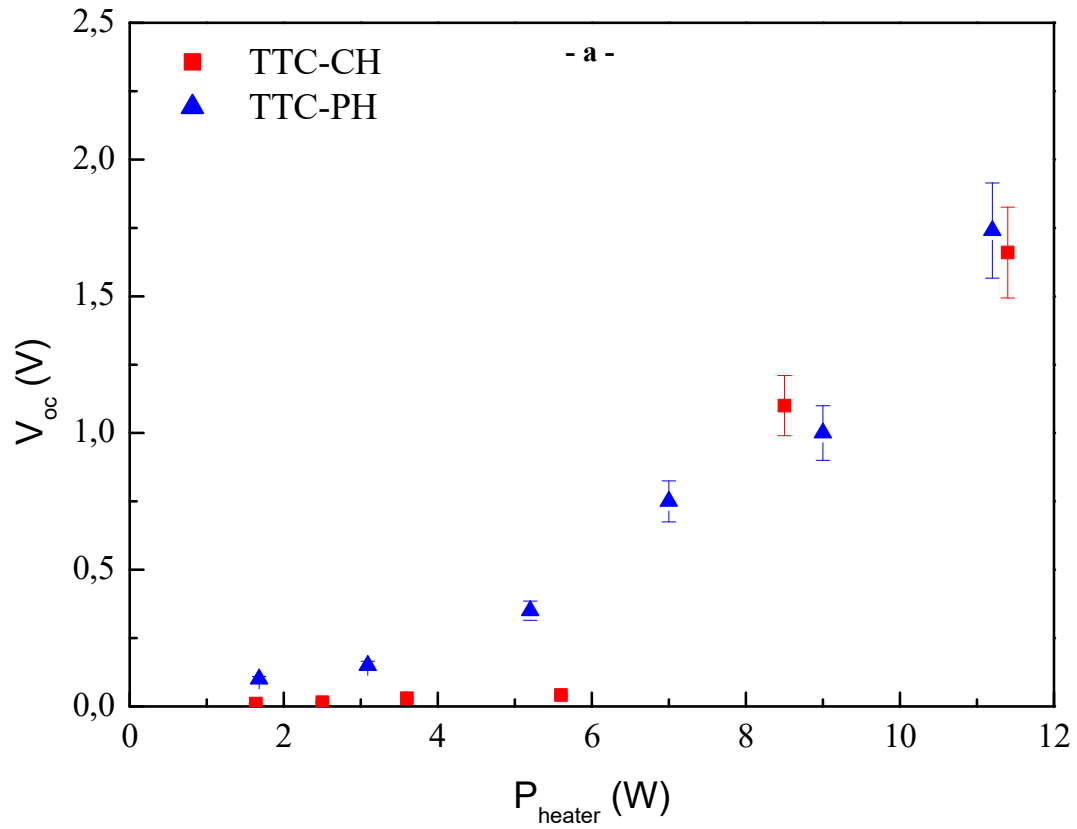


Figure 12 – TTC heating power dependence  $P_{heater}$  of  $\mu TEG$  voltage  $V_{oc}$  (a) and power  $P_{\mu TEG}$  (b) when the central heater (CH) or peripheral heater (PH) is activated.

Thanks to the parallel structure, low voltages are measured, coherent with calculated values in Table 3, and compatible with standard power management circuit (i.e.  $< 3V$ ). Figure 12b presents the TTC heating power dependence  $P_{\text{heater}}$  of  $\mu\text{TEG}$  power  $P_{\mu\text{TEG}}$  when the central heater (CH) or peripheral heater (PH) is activated. As for  $V_{\text{oc}}$ , values of  $P_{\mu\text{TEG}}$  are very low up to 5 W then increase. As shown, a power of  $680 \mu\text{W}$  is obtained for  $P_{\text{heater}}$  at 11.2 W ( $\Delta T_{\mu\text{TEG}} = 15.5 \text{ K}$ ). Even if these values are lower than expected in Table 3, due to higher electrical resistances, such power are high enough to supply sensors or load batteries. It can also be observed in Figures 12a and 12b that there is no influence of the heating part location: indeed, the heat coming from TTC central heater or peripheral heater does not modify  $\mu\text{TEG}$  performances, which is logical: only the heating power quantity, and so the temperature difference obtained between the two sides of the  $\mu\text{TEG}$  influence the electrical power generated.

Moreover, Figure 13 shows a comparison of the power density generated by the  $\mu\text{TEG}$  presented in this work with other Si-based  $\mu\text{TEGs}$  from the state-of-the-art. For information, commercial  $\text{Bi}_2\text{Te}_3$ -based  $\mu\text{TEG}$  has also been reported. As illustrated, our  $\mu\text{TEGs}$  deliver the highest power density compared to the SoA. Only  $\text{Bi}_2\text{Te}_3$ -based  $\mu\text{TEGs}$  propose logically higher power as they are made of the best TE materials at room temperature, but these devices are not CMOS compatible and cannot be integrated in IC environment.

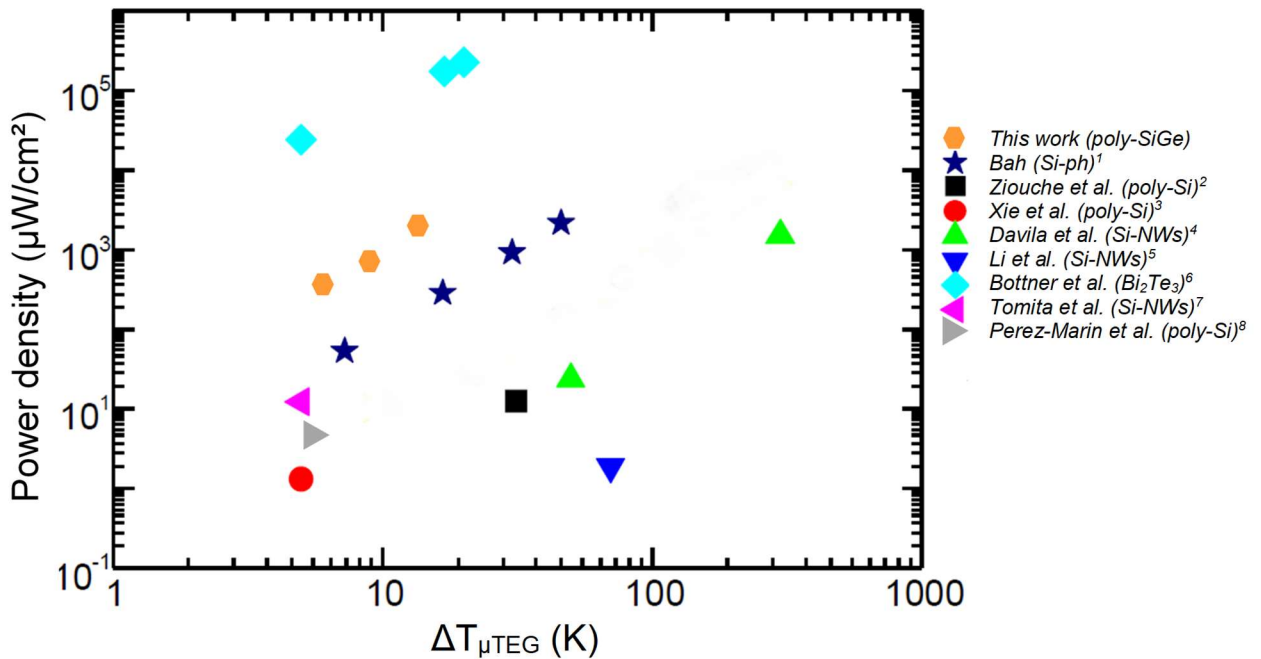


Figure 13 – Comparison of the power density generated by  $\mu\text{TEG}$  presented in this work with other Si-based  $\mu\text{TEGs}$  from the state-of-the-art.



## 5. Conclusion

We have developed high power micro-thermoelectric generators  $\mu$ TEGs fully compatible with CMOS technology.  $\mu$ TEGs have been designed with an original 2.5D architecture, combined with optimized series/parallel connections, and associated to  $\mu$ channels technology. This is the first time that this architecture has been applied to  $\mu$ TEGs in in-IC environment. Power up to 680  $\mu$ W has been measured corresponding to a temperature difference equal to 15.5 K, making these devices among the most competitive in CMOS technology. Such power is more than enough to load batteries, and so to ensure a continuous running of nearby sensors. Further work will consist in improving electrical contact resistances between TE materials and metal by studying the diffusion of silicide through SiGe. The study of other factors, such as flowing velocity and oil inlet temperature, will be also performed to evaluate  $\mu$ TEG performances in other test conditions.

Moreover, another way to improve  $\mu$ TEGs performances would consist in using thermoelectric nanostructured materials instead of bulk SiGe layers. For example, our previous studies have already shown that the use of quantum dot superlattice (QDSL) based on  $\text{TiSi}_2$  nanoparticles inside a SiGe matrix improved the performances of micro-thermoelectric sensors ( $\mu$ TES) compared to the same  $\mu$ TES integrating bulk SiGe layers [16-17]. Combination of improved contact resistances with such high-performance nanostructured materials will enable these  $\mu$ TEGs to increase still more their performances.

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