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# Characterisation of IGBTs in Soft Commutation Mode for Medium Frequency Transformer Application in Railway Traction 

Jérémy.Martin* **, Philippe.Ladoux**, Bertrand.Chauchat*<br>*ALSTOM Transport, Power Electronics Associated Research Laboratory (PEARL), Rue du dr Guinier BP 465601 Semeac Cedex, (France)<br>** Université de Toulouse, LAPLACE-INPT, 2 rue Charles Camichel 31000 Toulouse, (France)


#### Abstract

Nowadays, the typical railway traction chain, that operates under AC catenaries, includes a bulky and heavy transformer. In order to reduce the weight and the size of the input transformer, a medium frequency topology, which involves soft commutation mode for the switches, is proposed. At this effect, for the characterization of high voltage components in soft commutation mode, a specific test bench is built in the PEARL. In this paper, experimental characterisation results are given for 6.5 kV IGBTs in Dual-Thyristor mode. The snubber capacitors provide a significant reduction in turn-off energy and a switching frequency of several kHz is then possible.


## 1. Introduction

### 1.1. Today's Railway Traction Chain

In a typical railway traction chain (Fig.1), the power converter topology includes a transformer which operates at low frequency $(50 \mathrm{~Hz}$ or $16 \mathrm{~Hz}^{2 / 3}$ ). This transformer, because of its low frequency operation, is bulky and heavy, which is particularly problematic in the case of multiple units train (loss of room for the passengers). Beyond this problem, the cost reduction of the transformer and the research of an higher efficiency are also important goals.


Fig. 1. Typical railway traction chain
A few years ago, several converter topologies including medium frequency transformers were proposed [1], [2], [3], [4], [5], [6], [7], [8]. Among these topologies, we have selected a Phase Controlled Multilevel Converter, based On Dual Structure Associations.

## 1.2. $A C-D C$ Conversion based on Phase Controlled Multilevel Converter

The principle of this phase controlled multilevel converter, which involves a soft commutation mode for the switches, was introduced by the LEEI in the 90's [9], [10], [11].
As it is shown in figure 2 , the AC-DC converter is composed of N stages connected in series on the catenary side and connected in parallel on the DC-Bus. Each stage includes a medium frequency transformer, a four quadrants current source inverter, a voltage source inverter and a DC-Bus capacitor.


Fig. 2. Phase controlled multilevel converter
On one hand, minimizing the number of serial stages requires high voltage components. On the other hand, reducing the size and the weight of the transformer, requires a high switching frequency. To succeed in this project, transformer technologies have to be investigated, especially the properties of the magnetic materials (induc-
tion level, losses, cost, specific power) and the high voltage isolation techniques. From the power converter point of view, reaching a high frequency with acceptable switching losses implies soft commutations. Finally, the choice of this frequency will be a trade off between switching losses, cooling system size and transformer size. One should note that the decrease of the weight and volume of the transformer will be more significant in the case of $15 \mathrm{kV}-16 \mathrm{~Hz}^{2 / 3}$ catenaries.

### 1.3. AC-DC Conversion



Fig. 3. Soft commutated converter with medium frequency stage

One stage of the power converter is depicted in figure 3. Whatever the sign of the input current $\mathrm{i}_{\mathrm{in}}$, the four quadrants current source inverter provides a medium frequency alternating current ( $\mathrm{i}_{\text {ac }}= \pm \mathrm{i}_{\text {in }}$ ) which enables soft commutation conditions on the voltage source inverter (Fig.4). Reciprocally, the voltage source inverter provides a medium frequency alternating voltage ( $\mathrm{V}_{\mathrm{ac}}= \pm \mathrm{E}$ ) which enables soft commutation conditions on the four quadrants current source inverter.


Fig. 4. Waveforms in the medium frequency stage ( $\mathrm{f}_{\mathrm{sw}}=5 \mathrm{kHz}$ )

### 1.4. Topology Sizing

As described in figure 2, the converter is composed of N stages. Each stage provides an output voltage $\mathrm{V}_{\mathrm{oN}}$ depending on the Thyristor turnon delay angle. $\mathrm{V}_{\text {ot }}$ is the total output voltage. Llink is the link inductor between the catenary and the converter. In the switching period, the stages are $\pi / \mathrm{N}$ interleaved and, thanks to a control loop, a quasi-sinusoidal current, $\mathrm{i}_{\mathrm{in}}$, is drawn in phase with the catenary voltage $\mathrm{V}_{\text {cat }}$.
Thus, according to equation (1), the vector diagram at the fundamental frequency, presented in figure 5 shows that the total voltage $\mathrm{V}_{\text {ot }}$ must be higher than the catenary voltage $\mathrm{V}_{\text {cat }}$.
$\underline{V_{\text {ot }}}=\underline{V_{\text {cat }}}-j . L \omega . \underline{l_{\text {in }}}$


Fig. 5. Vector diagram at the fundamental frequency

As it is shown by equation (2), the minimum number of stages depends on the DC-Bus voltage E . That's why high voltage components are required to limit this number.

$$
\begin{equation*}
N>\frac{V_{c a t} \sqrt{2}}{E} \tag{2}
\end{equation*}
$$

In the case of a 2 MW power level, the input current $i_{i n}$ equals $80 A_{\text {RMs }}$ for a 25 kV catenary and equals $135 \mathrm{~A}_{\text {RMS }}$ for a 15 kV catenary.
Considering a unity turns ratio for the transformers, Table 1 shows the minimum number of stages required in the case of $25 \mathrm{kV}-50 \mathrm{~Hz}$ and $15 \mathrm{kV}-16 \mathrm{~Hz}{ }^{2 / 3}$ catenaries.

| Semiconductor Blocking Voltage | DC-BUS | Number of stages 25kV/50Hz AC lines $29 \mathrm{kV}_{\text {rms }} / 50 \mathrm{~Hz}^{*}$ | Number of stages $15 \mathrm{kV} / 16 \mathrm{~Hz}^{2 / 3} \mathrm{AC}$ lines $17,5 \mathrm{kV}_{\mathrm{rms}} / 16 \mathrm{~Hz}^{2 / 3 *}$ |
| :---: | :---: | :---: | :---: |
| 3.3 kV | 1.8 kV | 23 | 14 |
| 4.5 kV | 2.5 kV | 17 | 10 |
| 6.5 kV | 3.6kV | 12 | 7 |
| 10 kV | 5.5kV | 8 | 5 |

Table. 1. Minimum number of stages versus catenary voltage and semiconductor blocking voltage

For the moment, the use of 6.5 kV IGBT requires twelve stages in the considered $25 \mathrm{kV}-50 \mathrm{~Hz}$ application [12]. Simulation waveforms with PSIM software for a number of twelve stages are given in figure 6.


Fig. 6. Simulation results
The converter provides a multilevel waveform with an apparent switching frequency of $2 . \mathrm{N} . \mathrm{f}_{\mathrm{sw}}$ and a number of levels equal to $\mathrm{N}+1$. As consequence, the value of the link inductor $L_{\text {link }}$ can be strongly decreased.

## 2. Test Bench for $\mathbf{6 . 5 k V}$ Devices

### 2.1. Test Bench Description

A test bench, presented in Figure 7, is installed at the PEARL. It enables the study of one elementary converter. The voltage source inverter is composed of switches with spontaneous turn-on at zero voltage crossing and controlled turn-off (Dual-Thyristor Mode) [11]. The current source inverter is composed of switches with spontaneous turn-off at zero current crossing and controlled turn-on (Thyristor Mode).


Fig. 7. Elementary converter test bench
The test bench is designed to provide real conditions of operation: maximum input voltage: 5 kV , maximum output current: 120 A .
Capacitors Cs are used to adjust the dv/dt on controlled turn-off switches. The inductor $\mathrm{L}_{\mathrm{ac}}$ limits the di/dt on controlled turn-on switches. These
non dissipative snubbers allow a strong decrease of the switching losses.
In this paper, only the voltage source inverter operation is under consideration (Fig.8).


Fig. 8. Voltage Source Inverter under test

### 2.2. Characterisation of 6.5 kV IGBT in Dual-Thyristor Mode.



Fig. 9. Characterisation Circuit
Preliminary tests were performed on one inverter leg loaded by a LC circuit (Fig.9). In this circuit the current level is fixed by selecting the switching frequency and the DC-Bus Voltage level. For measuring the temperature rise during operation, thermocouples are placed under the base plates of the devices.
In the circuit, the inverter leg operates with a duty cycle of 0.5 and the switching frequency is always above the resonant frequency of the LC load. Thus, the current has a symmetrical triangular waveform (Fig.10) and there is a direct relation between the switching frequency, the DCBus voltage ( E ) and the current ripple $\Delta \mathrm{i}_{\mathrm{L}}$ :

$$
\begin{equation*}
\Delta i_{L}=\frac{E}{4 . L \cdot f_{s w}} \tag{3}
\end{equation*}
$$



Fig. 10. General experimental waveforms on the inverter leg

To get a Dual-Thyristor mode for the reverse conducting IGBTs, a sufficient dead time is introduced between the control signals of K1 and K2.

The figures hereafter (Fig.11, Fig. 12 and Fig. 13) show the experimental waveforms at the IGBT turn-off and for different values of the snubber capacitors. In any case, the frequency is adjusted to switch a current of 120A under 3.6 kV DC-Bus voltage.

Using snubbers, directly connected in parallel with the IGBTs, reduces strongly the turn-off energy and modify the collector current waveform particularly during the tail phase. Because of this current tail, the turn-off energy cannot be totally canceled by the snubbers.


Fig. 11. IGBT snubberless turn-off


Fig. 12. IGBT turn-off with $C_{s}=120 n F$


Fig. 13. IGBT turn-off with $C_{s}=330 \mathrm{nF}$
Figure 14 and figure 15 show the turn-off energy versus the commutated current and for a 3.6 kV DC voltage. The snubbers allow a significant reduction of the losses (by a factor 6 in the case of the higher capacitor value).


Fig. 14. IGBT Turn-off versus switched current.
Between figure 14 and figure 15, the value of the turn-off gate resistor $\mathrm{Rg}_{\text {off }}$ has been reduced from $75 \Omega$ to $36 \Omega$. As expected, the turn-off energy is slightly reduced in the snubberless operation. In other cases, the decrease of $\mathrm{Rg}_{\text {off }}$ value is not effective.


Fig. 15. IGBT Turn-off versus switched current $\mathrm{Rg}=\mathrm{Rg}_{\text {off }} / 2$

Figure 16 shows the influence of the snubber capacitor value on the tail phase. In this figure, the current waveforms during turn-off are surimposed. It should be notice that the more the current tail begins at a high current level, the lower it lasts. The quantity of electricity corresponding to the current tail was calculated using the equation (4). Figure 17 reveals that the electric charge depends on the commutated current level and the snubber capacitor value.
$q=\int_{t 1}^{t 2} i . d t$


Fig. 16. Tail current waveforms versus capacitor value


Fig. 17. Electric charge versus turn-off current and snubber capacitor value

## 3. Losses Calculations for the Considered Structure

### 3.1. Calculations of Switching Losses in the Voltage Source Inverter

The expression of losses in the voltage source inverter switches is given by the following expression which is demonstrated in the paper [12].
$\mathrm{P}_{\mathrm{sw}-\mathrm{T}-\mathrm{vsl}}=\mathrm{f}_{\mathrm{sw}} \cdot \frac{\mathrm{E}}{\mathrm{V}_{\mathrm{tef}}} \cdot\left[\frac{(\hat{\mathrm{l}})^{2}}{2} \cdot \mathrm{a}_{\mathrm{off}}+\frac{2 \hat{\mathrm{l}}}{\pi} \cdot \mathrm{b}_{\mathrm{off}}+\mathrm{c}_{\mathrm{off}}\right]$
In this expression, $\mathrm{f}_{\mathrm{sw}}$ is the switching frequency and $\mathrm{V}_{\text {ref }}$ is the test voltage given in the semiconductor datasheet.
The coefficients a, b, c are extracted by interpolation of the curves presented in figure 14.The following graph shows the evolution of losses versus the switching frequency considering $\mathrm{i}_{\mathrm{in}}$ as sinusoidal equal to $80 \mathrm{~A}_{\mathrm{rms}}$ and a DC-Bus set to 3600V. Conduction losses are considered for a modulation ratio equals to 0.83 .


Fig. 18. Total IGBT module losses Vs switching frequency

Considering 1 kW as the maximum dissipated power by module, a very high switching frequency can be achieved. However, when the input current $i_{i n}$ is crossing zero, the natural commutation in Dual-Thyristor mode is impossible. The turn-on has to be forced and the energy stored in the snubber capacitors is dissipated by the switch, which is not desirable regarding the reliability of the switches.
A way to avoid this problem is to design a transformer with a sufficient magnetizing current. This solution leads to additional conduction and switching losses and limits the modulation ratio of the converter. Finally, the choice of $\mathrm{C}_{\mathrm{s}}$ will be a compromise between the turn-off $\mathrm{dv} / \mathrm{dt}$, the modulation ratio of the converter, the magnetizing current level and the switching losses.

For example, a 5 kHz switching frequency, the use of 120nF snubber capacitors with a magnetizing current of $20 \mathrm{~A}_{\mathrm{pk}}$, limits the modulation ratio at 0.83 . In this case, compared to the ideal case (Fig.18) conduction losses are increased by 14,5\% and switching losses are increased by $17,5 \%$ which corresponds to a total losses of 488W per IGBT module. This relatively low dissipated power is acceptable regarding the cooling system and the converter efficiency. Nevertheless, 14 stages are necessary to operate with a 29 kV RMS catenary voltage.

## 4. Conclusion

Table 2 shows the results of the study that compares two prototypes of 270kVA medium frequency transformers which are designed for the $25 \mathrm{kV}-50 \mathrm{~Hz}$ application.

|  | Prototype 1 | Prototype 2 |
| :---: | :---: | :---: |
| Frequency (kHz) | 5 | 10 |
| Apparent Power <br> (kVA) | 270 | 270 |
| Weight (kg) | 44 | 25 |

Table. 2. Medium Frequency Transformers
The total weight for the copper and the magnetic core are indicated in Table 2. Thus, by considering a 2MW power level and a switching frequency of 5 kHz , the structure needs a total transformer weight of $14 * 44 \mathrm{~kg}=616 \mathrm{~kg}$.

Since a 2MW low frequency transformer weight is 1224 kg , the total weight for copper and magnetic core will be reduced by 2 . This result is not clearly significant and to improve the gain on the transformer weight, it is necessary to increase the switching frequency and reduce the capacitor value. Another compromise has to be found.

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