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ADVANCED 3D DESIGN AND TECHNOLOGIES FOR 3-LAYER SMART IMAGER

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***Abstract*—CMOS Imagers have adopted 3D integration using Back-Side Illumination (BSI) technology, with 2 CMOS layers assembled using Wafer-to-Wafer and advanced Hybrid Bonding technology. Targeting innovative AI and Machine Learning application, for offering AI processing at the edge within the image sensor itself, this paper presents some new 3D design and technology solutions in order to build a 3-layer Smart Imager. The hybrid bonding technology for assembly of multi wafers with a capability below 1 µm pitch is shown as well as Through Silicon Via (TSV) of 2 µm pitch compatible with hybrid bonding. To offer Design Technology Co-Optimization (DTCO) capabilities, a Place & Route methodology is proposed with the associated PDKIT to benefit of fine pitch interconnects.**

I. INTRODUCTION

CMOS Imagers have adopted 3D integration using Back-Side Illumination (BSI) technology, with 2 layers assembled using Wafer-to-Wafer and Hybrid Bonding technologies. These technologies are widely adopted currently by the industry for current CMOS imager sensors of the consumer market, allowing form factor reduction, and the heterogeneous assembly of optimized CMOS pixel technology onto a layer dedicated to imager logic acquisition and data processing [1, 5]. There is a need to pursue the integration of more features within the image sensor. With advanced Machine Learning (ML) application and associated demands from the market, it is proposed to embed AI processing at the "edge", in that case within the image sensor itself [2]. Such edge AI capability in the CMOS sensor itself is expected to reduce the system latency, increase the user privacy, and increase the energy efficiency. To tackle such Smart Imager architecture, it is proposed to integrate in 3D a third silicon layer within the imager, offering larger computing capability and memory capacity leading to larger ML applications.

Current hybrid-bonding technologies for imagers are currently limited to two layers [1], while advanced hybrid bonding and TSVs integration was presented but not yet closely assembled togather[3,4]. Regarding the design for 3D pitches below 1µm, available CAD tools are not able to address it efficiently, current design solutions consists in tricking existing 2D place & route tools but still requiring separate placements [7].

In order to tackle such 3-layer Smart Imager system, the following contributions are proposed in this paper:

- The hybrid bonding for 3D assembly of 3 wafers, with fine pitch interconnects capability below 1 µm,
- High Density TSVs (HD-TSV), with 2 µm pitch, allowing communication between the two bottom layers, and compatible with hybrid bonding,
- A 3D Place and Route design flow with associated Process Design Kit (PDKIT) to offer Design Technology Co-Optimization (DTCO) capabilities.

II. ADVANCED 3D TECHNOLOGY

A. *Hybrid Bonding technology for 3D Assembly of multi Wafers*

Three wafers stacking including two successive hybrid bonding operations is considered from a morphological point of view. The performance of 3D vertical links will then be assessed with electrical measurement of vertical interconnects crossing both interfaces of a 3 layer Test Vehicle (TV). Each TV wafer includes multiple metal layers. Results of wafer-to-wafer alignment is the key point to achieved fine pitch CMOS Image Sensor [5]. Here, vector maps are analyzed separately for both hybrid bonding interfaces of different TV. Fig 1a displays a misalignment vector map after bonding of the first hybrid bonding operation where the maximum misalignment is 350nm [3σ]. An average value of 100nm is recorded and well compatible with a hybrid bonding pitch less than 1.5µm [5].

After bonding and annealing, the quality of interface over the complete wafer surface was assessed with homogeneous dark contrast of acoustic microscopy scan (SAM) (Fig 1b). Then bonding strength was sufficient to support mechanical grinding and provide wafer thinning less than 10µm with a total thickness variation (TTV) < 2µm [6]. In addition, TEM cross section shows local hybrid bonding interface for a quasi-perfect aligned die (Fig. 1c).The comparison with the second hybrid bonding alignment is summarized in Fig 1d. In this simplified TV version, hybrid bonding is done after a preliminary direct bonding using SiO_2-SiO_2 interface and followed with a wafer thinning downto 10µm. The maximum misalignment at wafer edge is slightly increased up to 1µm and is characterized with a run out mechanism.

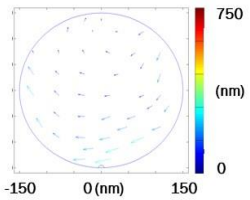

Fig. 1a. Misalignment vector map for the first hybrid bonding sequence of the TV.

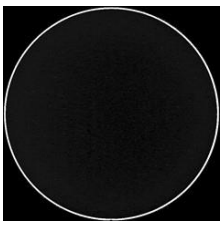

Fig. 1b. Scanning acoustic microscopy picture after hybrid bonding and annealing of TV

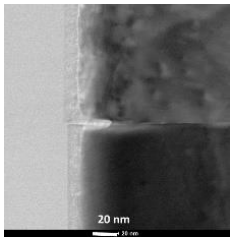

Fig. 1c. TEM cross section of a hybrid bonding interface with a quasi-perfect alignment in the X direction

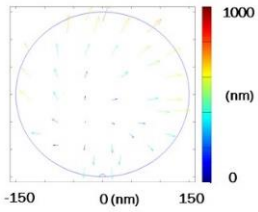

Fig. 1d Misalignment vector map for the second hybrid bonding sequence after 10 µm wafer thinning.

B. *High Density TSV (HD TSV)*

Through-Silicon-Vias (TSV) are mandatory to connect the different levels of a system made of more than two layers stacked in a wafer-to-wafer flow. In a 3-layer smart imager, they can be used either for all connections (e.g. 1+2 and 2+3) like in [1], or only between two layers (e.g. 1+2) in combination with hybrid bonding to connect 2+3 in a face-to-face assembly [6]. Towards this latter integration scheme, we developed copper TSV in a via-last approach, through a thin wafer bonded on top of a thick wafer with metal patterns embedded. In order to meet the need for interconnections density, the diameter of our TSV was 1µm with a pitch of 2µm. They were 10µm-deep in a first iteration considering the thinning capability at that time, but current work is done on thinner HD-TSV. The realization of TSV with an aspect ratio of 10:1 is challenging in terms of patterning because the low etch rates at the bottom of deep and narrow cavities require thick masks and/or highly selective processes. Deposition is challenging due to the dielectric material (silicon oxide) lined on the sidewalls, and must be conformal enough to provide sufficient substrate isolation. A 30nm-thick dielectric layer was measured at the bottom of the TSV after the etch-back process (contact opening on the pad). The metals (Ti/TiN + Cu used as a barrier/seed stack) must also be conformal enough to allow a void-free copper plating in a bottom-up filling regime.

The fine pitch also constitutes a challenge in terms of lithography since the overlay between the TSV and the pads underneath must remain below the design rules defined for this enclosure. By applying a novel alignment method using specific marks, we reached an overlay below 50nm (|mean|+3σ) after correction. Figure 2 shows a daisy chain between both sides of the thin wafer, with a zoom on the upper (resp. lower) part of the TSV to highlight the alignment and the contact with the top (resp. bottom) line. The electrical yield was close to 100% on structures with 100 000 TSV. The resistance measured on Kelvin structures was between 800mΩ and 1Ω per TSV with a dispersion that can be imputed to CD and silicon thickness variations across wafers.

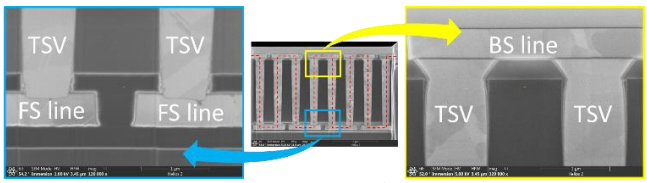

Figure 2 : cross-sectional SEM micrograph of a daisy chain with 1x10µm Cu TSV at a pitch of 2µm.

III. 3D Design Methodology for High Density TSV

A. *PDKIT*

In order to enable digital place and route capabilities and especially handling timing-driven routing across HD-TSVs for the two bottom tier digital layer of the 3-layer Smart Imager, we customized the technology files and design environment. Each tier is based on a 28nm FDSOI technology using a 10 metal layers (ML) Back-End Of Line (BEOL) option. The proposed PDKIT consists in modelling a 20 ML structure co-integrating the two tiers. The HD-TSV itself is modelled in the technology LEF file (.lef), as a regular via, with a pitch of 2 µm, while the BEOL parasitics are modelled using the Interconnect Technology Format (.itf).

Creating a 20ML BEOL stack (10ML on 10ML with HD-TSV) as shown Figure 3 requires duplication of the whole bottom-tier 10ML stack with rename and properties update of all top-tier layers to avoid duplicates. Standard-cells library and technology file description (LEF format) are duplicated and renamed to differentiate bottom-tier std-cells from top-tier std-cells and associated layer mappings.

Fig 3. BEOL stack description with HD-TSV, and example of standard cells

B. *Place & Route Design Methodology*

For 3D technology with relaxed pitch (> 10µm) or interposers, standard CAD tools are implementing the 3D circuits separately with multiple netlists. With aggressive pitches, in order to fully optimize cross-layer timing and 3D pin assignment, it is mandatory to implement the multi-layer design in a single session using a unique design database.

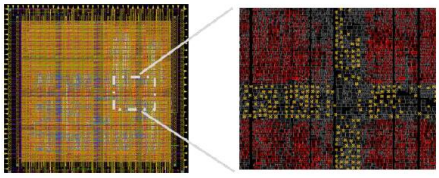
Fig 4 : Placed & Routed design with HD-TSV (*yellow*) in reserved zones

Based on a Memory-on-Logic design methodology [8], and using the above 20 ML PDKIT integrating HD-TSV, a design flow is proposed for any Logic-on-Logic design. With a pre-partitioned netlist with bottom and top standard cells, a 2 layer floorplan with power mesh is created with open spaces for future TSV localization, an iterative placement is then performed to place and refine iteratively the bottom and top standard-cells using LEF format "cover" attributes, while finally a single routing is performed to route all metal layers: top, bottom and HD-TSV created as regular vias (Fig.4).

IV. Conclusion

Advanced technology bricks were presented: 3D hybrid bonding technology for multi-wafers assembly and 2µm pitch HD-TSV, with the associated Place & Route design flow and PDKIT. Future works consist in the assembly of a 3 layers Test Vehicule including the HD-TSV and designing the 3-layer Smart Imager architecture.

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