

# Known Good Dies (KGD) strategies compatible with Direct Hybrid bonding

E. Bourjot<sup>a</sup>, P. Stewart<sup>a</sup>, C. Castan<sup>a</sup>, L. Sanchez<sup>a</sup>, G. Mauguen<sup>a</sup>, Y. Exbrayat<sup>a</sup>, V. Balan<sup>a</sup>, N. Bresson<sup>a</sup>, A. Jouve<sup>a</sup>, F. Fournel<sup>a</sup>, F. Servant<sup>a</sup>, N. Raynaud<sup>c</sup>, P. Metzger<sup>c</sup>, S. Cheramy<sup>a</sup>, P. Vivet<sup>b</sup>

<sup>a</sup> Univ. Grenoble Alpes, CEA, LETI, 17 rue des Martyrs, 38000 Grenoble, France

<sup>b</sup> Univ. Grenoble Alpes, CEA, LIST, 17 rue des Martyrs, 38000 Grenoble, France

<sup>c</sup> SET Corporation, 131 impasse bartheudet, 74490 Saint-Jeoire

Die-To-Wafer (D2W) direct hybrid bonding process, using copper/oxide mix interfaces, is identified by major microelectronic industrials as essential for the success of future logic & memory stacks, thanks to heterogeneous integration with low interconnection pitch and known good die (KGD) selection capabilities [1]. The current interconnection pitch demonstrated in LETI is 10 $\mu$ m [2]. 5 $\mu$ m is aimed by the end of 2021. Testing chips at wafer level before assembling adds significant value to Chip-to-Wafer approach by increasing yield of final product [3]. However, it rises integration challenges to make the test compatible with the direct bonding afterwards. At which level the test can be performed ? Which solutions can be proposed to enable direct bonding after testing ? This paper presents the complete solution developed at CEA-Leti of D2W direct bonding using KGD selection before stacking.

The first part of this presentation will review the D2W direct hybrid bonding as developed in CEA-Leti [4]. Direct hybrid bonding is based on the direct bonding of Cu/SiO<sub>2</sub> surfaces. After an additional annealing, the bonding interface is sealed and Cu interconnections are rebuilt. The D2W hybrid bonding integration flow is depicted in Fig 1. First of all, two damascene bonding levels are created directly after the last interconnection level on both bottom wafer and top dies at wafer scale. The cross section in Fig.2 shows the damascene levels stack after CMP with 10 $\mu$ m bonding pitch. Main challenges for a good bonding quality lie in the realization of post CMP treatments without bonding surface degradation nor particle contamination. Thus, special care was carried out for dicing post treatment, die handling and stacking to limit defect on the bonding surface. Finally, dies were directly stacked with SET NEO HB stacking system [5] on surface prepared bottom wafer. Extremely good bonding quality was observed by scanning acoustic microscopy (SAM) as shown in Fig. 3 and lead to electrical yields higher than 75% (Fig.4). D2W hybrid bonding was successfully demonstrated.

In the second part, latest KGD development applied to D2W direct bonding will be presented. The great advantage of D2W in regards with W2W is the capability to select dies with good electrical performances before stacking (Fig. 5). KGD scheme strongly improves the final yield of the 3D system as demonstrated for conventional 3D stacking [1], [3]. However, KGD rises challenges of compatibility with high surface flatness and roughness requirement of direct bonding [6]. Indeed, electrical testing creates high topographies on testing pad which disable direct bonding. In this paper, several integration strategies are discussed to render KGD compatible with hybrid bonding. After the characterization of topography induced by test probes (Fig.6), post test planarization processes were developed to minimize defect. Finally, CEA-Leti successfully demonstrated a D2W hybrid bonding with KGD strategy, as shown by the SAM of bonded tested dies in Fig.7. These results demonstrate the feasibility of including a KGD strategy into the D2W direct bonding flow, which is a mandatory requirement to make D2W HB transferred into high volume manufacturing. Main conclusion of this presentation is the demonstration to KGD integration flow adapted to D2W direct hybrid bonding.

**Acknowledgements:** This work was partially funded thanks to the French national program "Programme d'investissements d'Avenir, IRT Nanoelec" ANR-10-AIRT-05".

## References:

- [1] Garrou, Bower, et Ramm, « Handbook of 3D Integration », *Wiley Online Library*.
- [2] A. Jouve *et al.*, « Die to Wafer Direct Hybrid Bonding Demonstration with High Alignment Accuracy and Electrical Yields », in *2019 International 3D Systems Integration Conference (3DIC)*, oct. 2019, p. 1-7
- [3] D. Gitlin *et al.*, « Generalized cost model for 3D systems », in *2017 IEEE SOI-3D-S3S Conference*, 2017, p. 1–3.
- [4] A. Jouve *et al.*, « Die to wafer direct hybrid bonding demonstration with high alignment accuracy and electrical yields ». *3DIC*, 2019.
- [5] P. Metzger *et al.*, « New flip-chip bonder dedicated to direct bonding for production environment », *Proc 2018 7th Electron. Syst.-Integr. Technol. Conf. ESTC*.
- [6] E. Bourjot *et al.*, « Towards a Complete Direct Hybrid Bonding D2W Integration Flow: Known-Good-Dies and Die Planarization Modules Development », in *2019 International 3D Systems Integration Conference (3DIC)*, oct. 2019, p. 1-5

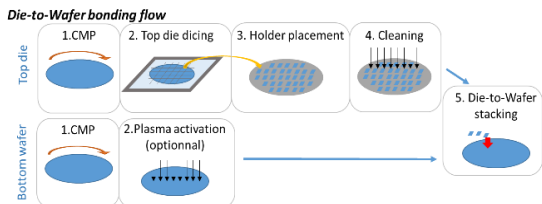


Figure 1: Simplified process flow for Die-to-Wafer direct hybrid bonding.

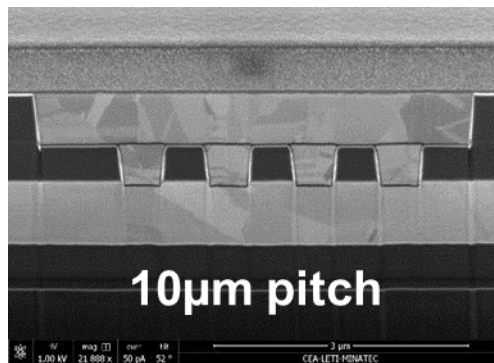


Figure 2: X-section of an electrical test vehicle after damascene & CMP processing with 10µm interconnection pitch.

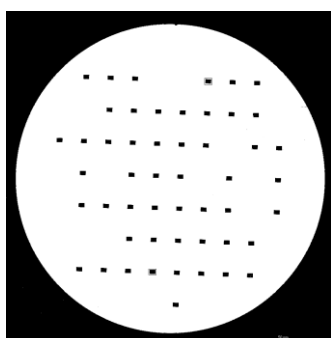


Figure 3: Bonding interface quality evaluation at wafer-level inspection: 90% of the dies present defect free interfaces.

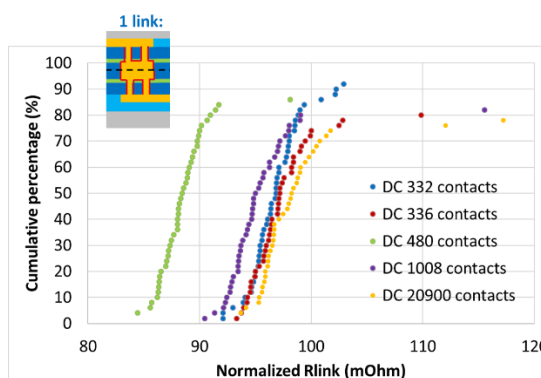


Figure 4: Cumulative percentage of 1 daisy-chain element resistance (Rlink) for different daisy-chains length.

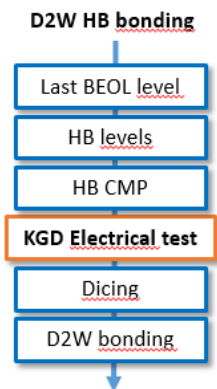


Figure 5: Integration of KGD module in the D2W hybrid bonding flow.

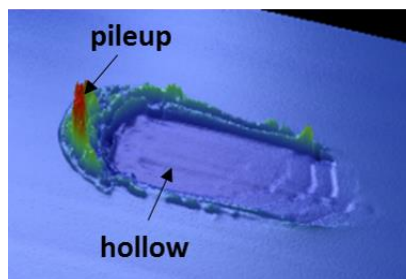


Figure 6: Optical interferometry of one probe mark on Cu, 3µm high topography measured.

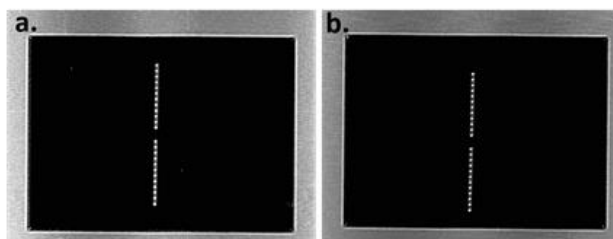


Figure 7: Acoustic scan of D2W bonding with (a) no test and (b) 50µm overdrive test + CMP : no difference is noticed.