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3D Design-for-Test Solution for Chiplet-based Active Interposer architecture

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Introduction

In the context of high performance computing, the integration of more computing capabilities with generic cores or dedicated accelerators for AI application is raising more and more challenges. Due to the increasing costs of advanced nodes and the difficulties of shrinking analog and circuit IOs, alternative architecture solutions to single die are becoming mainstream. Chiplet-based systems using 3D technologies enable modular and scalable architecture [1]. The current *passive* interposer solutions – silicon passive interposers [2] or organic substrates [3] – brings clear cost reduction by smart technology partitioning [4] and using the so-called Know Good Die (KGD) approach [5]. Nevertheless, they still lack flexible efficient long-distance communications, smooth integration of chiplets with incompatible interfaces, and easy integration of less-scalable analog functions, such as power management and system IOs.

In [6][7], we have presented the first CMOS *active* interposer, integrating i) power management without any external components, ii) distributed interconnects enabling any chiplet-to-chiplet communication, iii) system infrastructure, circuit IOs, and the associated Design-for-Test solution. The INTACT circuit prototype (fig 1) integrates 6 chiplets in FDSOI 28nm technology, which are 3D-stacked onto an active interposer in 65nm process, offering a total of 96 computing cores (Fig. 1).

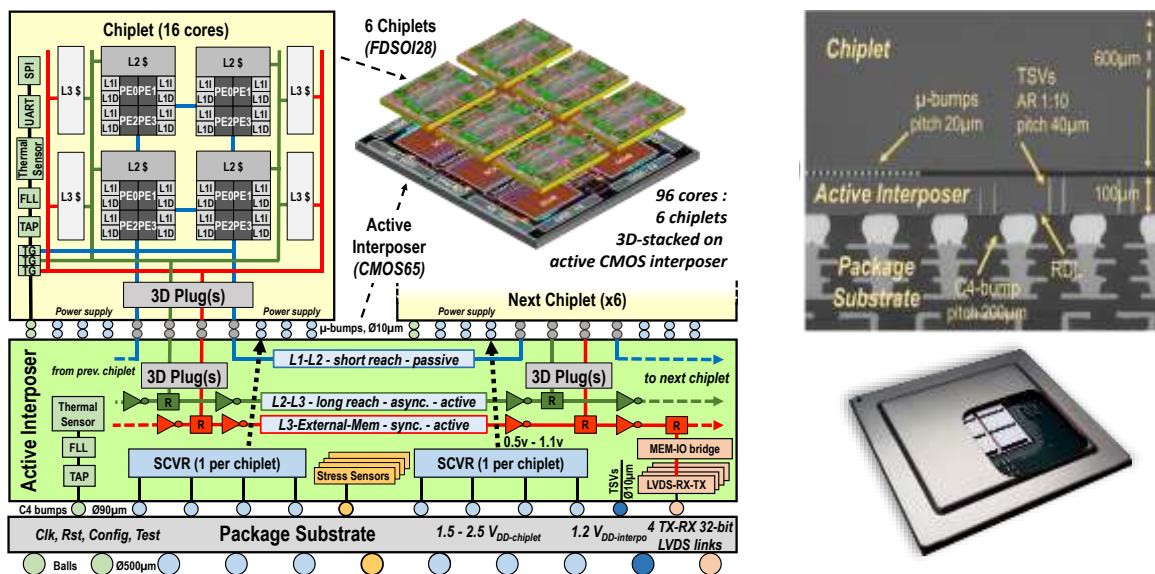


Fig. 1. INTACT overall circuit architecture, 3D cross section, and package [6]

In terms of complexity: 150,000 3D connections are performed using μ -bumps (20 μ m pitch) between the chiplets and the active interposer, with 20,000 connections for system communication, using the various 3D-communication interfaces, called 3D-Plugs, and 120,000 connections for power supplies using the integrated voltage regulators (SCVRs); while 14,000 TSVs are implemented for power supplies and off chip communication.

Testability Challenges

With such 3D active interposer, as for passive interposers, testability is raising various challenges. First, it is required to ensure Know-Good-Die (KGD) sorting to achieve high system yield [8]. This implies that the 3D test architecture must enable Electrical Wafer Sorting (EWS) test of the chiplet and the interposer (pre-bond test, before 3D assembly), and final test (post-bond, after 3D assembly in the circuit package). Moreover, due to fine pitch μ -bumps, reduced test access is observed, μ -bumps cannot be directly probed in test mode. This implies to include additional IO pads, which are only used for test purpose, and not in functional mode (see Fig. Fig. 2).

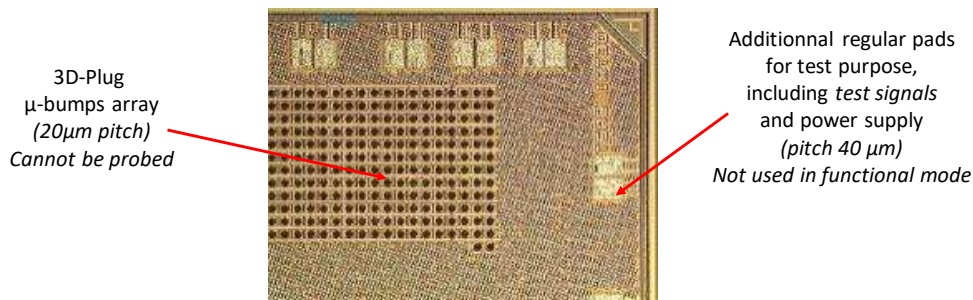


Fig. 2. Chiplet layout (zoom), with 3D-Plug interface and additional test pads

Finally, with 3D technologies, additional defects may be encountered, such as μ-bumps misalignments, TSV pinhole, shorts, etc. which lead to specific care for testing the 3D objects and interfaces. Another concern is also regarding the Automatic Test Pattern Generation (ATPG) engineering effort, where easy re-targeting of test patterns from pre-bond test to post-bond test should be proposed to reduce test development efforts.

Numerous researchers have addressed specific test solutions for 3D defaults [9][10], for testing generic 3D architectures using die wrappers and elevators [11], and for testing 2.5D passive interposers [12]. A standardization initiative on 3D testability has emerged with the P1838 proposal, with recent outcomes and results [13]. Nevertheless, no work addressed initially the testability of active interposers.

3D Design-for-Test Architecture

Within the INTACT architecture, the test of the 3D system must address the test of all the following elements: i) the regular standard-cell based logic, ii) all memories using BIST engines and Repair, iii) the distributed 3D interconnects and IOs: 3D connections of active links and passive links, which are implemented by micro-bumps, and finally iv) the regular package IO pads for off-chip communication through the TSVs.

In order to test the Active Interposer and its associated chiplets, the proposed 3D Design-for-Test architecture (Fig. 3) is based on the two following main Test Access Mechanisms (TAMs), as proposed earlier in [14]:

- A JTAG IEEE1687 hierarchical and configurable chain, accessed by a primary JTAG TAP port, for testing all the interconnects and memories, based on the concept of “chiplet footprint”,
- A Full Scan logic network using compression logic, for reduction of test time and of number of test IOs.

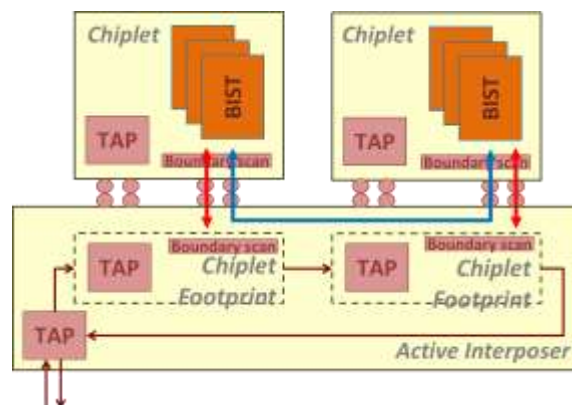


Fig. 3. Concept of “chiplet footprint” : a chain of TAPs for testing individual chiplets within the active interposer [14]

By using JTAG IEEE 1687, the JTAG chain is hierarchical and fully configurable: the JTAG chain provides dynamic access to any embedded test engines. The active interposer JTAG chain is designed similarly to a chain of TAPs on a PCB board. It is composed of “chiplet footprints”, which provide either access to the above 3D-stacked chiplet or to the next chiplet interface, and which are chained serially. The JTAG network is used to test and control the 3D active links, the 3D passive links, the off-chip interfaces, and the embedded test engines, such as the memory BISTs. This TAP chain presents a reduced area impact and reduced 3D pin count.

The Full Scan logic network offers efficient and parallel full scan test of the whole 3D system logic. In order to reduce the number of 3D parallel ports, compression logic is used in both the chiplets and the active interposer, with a classical tradeoff (shift time/pin count). Independent scan paths are used between the chiplets and the active interposer, to facilitate the test architecture integration.

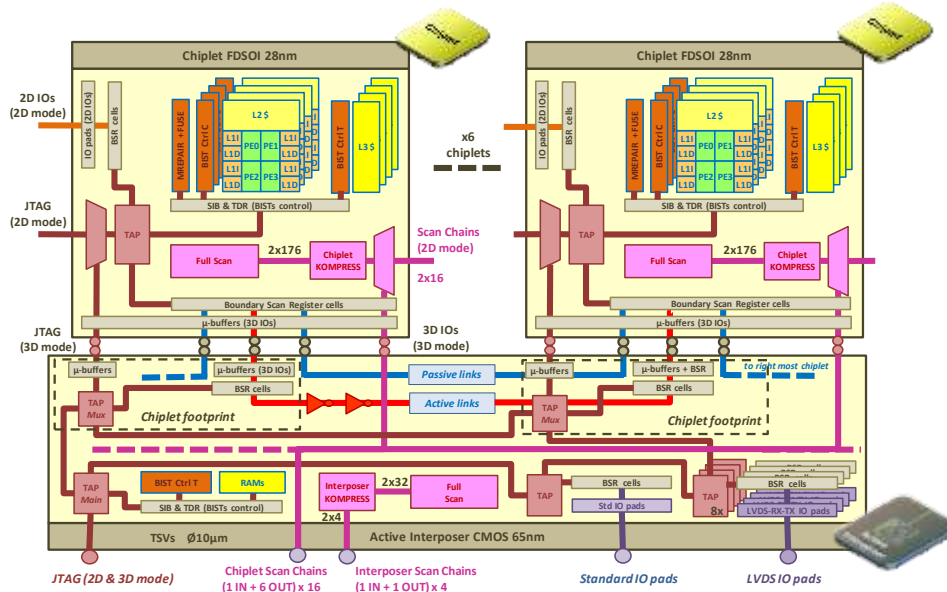


Fig. 4. 3D Design-for-Test architecture for INTACT : detailed implementation

Test CAD Flow and Test coverage

The proposed 3D Design-for-Test architecture has been designed and inserted using Tessent™ tools from Mentor, a Siemens Business [15]. By using IJTAG and IEEE1687, high level languages such as “Instrument Connectivity Language” (ICL) and “Procedural Description Language” (PDL) are provided and enable to handle the complexity of such a system. In particular, it is possible to fully-automate the test pattern generation of Memory BIST engines, from ATPG at chiplet level to ATPG of the same patterns within the full 3D system, enabling so-called test pattern retargeting. As presented in Table I, full testability is achieved for all logic, 3D interconnects and regular package IOs, and memory BIST engines, before 3D assembly and after 3D assembly.

TABLE I: INTACT DESIGN-FOR-TEST RESULTS

DFT access	Active Interposer 65nm	Chiplet FDSOI 28nm	Full 3D System
Full Scan	32 scan chains, 4 after compression, #faults 5.7M, Test cov. ~60%**, 1318 patterns	182 scan chains, 16 after compression, #faults 21.5M, Test cov. 97,06%, 1790 patterns	#faults 134.8M Test cov. 95.5%
IJTAG + Interco. Boundary Scan	All IO pads <i>pre-bond</i> 2D pads (826) 3D IO (13 548) 81 patterns	All IO pads <i>pre-bond</i> 2D pads (249) 3D IO (2 258) 68 patterns	3D IO pads <i>post-bond</i> (13 548) 27 patterns
BIST & Repair	#BIST: 1 12 patterns / BIST	#BIST: 5 20 patterns / BIST	#BIST: 31 612 patterns

** Limited test coverage is reported by the tool within the interposer, this is due to the asynchronous NoC that can be tested using a dedicated test solution not reported here

Using the proposed DFT architecture & generated test patterns, the full system was tested using an Automated Test Equipment (ATE):

- The 28nm chiplet has been tested at wafer level using a dedicated probe card, with a binning strategy.
- The active interposer has not been tested at wafer level, supposing the maturity of the 65nm technology and its high yield due to its low complexity. Nevertheless, its standalone DFT and dedicated IO test pads on the front face were initially planned and designed as mentioned above.
- The full INTACT circuit, after 3D assembly and packaging, has been tested within a dedicated package socket.

Conclusions and Perspectives

3D integration and Active Interposer open the way towards efficient integration of large-scale chiplet-based computing systems. Such scheme can be applied for integration of similar chiplets as presented with the INTACT circuit in this paper, but also for smooth integration of heterogeneous computing chiplets [16].

Regarding testability and DFT, the proposed solution allows to perform KGD sorting of both the chiplet and the active interposer, with final test of the full system. The DFT solution is based on existing DFT standard (IEEE1687 and compressed full scan) and tools. A chain of TAP, called chiplet footprint, offers a modular and scalable DFT for any number of chiplets within the active interposer. The solution has been successfully implemented and tested using the Mentor Graphics Tessent tool suite.

Regarding chiplet integration, it is currently complex to integrate chiplets from different sources, due to missing standards, even if strong standardization initiative are on-going [17, 18]. With passive interposers, wire-only interposers prevent the integration of chiplets using incompatible protocols, while active interposer enable to bridge them easily by ad-hoc logic within the active interposer. This has been proposed for instance as a generic connectivity, as adopted by zGLUE Inc. [16].

Regarding 3D technology, the technologies are still evolving to provide more advanced chiplet integration, with reduced pitches and improved thermo-mechanical behavior. Hybrid bonding technology initially devoted for Wafer to Wafer are also appearing for chip2wafer assembly, with reduced pitches (10 μ m pitch as of today) [20], while also proposing adequate solutions for KGD sorting on 3D copper pad physical interfaces [21].

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