



Key low temperature processes for a silicon-based 3D sequential integration

Xavier Garros, Perrine Batude, Claire Fenouillet-Beranger, Laurent Brunet, Camila Calvacante, Tadeu Mota Frutuoso, Remy Gassilloud, Mickael Ribotta, Laurent Brevard, Valerie Lapras, et al.

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Xavier Garros, Perrine Batude, Claire Fenouillet-Beranger, Laurent Brunet, Camila Calvacante, et al.. Key low temperature processes for a silicon-based 3D sequential integration. 2022 IEEE SYMPOSIUM ON VLSI TECHNOLOGY AND CIRCUITS, Jun 2022, Honolulu, United States. cea-03727300

HAL Id: cea-03727300

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Submitted on 11 Oct 2022

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Key low temperature processes for a silicon-based 3D sequential integration

X. Garros, P. Batude, C. Fenouillet-Beranger, L. Brunet, C. Cavalcante*, T. Mota Frutuoso, R. Gassilloud, M. Ribotta, L. Brevard, V. Lapras, F. Andrieu, F. Gaillard

CEA, Leti, Minatec Campus, & Grenoble Alpes University

**Now with IMEC*

Outline

- Introduction to 3D sequential integration
- Max thermal budget for the Top Tier
- Key process steps for a low temperature high performance 3DSi CMOS integration
 - Gate oxide
 - Junction engineering
 - Other processes required for RF applications
- Conclusion

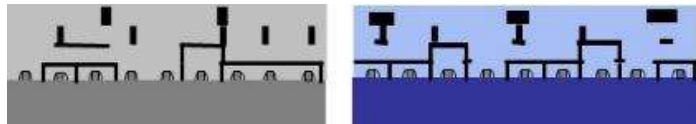
Outline

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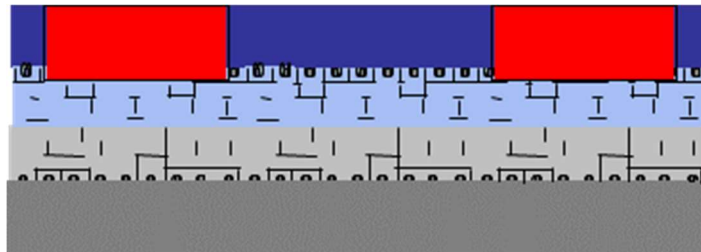
3D parallel integration $\neq$ 3D sequential integration

Parallel integration (e.g: TSV, Hybrid bonding, Cu pillar, etc..)

1/ Wafers processed separately (in parallel)



2/ Stacking and contacting

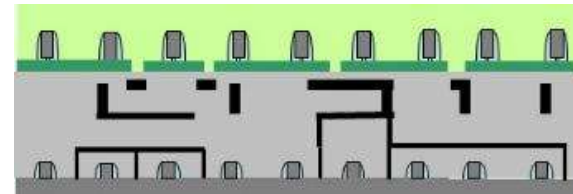


Sequential integration

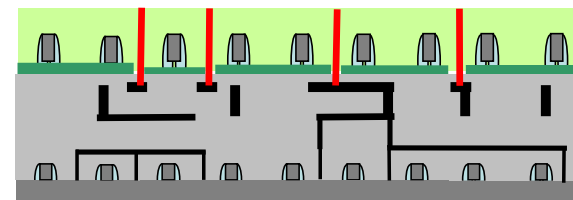
1/ Bottom Layer process



2/ Top layer process



3/ 3D contact formation

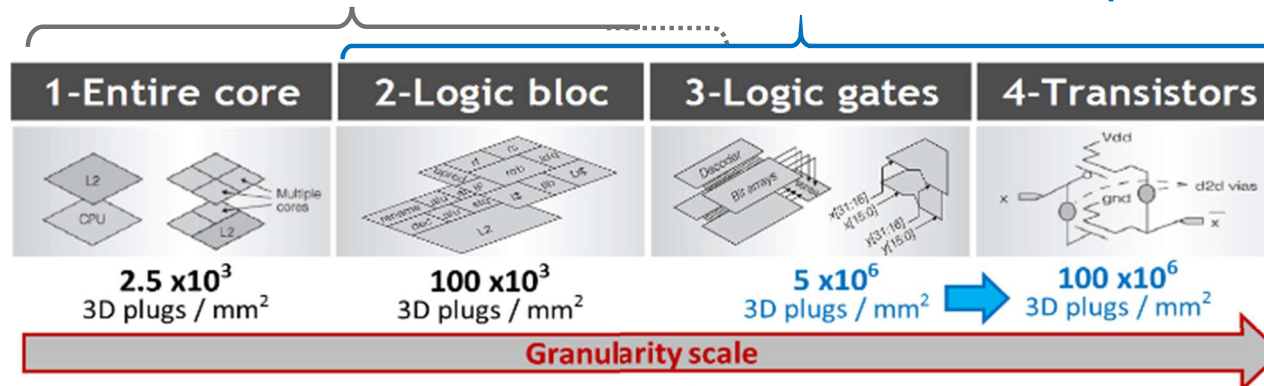


Parallel integration: stacked MOSFETs processed separately
Sequential integration: stacked MOSFETs processed sequentially

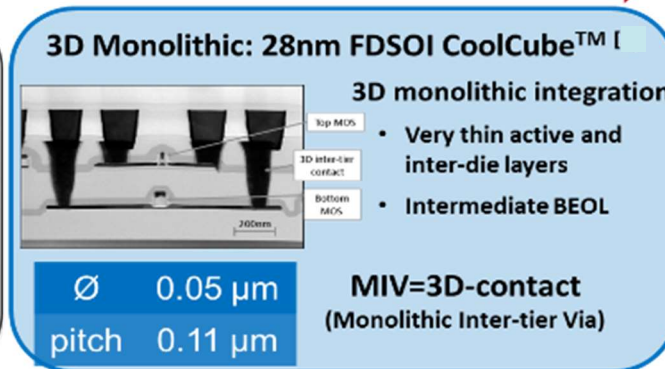
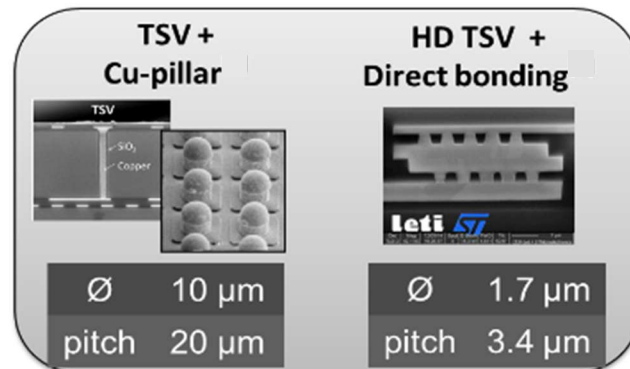
3D contact pitch and design granularities

Global Interconnect: 3D parallel

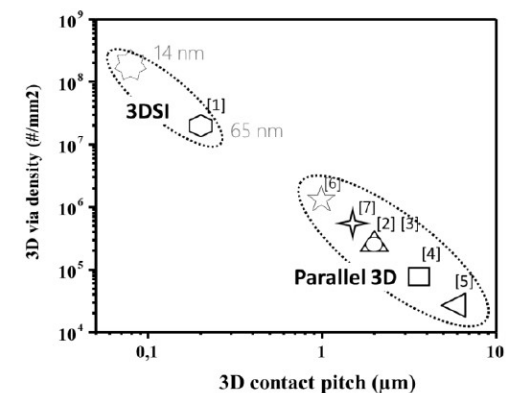
Local Interconnect: 3D sequential



TSV &
Cu-Pillar
> 10 μm



High 3D contact density:
 2×10^7 via/mm² demonstrated¹



3DSi
Pitch ~100nm

Partitioning a circuit in separated stacked levels can be made with different block sizes
3D sequential enables partitioning with all granularities

3DSI applications



High Performance

CMOS over CMOS Wirelength reduction
Boost CMOS (N/P) with alternative channel materials

More Moore



Energy Efficiency

Near memory computing/
In memory computing



Smart Sensors

e.g. miniaturized sensor arrays

More than Moore

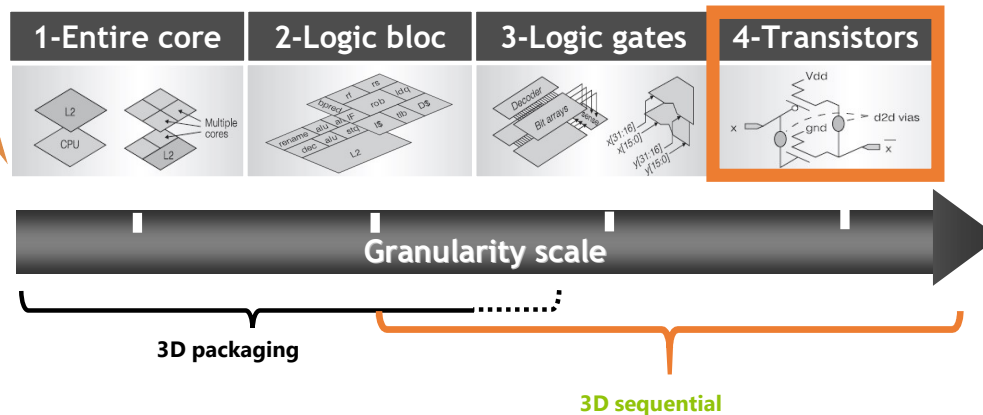
3DSI applications



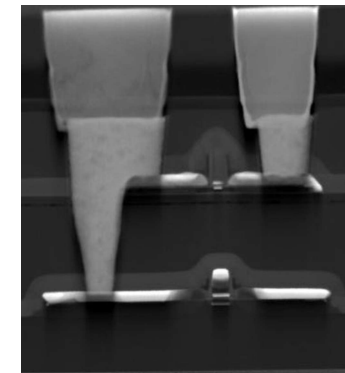
High Performance & Scaling for Computing

CMOS straddled on two stacked channels to address the ultimate pitch

More Moore



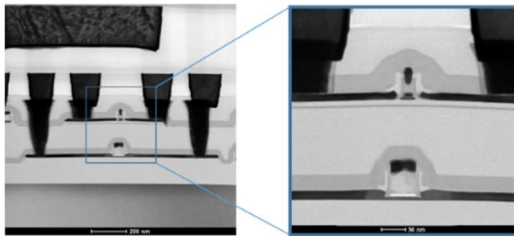
Digital/Digital



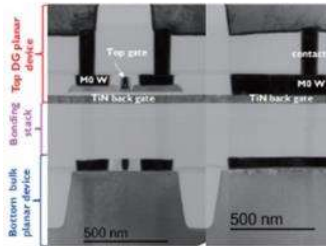
X. Garros et al., IEDM 2019 (Leti)

CMOS straddled on two levels

3D Seq → ultimate performance boost



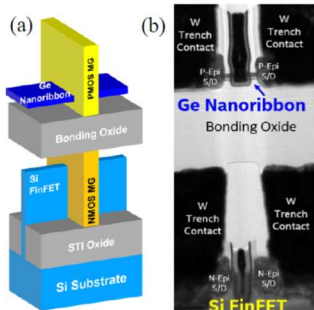
L. Brunet et al., VLSI'16 (Leti)



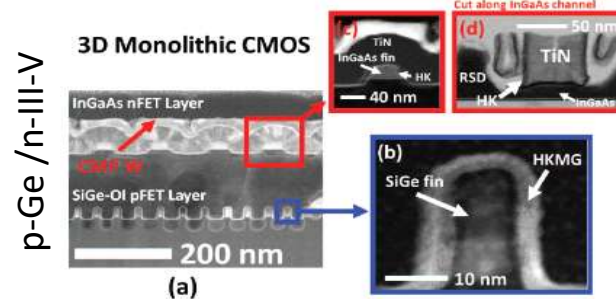
A. Vandooren et al., VLSI'19 (IMEC)



n-Si / p-Ge



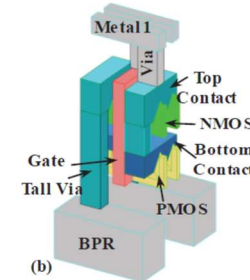
W. Rachmady et al., IEDM'19 (Intel)



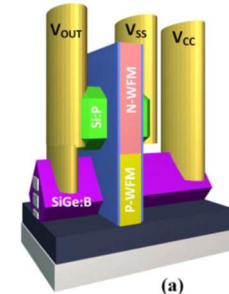
V. Deshpande et al., IEDM'15 (IBM+Leti)

Key argument → Independent transistor's optimization
Simplifying alternative channel co-integration e.g. Ge for pFET & III-V for NFET

CFET → Ultimate cell scaling



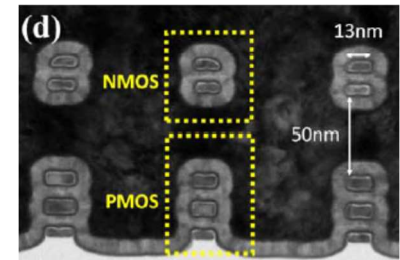
(b)



(a)



S. Subramanian et al., VLSI'20 (Imec)



C-Y. Huang et al., IEDM'20 (Intel)

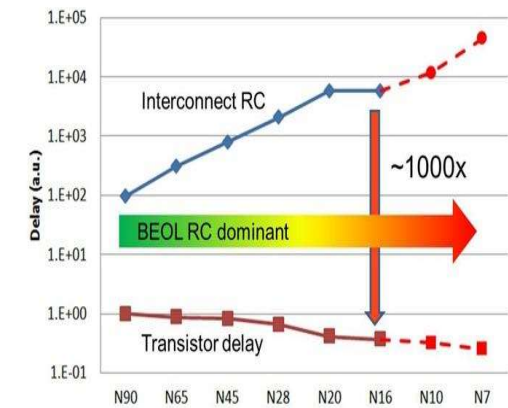
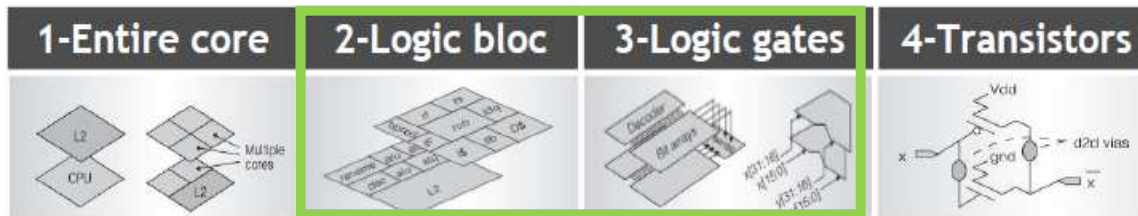
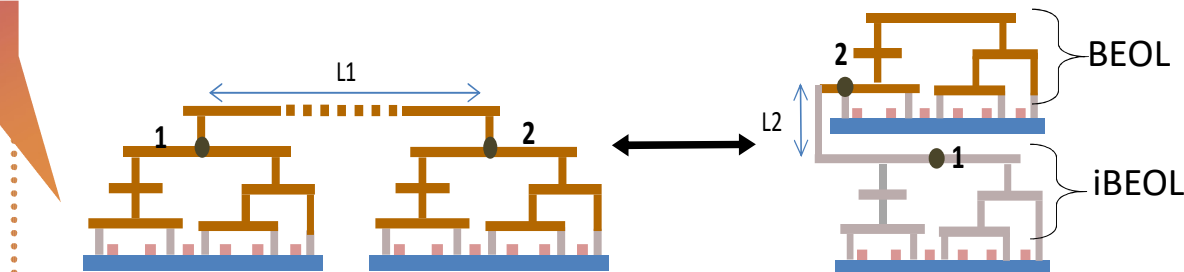
Key argument → Highest scalability
Self aligned bot & top patterning for active and gate

3DSI applications



High Performance for Computing
CMOS over CMOS to reduce interconnect delay

More Moore



G. Yeap, IEDM 2013 (Qualcomm)

3D sequential applications

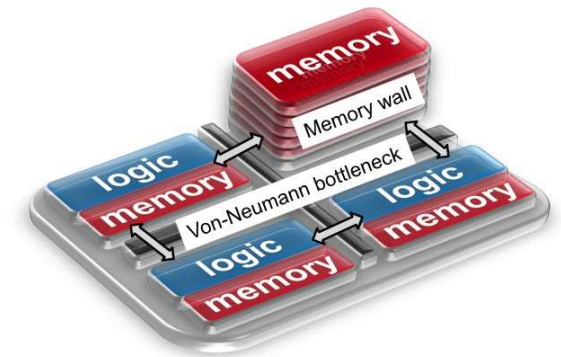


Energy Efficiency



3D Sequential to solve the Memory Wall

Near memory computing / In memory computing



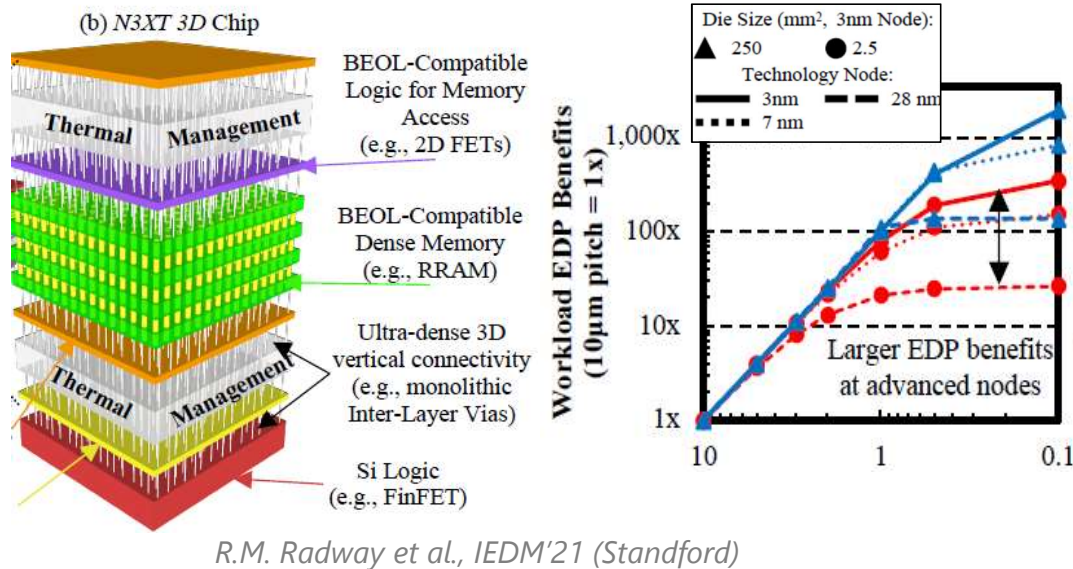
Operation	Energy
Addition of data (fixed point)	1x
Access data (onchip cache)	55x
Access data (offchip DRAM)	3500x

Pedram, IEEE D&T 2016

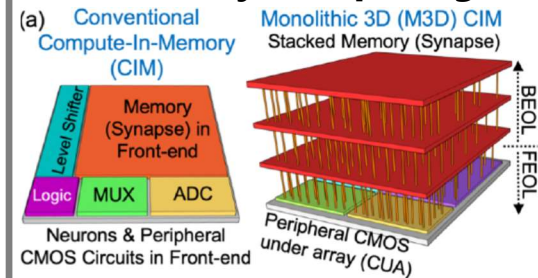


3DSI for Energy Efficient Computing

Near memory Computing Fine grain memory and logic partitioning

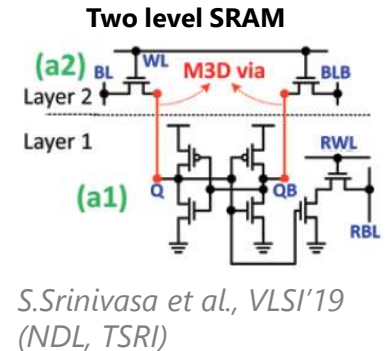
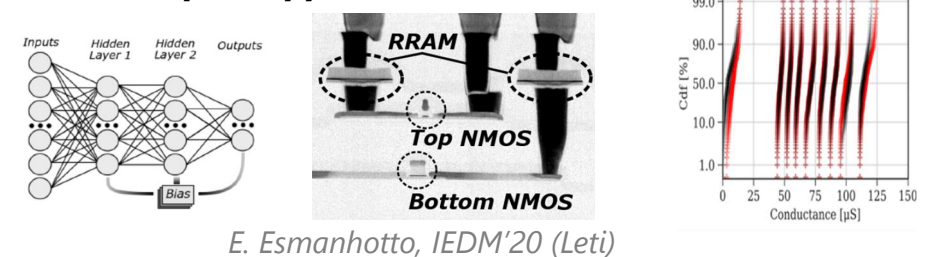


In memory Computing



S. Dutta et al., IEDM'20 (ND Univ)

Neuromorphic approach

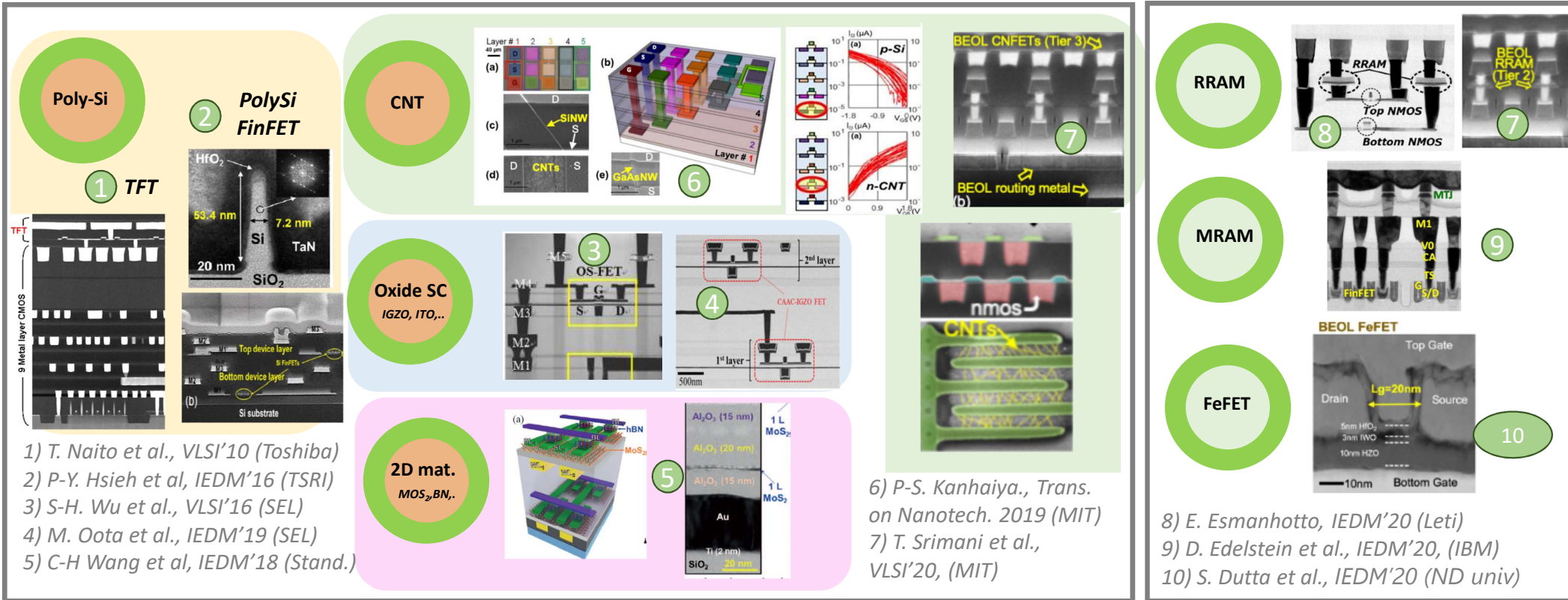


3DSI enables fine grain memory and logic partitioning
Energy Delay Product gain increases with more advanced nodes
Requires iBEOL in between layers. Stacked transistors thermal budget~400-500°C

BEOL compatible materials for 3DSI logic & memory

BEOL FETs

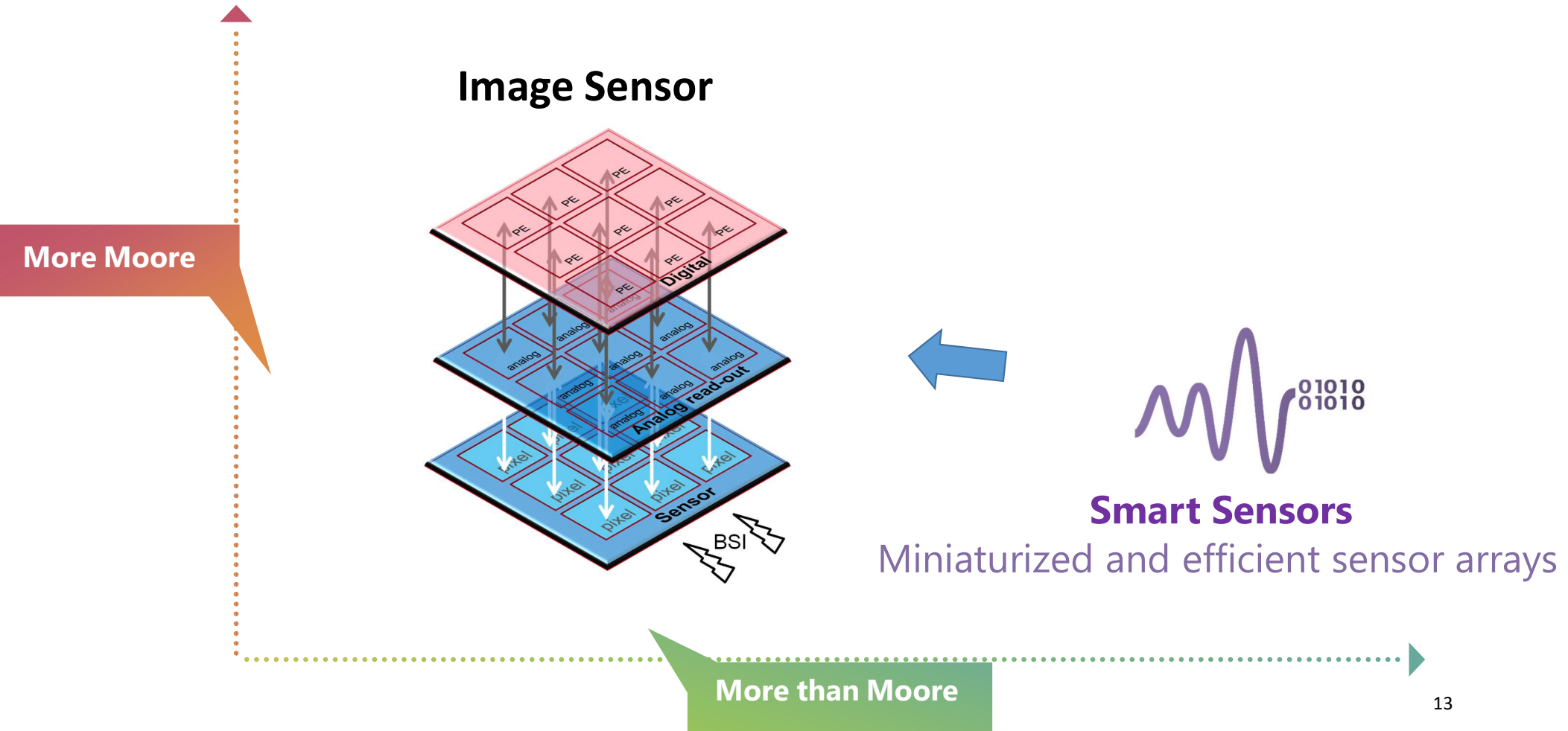
BEOL memory devices



>2 device layer stacking: multilayer
 → Ultra low TB devices, BEOL compatible
 → Low cost devices preferred

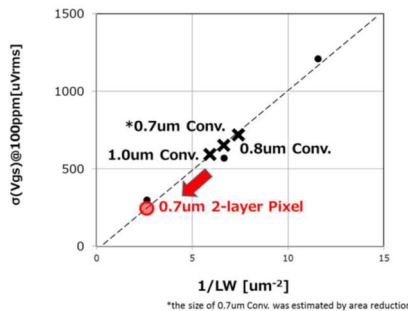
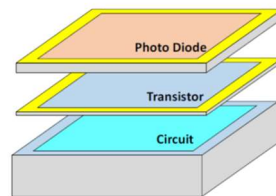
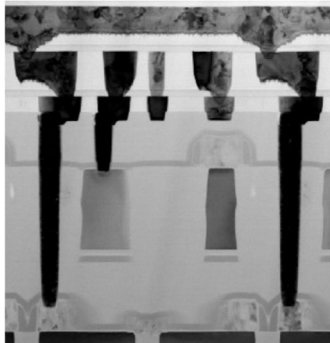


3D sequential opportunities



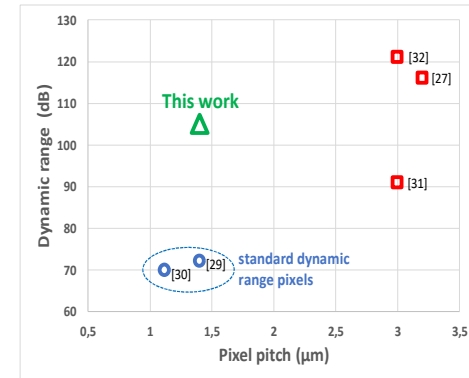
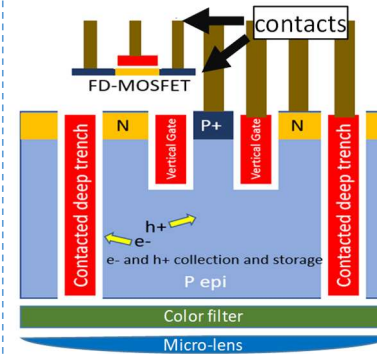
3DSI demonstrators - small pixel image sensors

2-Layer Transistor Pixel Stacked CMOS Image Sensor 33M Pixels 0.7 μm



K. Nakazawa et al., IEDM 2021 (SONY)

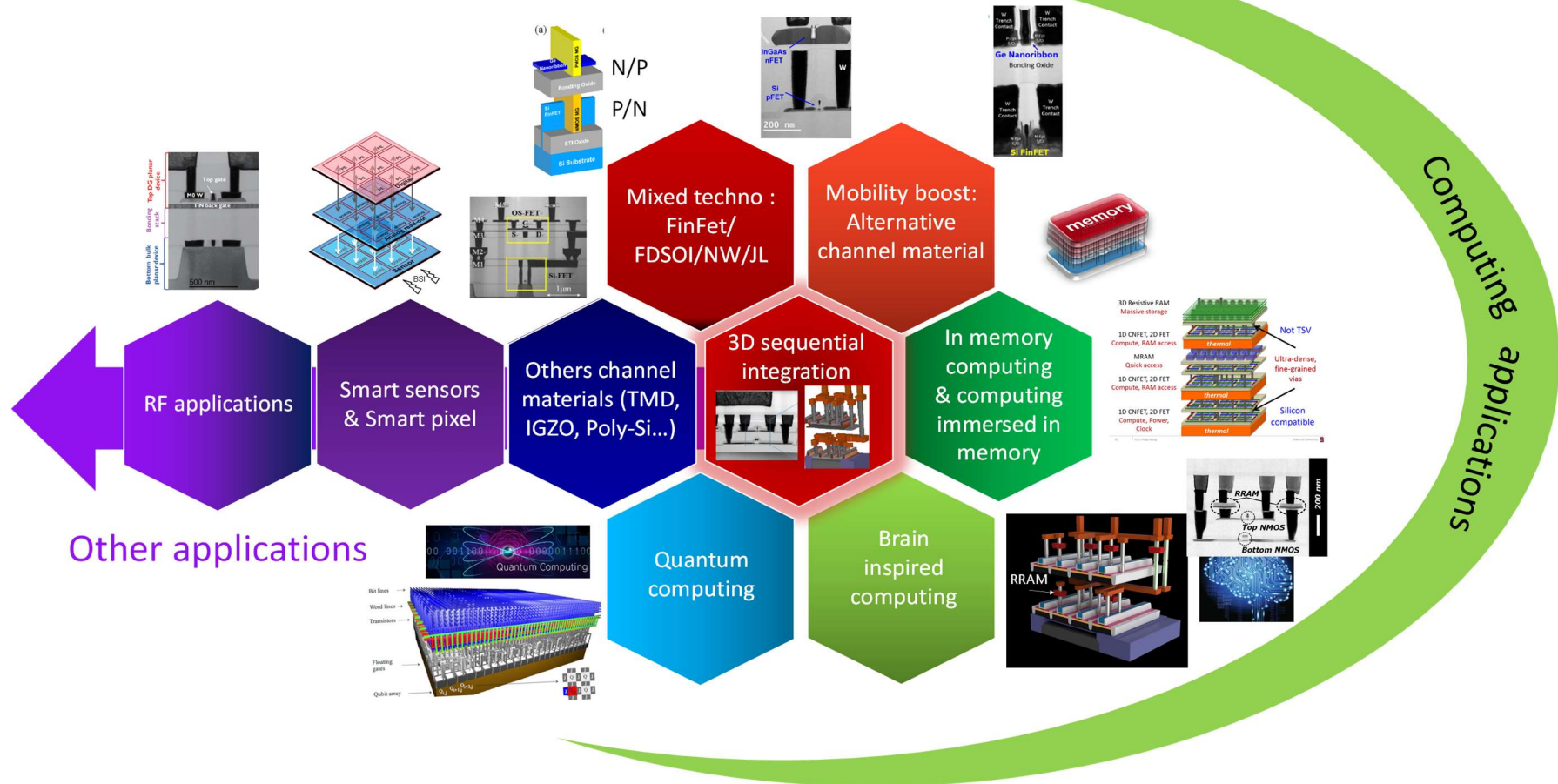
Image Sensor with Back Side PhotoDiode 1.4 μm High Dynamic Range pixel



P. Batude¹, P. Malinge², IEDM 21 (¹Leti, ²STMicroelectronics)

First industrial 3DSI demonstrators → image sensor with improved performance
3D seq offers further scalability and added value (smarter pixel)

3D sequential applications

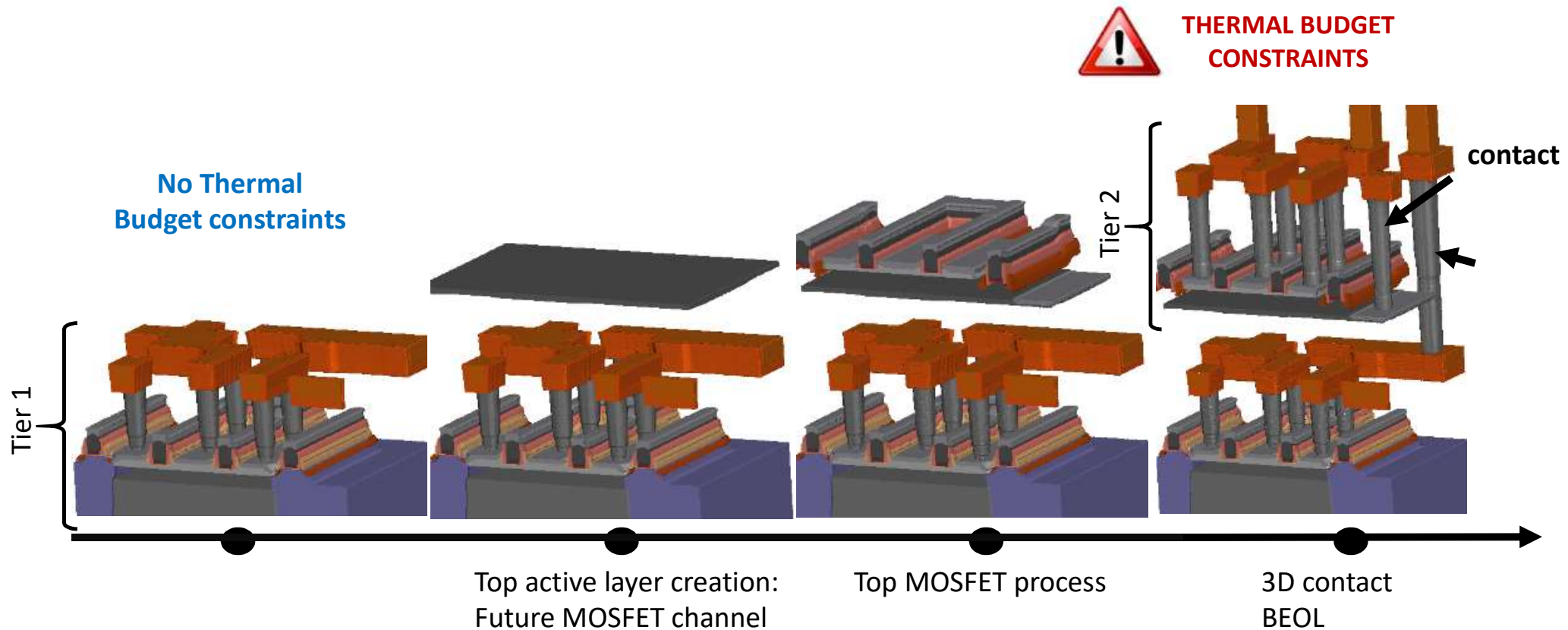


→ 3DSI offers a unique opportunity for More than Moore & Beyond Moore applications¹⁵

Outline

- Introduction to 3D sequential integration
- **Max thermal budget for the Top Tier**
- Key process steps for a low temperature high performance 3DSi CMOS integration
 - Gate stack module
 - Junction engineering
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3D sequential integration flow – Si channel



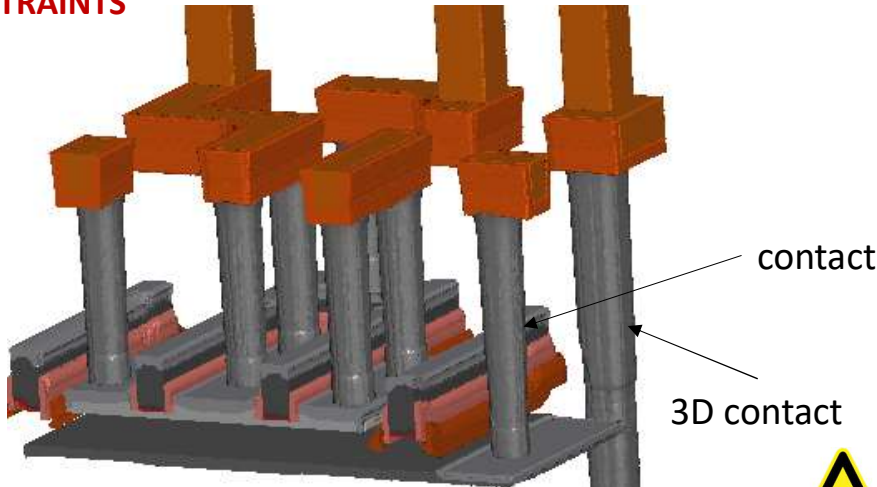
Also named 3D monolithic, 3D VLSI, CoolCube™ ...

3D sequential integration flow – Si channel

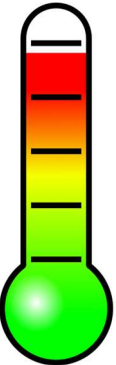
THERMAL BUDGET
CONSTRAINTS



Top Tier



*Max thermal budget for
Top Tier process?*

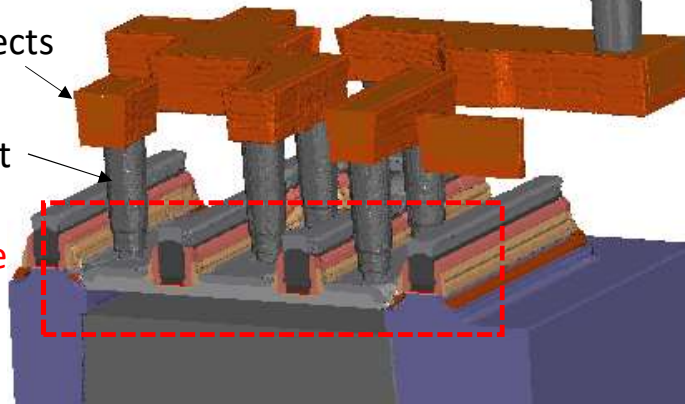


Bottom Tier

Interconnects

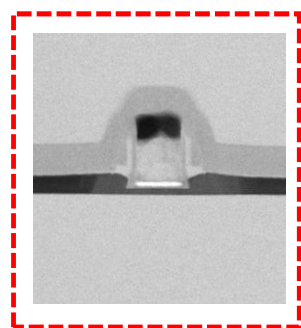
Contact

Device

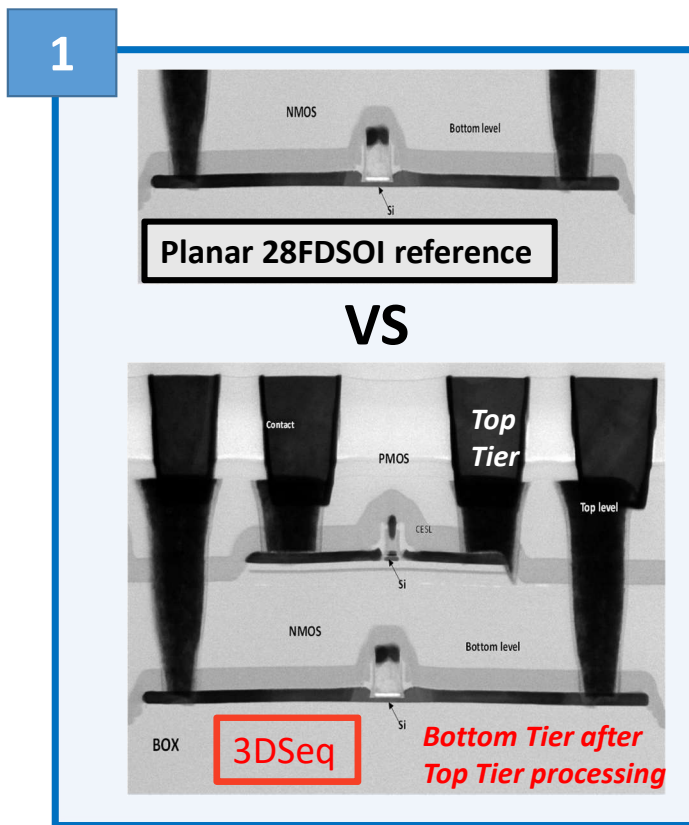


→ Needs to preserve the
stability of the Bottom Tier
ie FET+ Interconnects

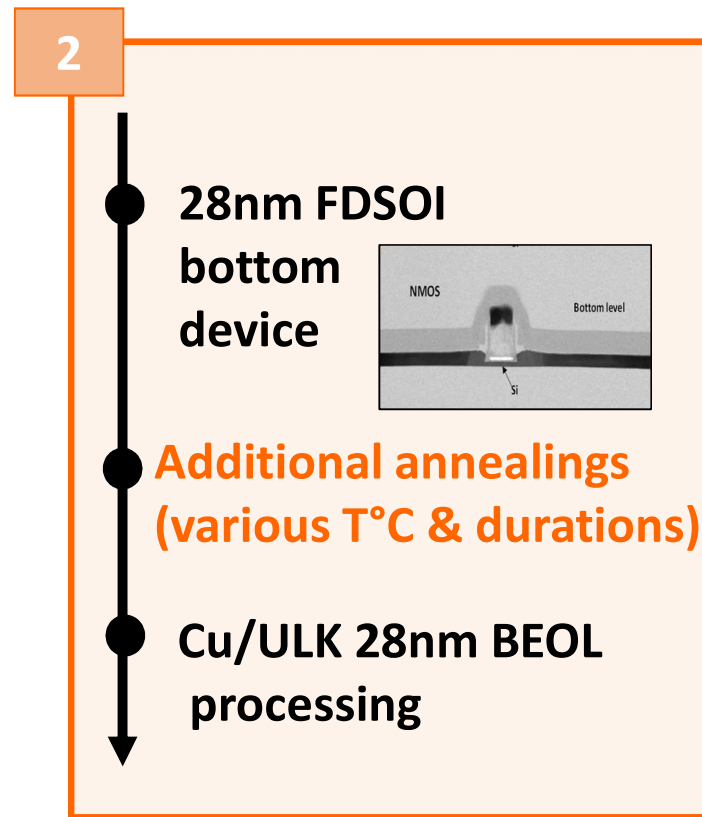
Thermal stability of the Si Bottom Tier? - MOSFET



Single Device



→ Top Tier processed at 630°C-2h (spacer formation)

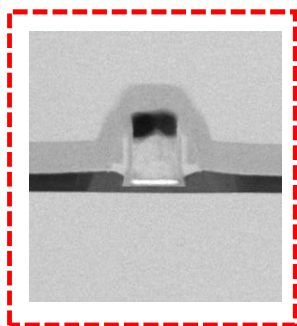


→ Add. Anneals 450-600°C

Thermal Budget

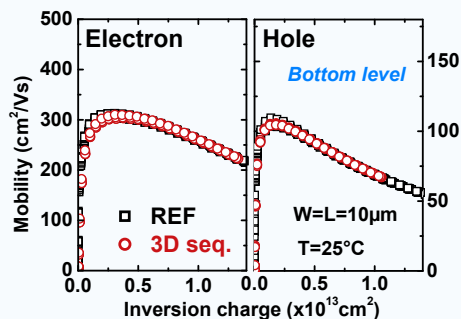
Thermal stability of the Si Bottom Tier? - MOSFET

1

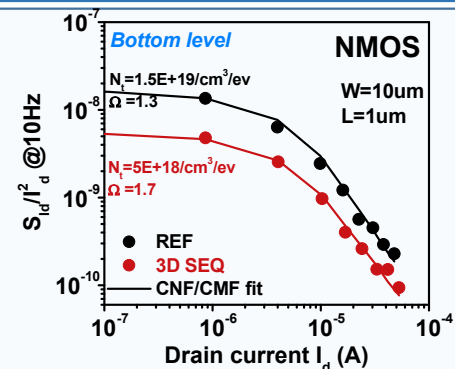


Single Device

Mobility

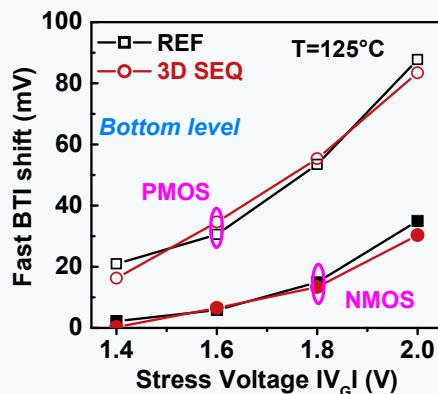


DC perf.



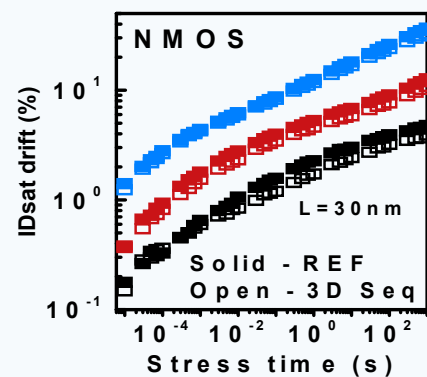
LFN Noise

BTI



Reliability

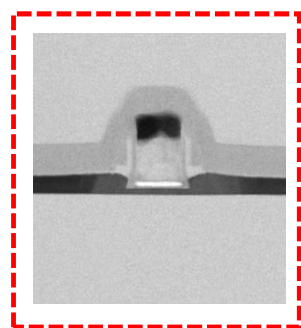
A. Tsiara et al.
VLSI 2018



HCI

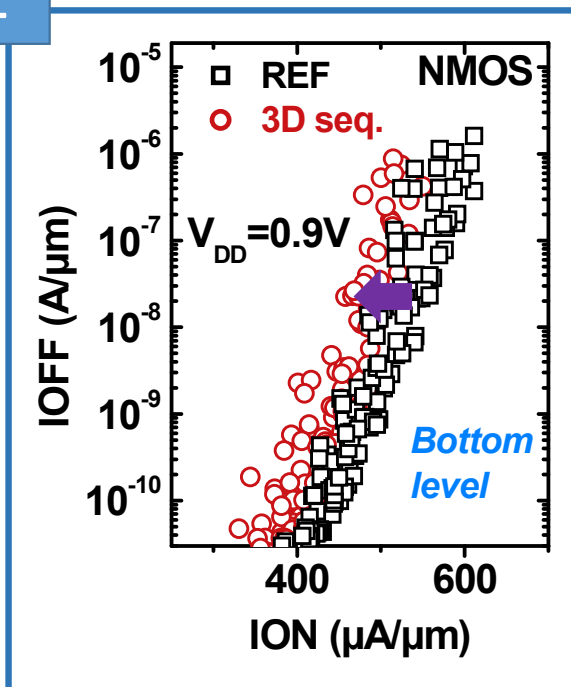
→ Intrinsic MOSFET properties are preserved up to 630°C

Thermal stability of the Si Bottom Tier? - MOSFET



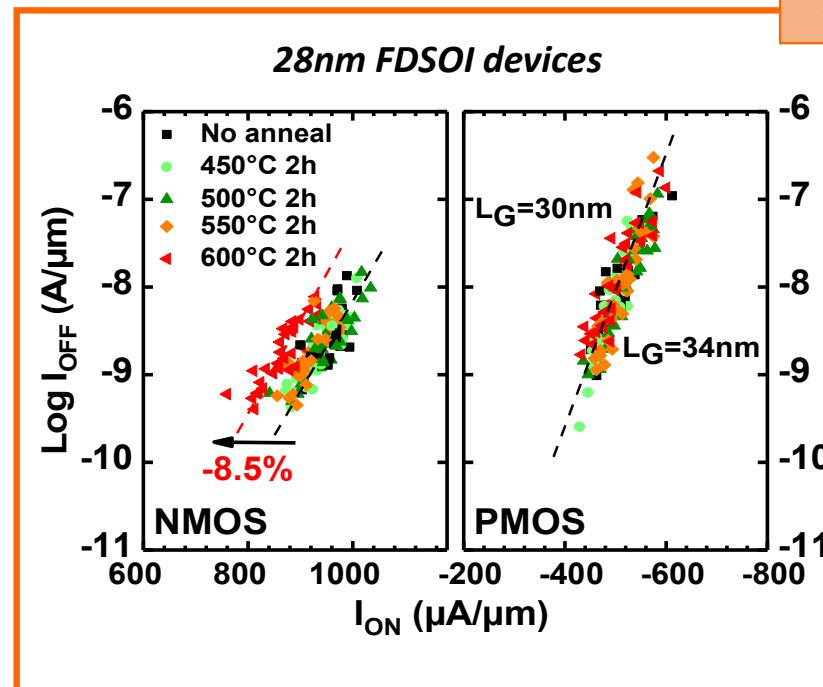
Single Device

1



A. Tsiara et al., VLSI 2018 (Leti)

2

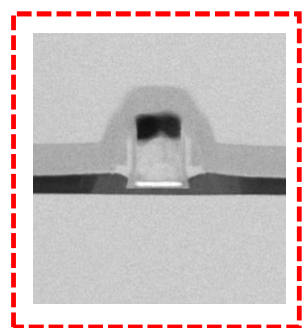


C. Cavalcante et al., VLSI 2020 (Leti)

- Max TB for short channel devices - 550°C-2H
- Perf. degradation at $T > 600^\circ C$

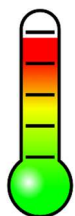
Thermal stability of the Si Bottom Tier? - MOSFET

2



Single Device

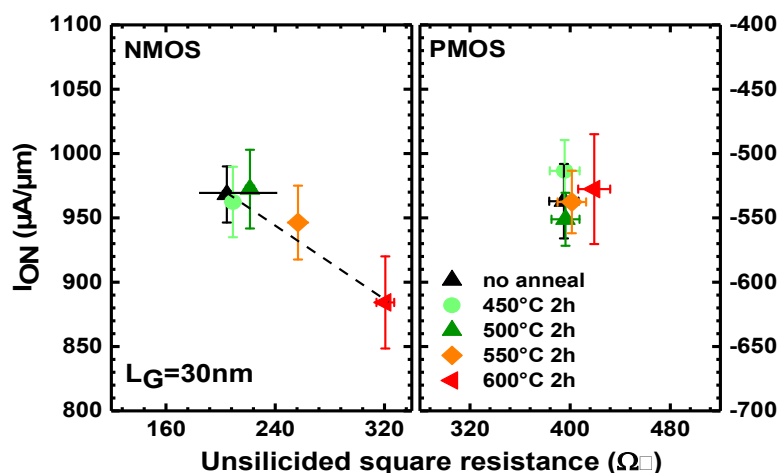
Max TB



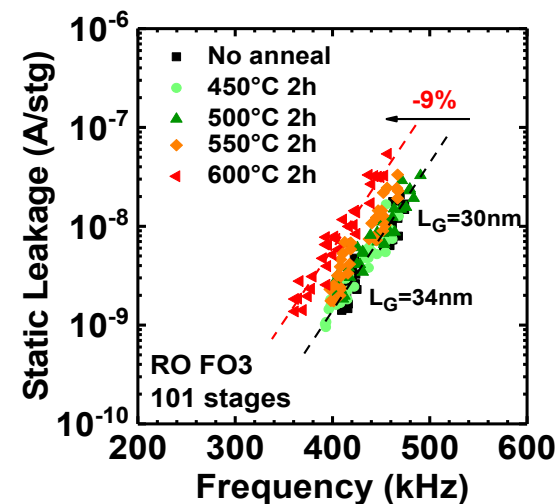
550°C-2H



28nm FDSOI devices



AC perf- ROs



C. Cavalcante et al., VLSI 2020 (Leti)

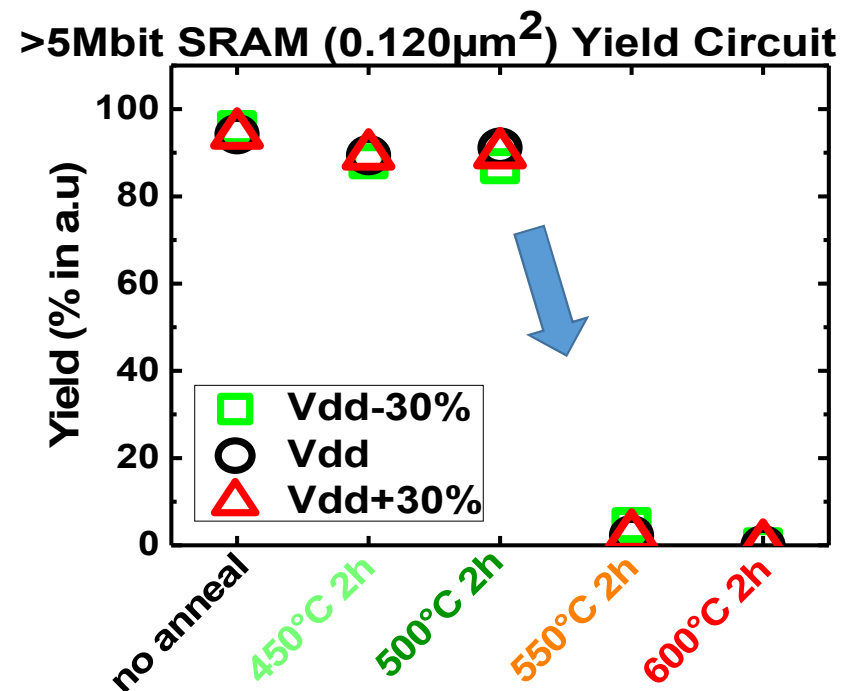
ION correlated to *unsolicited* resistance
 → degradation due to dopants deactivation
 → also impacts AC performance (leakage)

Thermal stability of the Si Bottom Tier? – SRAM array

Dense SRAM Array



- 28FDSOI
5MB SRAM array
- Anneal post CMP, PMD
(various T°C & durations)
- Cu/ULK 28nm BEOL
processing



C. Cavalcante et al., VLSI 2020

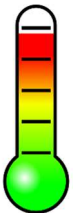
→Yield reduction above 500°C-2H

Thermal stability of the Si Bottom Tier? – SRAM array

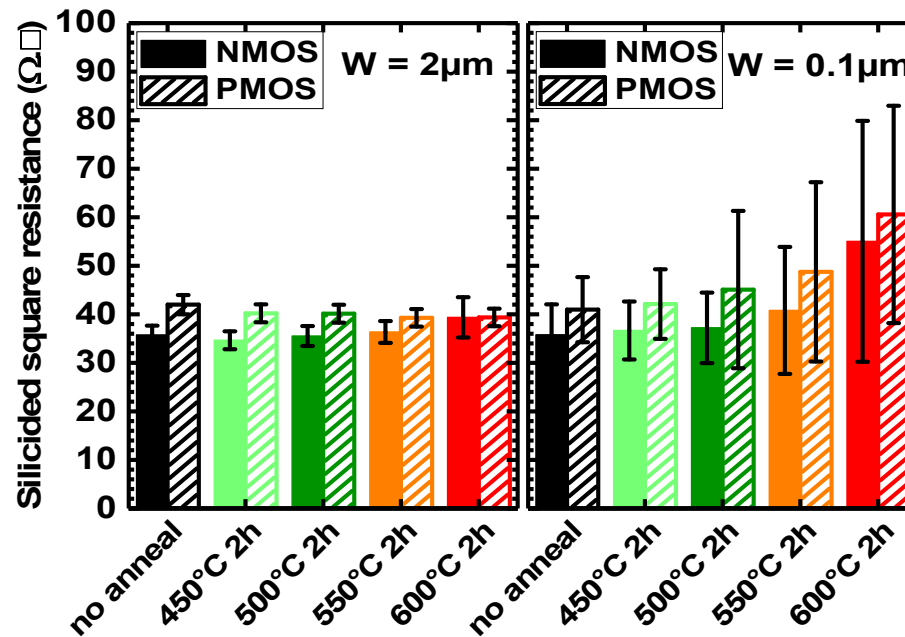
Dense SRAM Array



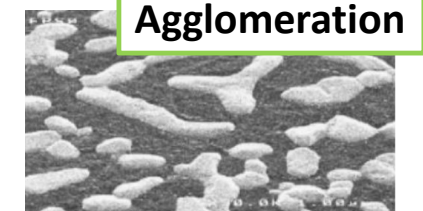
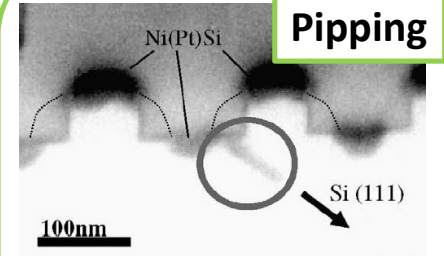
Max TB



500°C-2H



C. Cavalcante et al., VLSI 2020

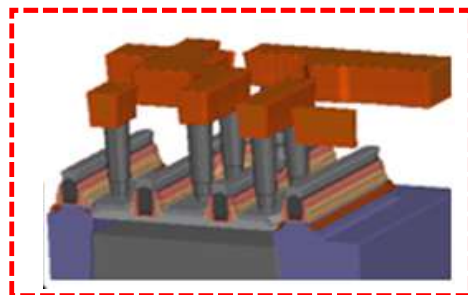


→ Yield reduction above 500°C-2H
→ ascribed to Salicide defects in dense structures

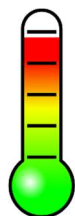
Thermal stability of the Si Bottom Tier? - Interconnects



Array



Array + Interconnects



***500°C-2H
compatible
with BEOL?***

3

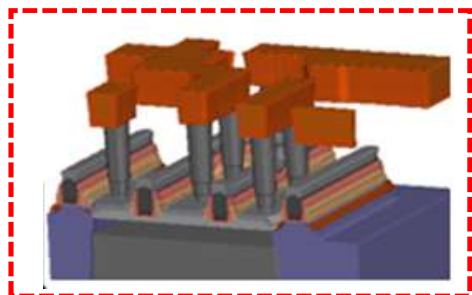
● 28nm FDSOI FEOL

● Cu/ULK 28nm BEOL

● Additional annealings
(T= 450°C-525°C
& durations)

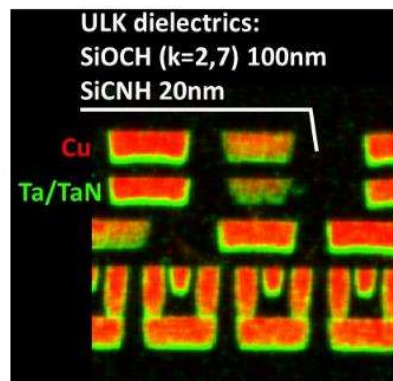
Thermal stability of the Si Bottom Tier? - Interconnects

3

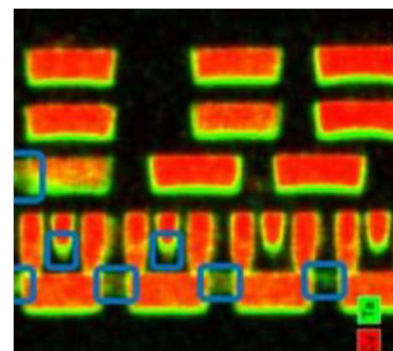


Array + Interconnects

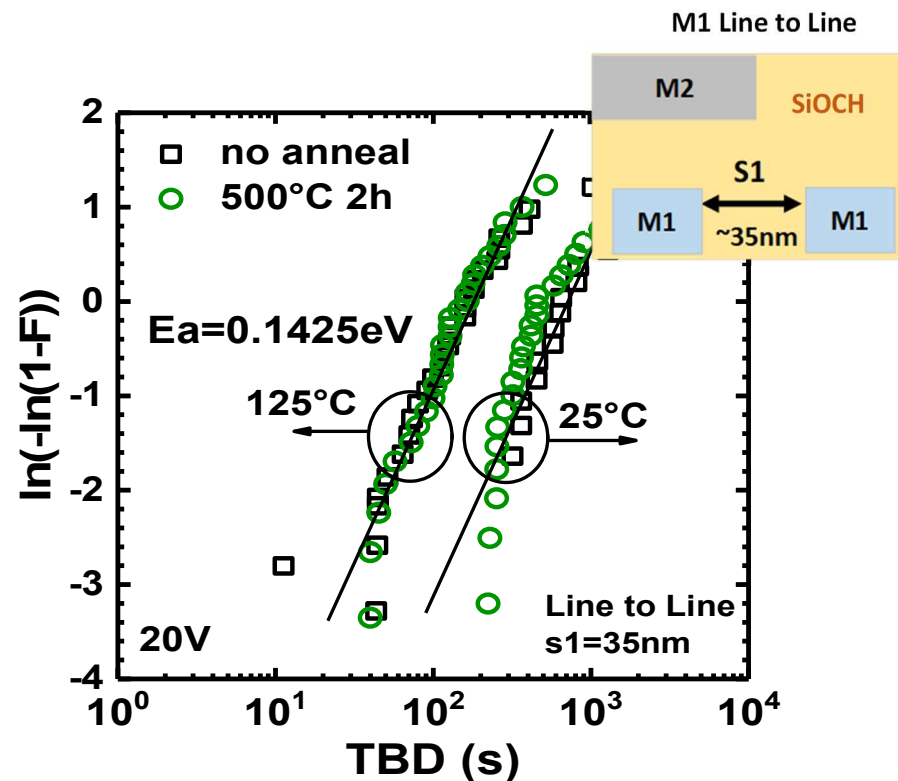
No anneal



525°C-2h



S. Beaupaire et al., MRS Spring, 2019



C. Cavalcante et al., VLSI 2020

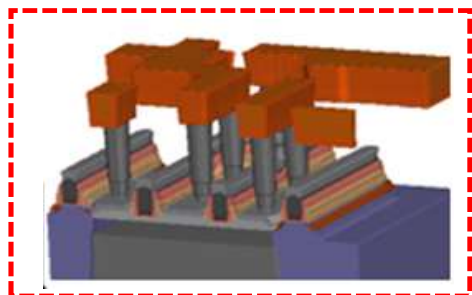
→ Interconnects are stable up to 500°C-2H

Thermal stability of the Si Bottom Tier? - FEOL+BEOL



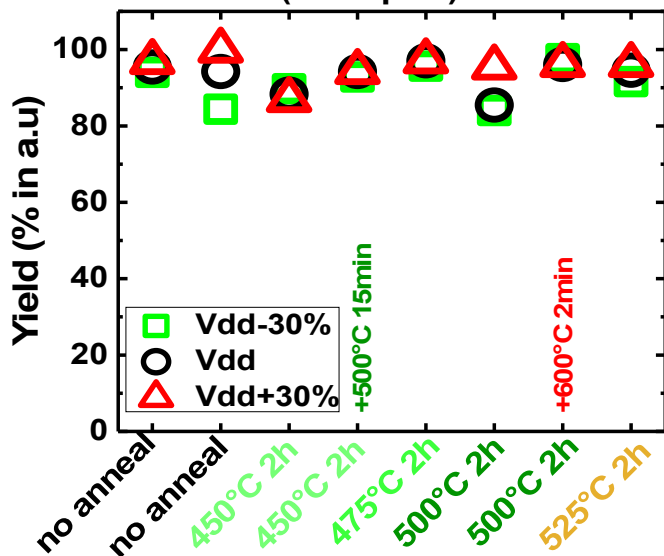
Anneals

3

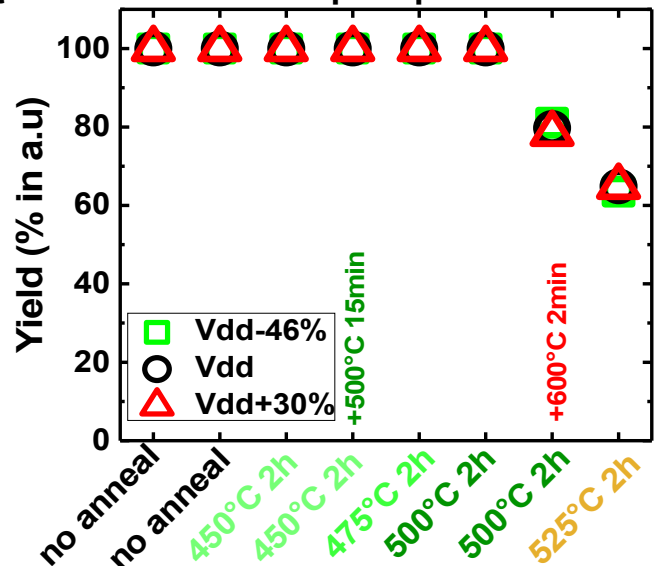


Array + Interconnects

>5Mbit SRAM (0.120 μm^2) Yield Circuit



1 Million Flip Flop Yield Circuit



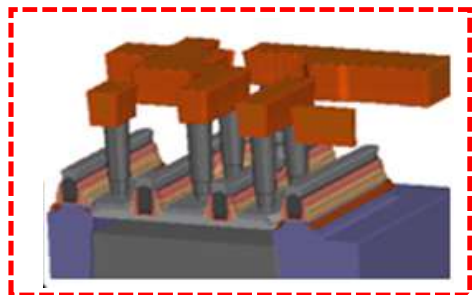
→ Interconnects are stable up to 500°C-2H
 → Confirmed by yield analysis on dense arrays

Thermal stability of the Si Bottom Tier? - FEOL+BEOL

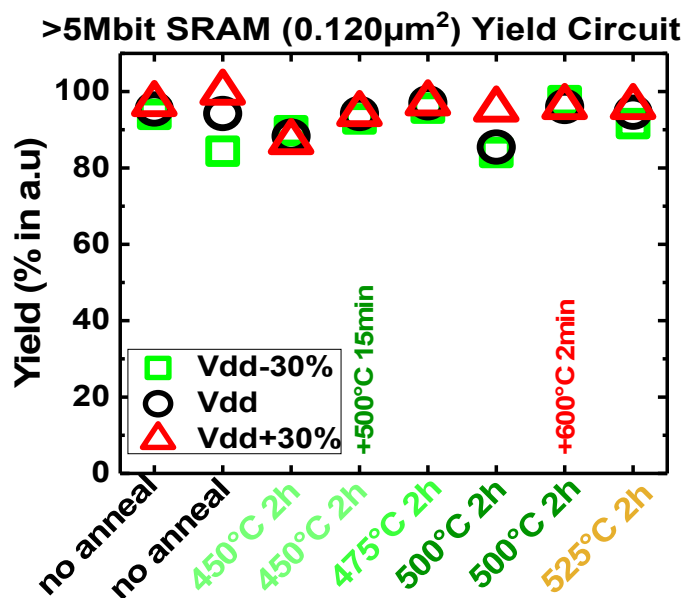


Anneals

3



FEOL+BEOL



→ FEOL stable up to 500°C-2h
→ BEOL stable up to 500°C-2h

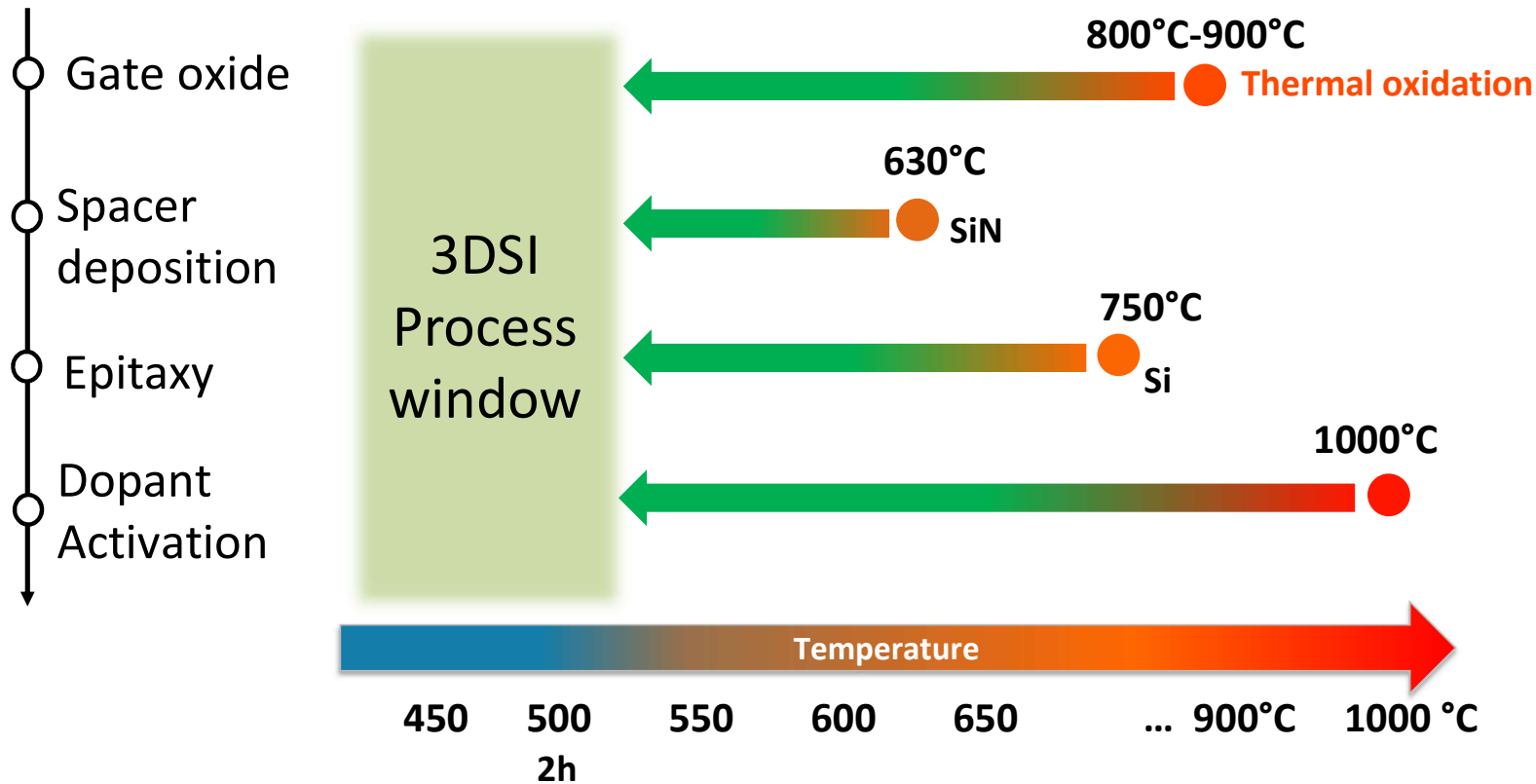


Safe thermal
budget
for Top Tier
processing
500°C 2h

Outline

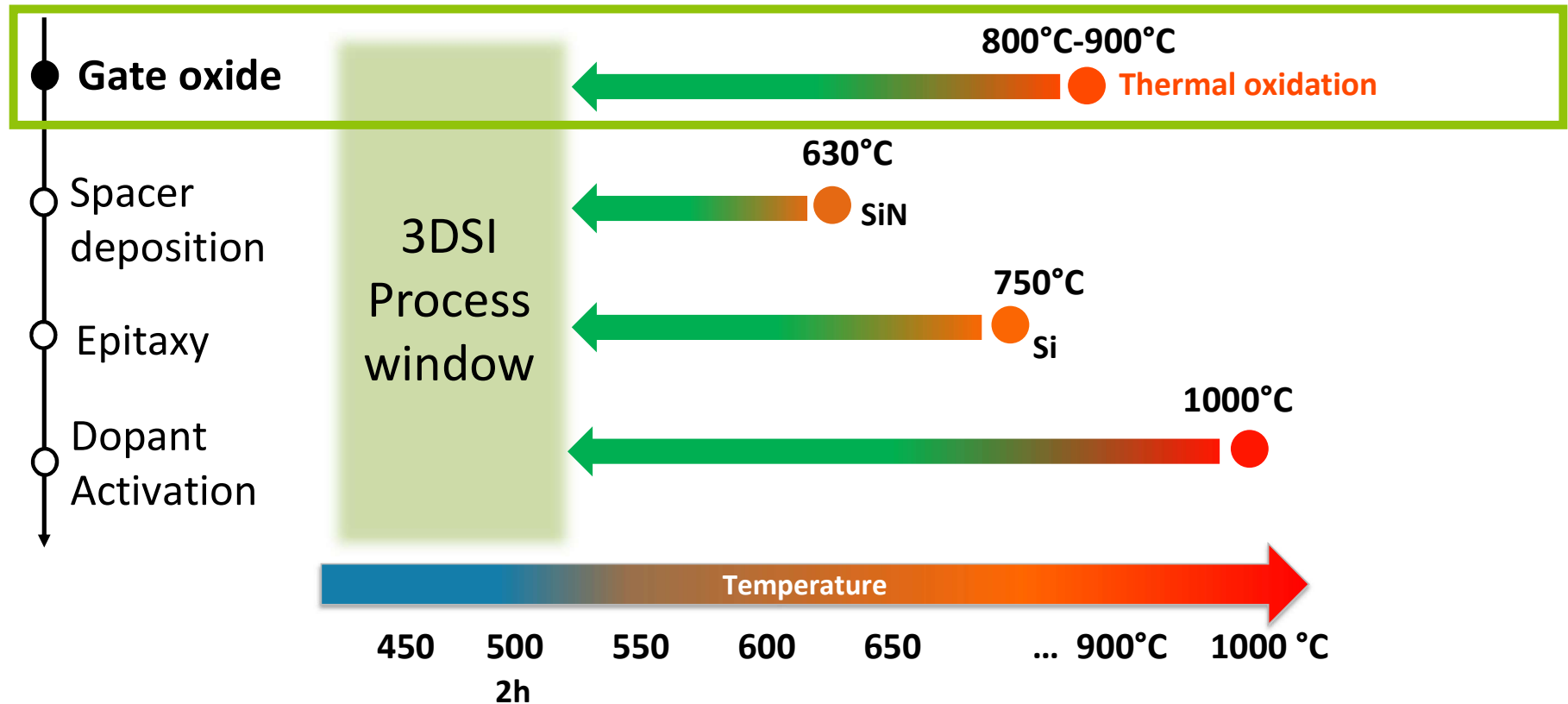
- Introduction to 3D sequential integration
- Max thermal budget for the Top Tier
- Key process steps for a low temperature high performance 3DSi CMOS integration
 - Gate stack module
 - Junction engineering
 - Other processes required for RF applications
- Conclusion

Low temperature process for Top Tier



→ Each step of the Si process flow must be revisited to fabricate the Top Tier at 500°C

Low temperature process for Top Tier



→ Each step of the Si process flow must be revisited to fabricate the Top Tier at 500°C

Gate stack challenges at low temperature

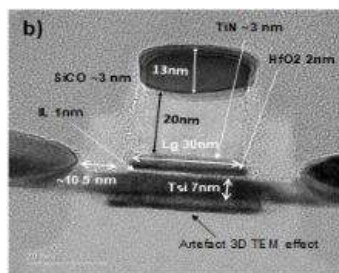
● Gate oxide

■ Main issue at 500°C → oxide reliability

→ Cannot use “Reliability anneals” at $T > 800^\circ\text{C}$ to cure oxide defects

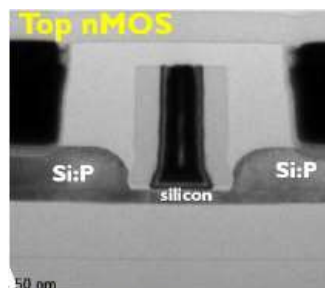
→ Same concern for both Gate First & Gate Last

Gate First

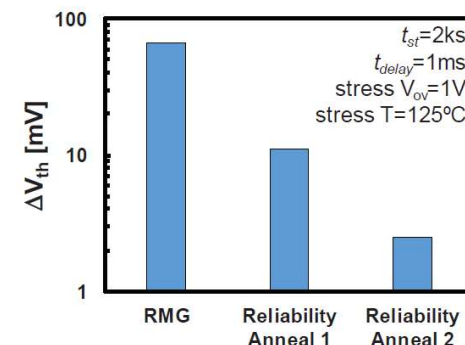


C. Fenouillet-Beranger et al., EDL, 68, 2021 (Leti)

Gate Last /RMG



A. Vandooren et al., EDL, 65, 2018 (IMEC)



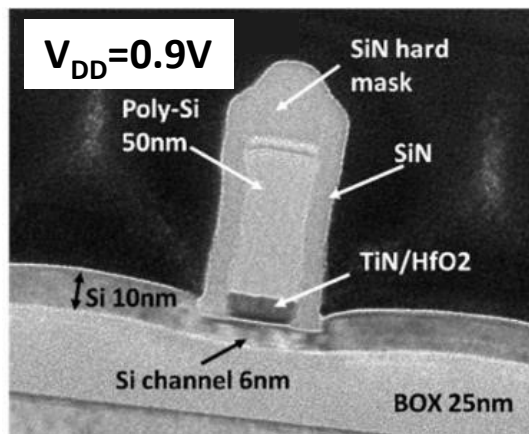
J. Franco et al., IEEE IRPS, 2017

Gate stack needs to be rethought

Gate stack challenges at low temperature

● Gate oxide

Digital CMOS

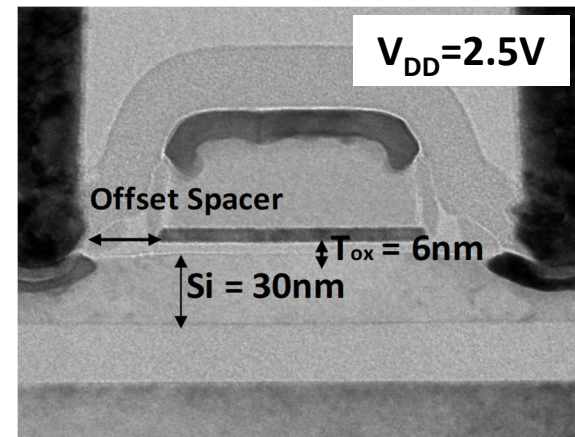


L. Brunet et al., IEDM 2018 (Leti)

Max TB
500°C-2H

- N&PMOS $L_G=30\text{nm}$
- undoped Si film 6nm
- thin oxide HK/MG

Analog



C. Cavalcante et al., IEEE VLSI-TSA 2020 (Leti)

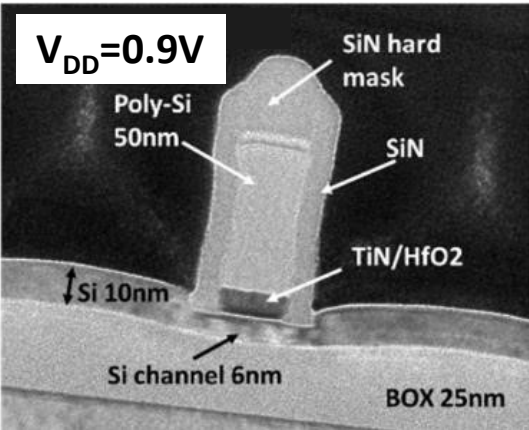
Gate First

- N or PMOS $L_G=250\text{nm}$
- doped Si film 30nm
- thick oxide $\text{SiO}_2 \sim 6\text{nm}$

Gate stack challenges at low temperature

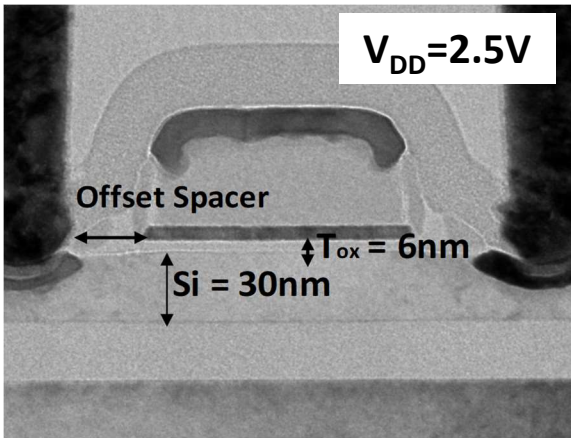
● Gate oxide

Digital CMOS



L. Brunet et al., IEDM 2018 (Leti)

Analog



C. Cavalcante et al., IEEE VLSI-TSA 2020 (Leti)

Max TB
500°C-2H

Requirements		Digital	Analog
Performance	EOT	++	--
	Leakage	-	+
	LF Noise	-	++ (low Dit)
Reliability		++ (NBTI&PBTI)	+ (NBTI or PBTI)

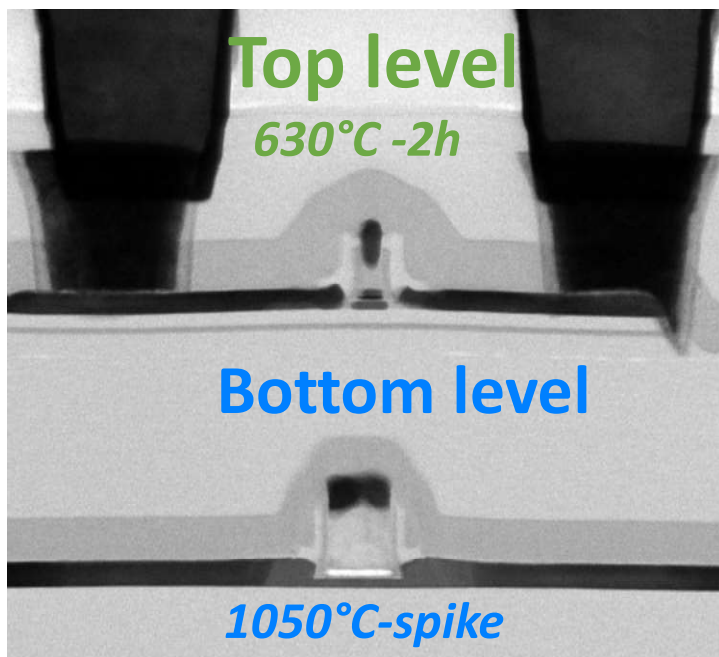
Challenging

↑ High

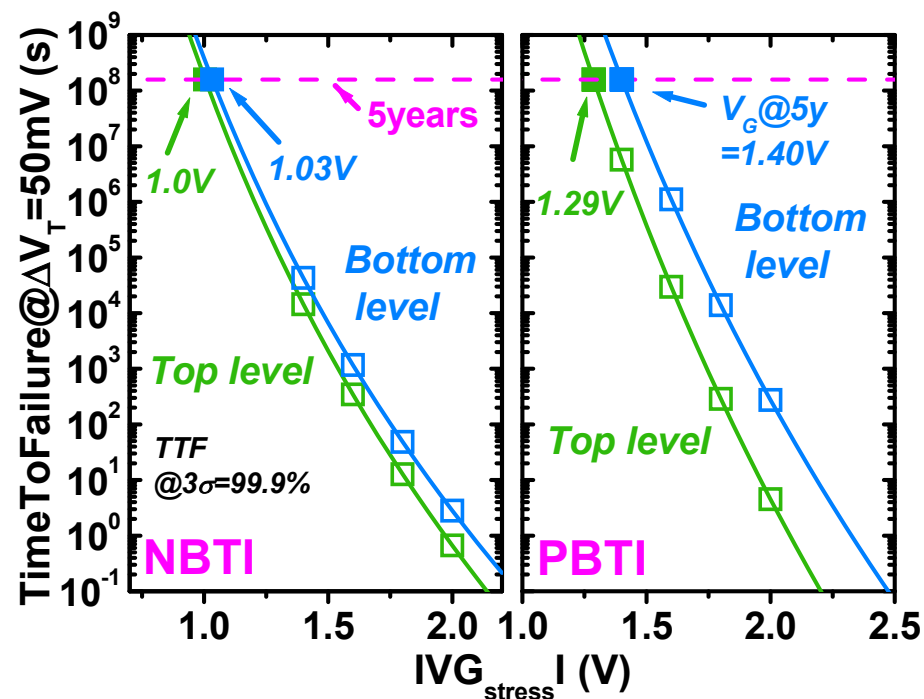
↓ Low

Gate Oxide Reliability - true 3DSI integration

Digital
HK/MG



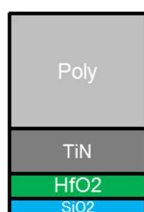
A. Tsiara et al., VLSI 2018 (Leti)



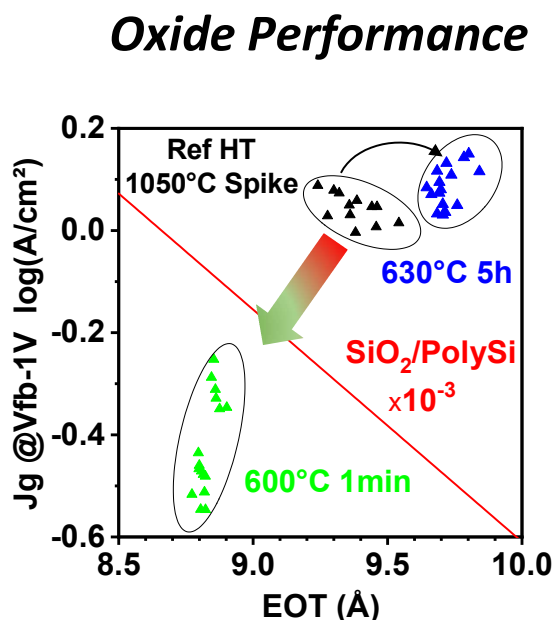
→ Top Level (630°C-2h) meets the BTI requirements
 → But TB must be reduced to 500°C-2h

Impact of Thermal Budget on thin oxide - Digital

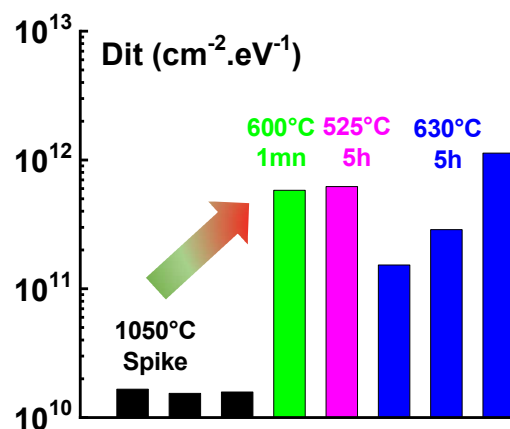
Digital



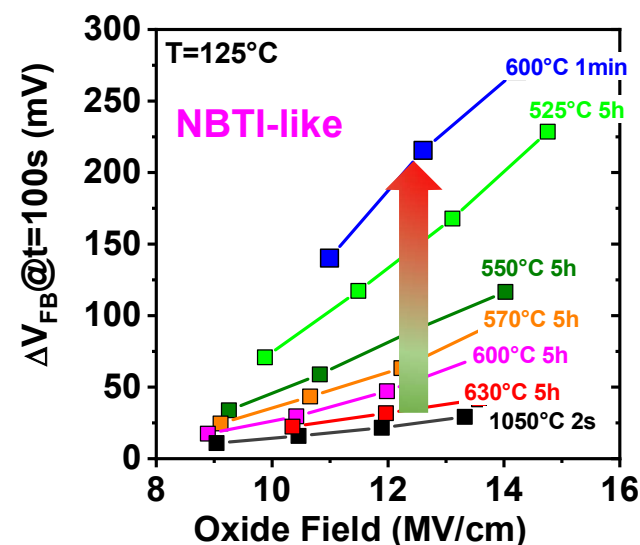
MOScap



Interface Quality



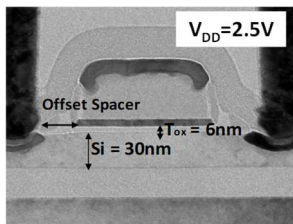
Oxide Reliability (NBTI)



→ Reducing the Thermal Budget $< 600^\circ C$ is favorable to improve gate stack perf. (lower EOT)
 → But also degrades interface quality and NBTI reliability

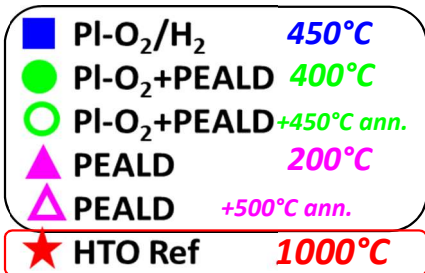
Impact of Thermal Budget on thick oxide - Analog

Analog



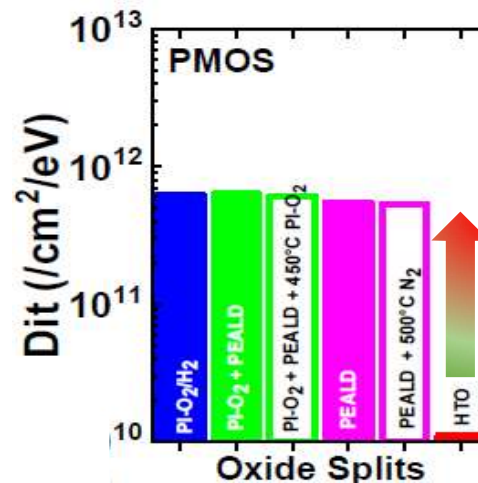
PMOSfet

SiO₂ 6nm

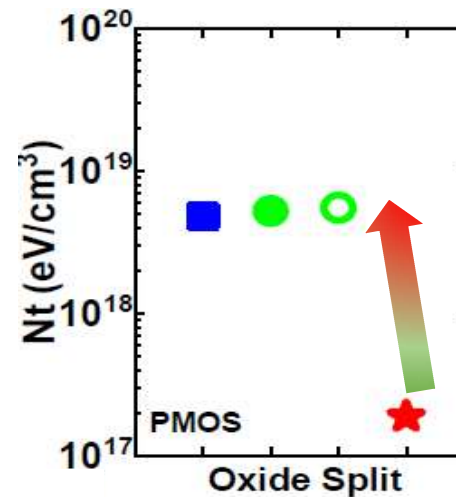


Low Temp
Plasma
oxidation

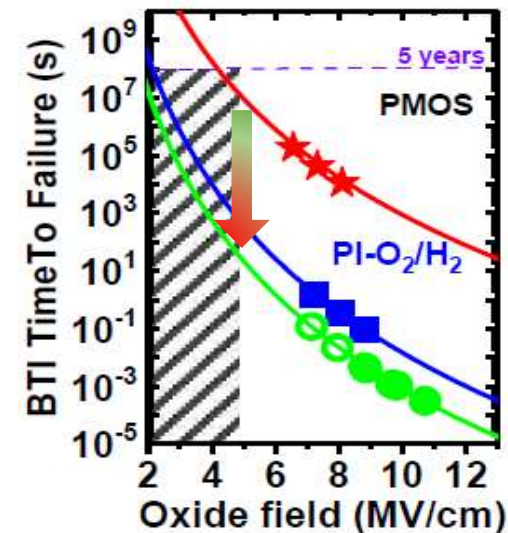
Interface Quality



LF Noise



NBTI reliability



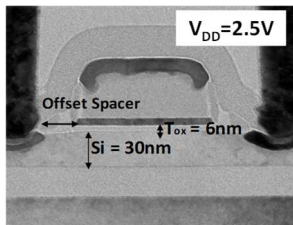
C. Cavalcante et al., IEEE VLSI-TSA 2020 (Leti)

→ Same behavior for thick oxide

→ Reducing TB below 500°C degrades interface quality, Noise and NBTI reliability,

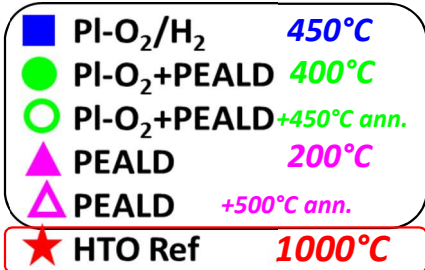
Impact of Thermal Budget on thick oxide - Analog

Analog



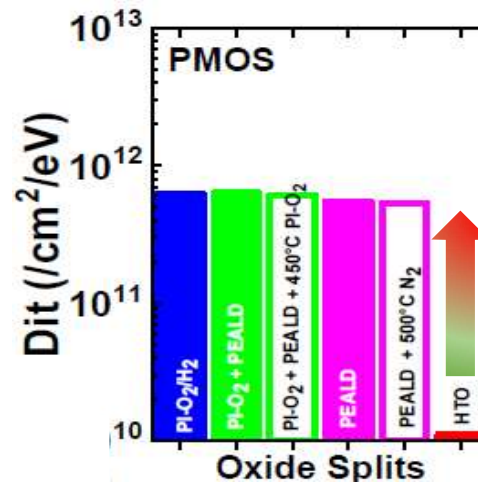
PMOSfet

SiO₂ 6nm

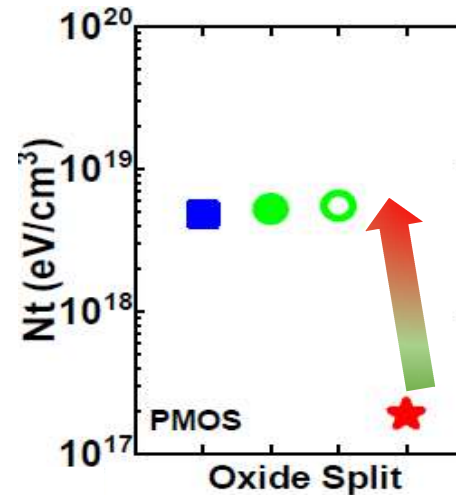


Low Temp
Plasma
oxidation

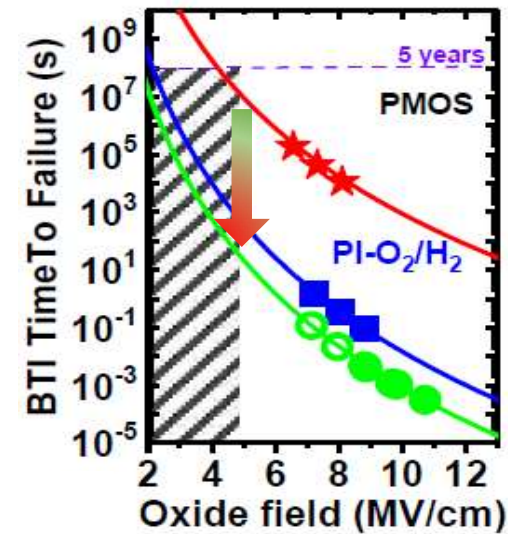
Interface Quality



LF Noise



NBTI reliability



High Dit



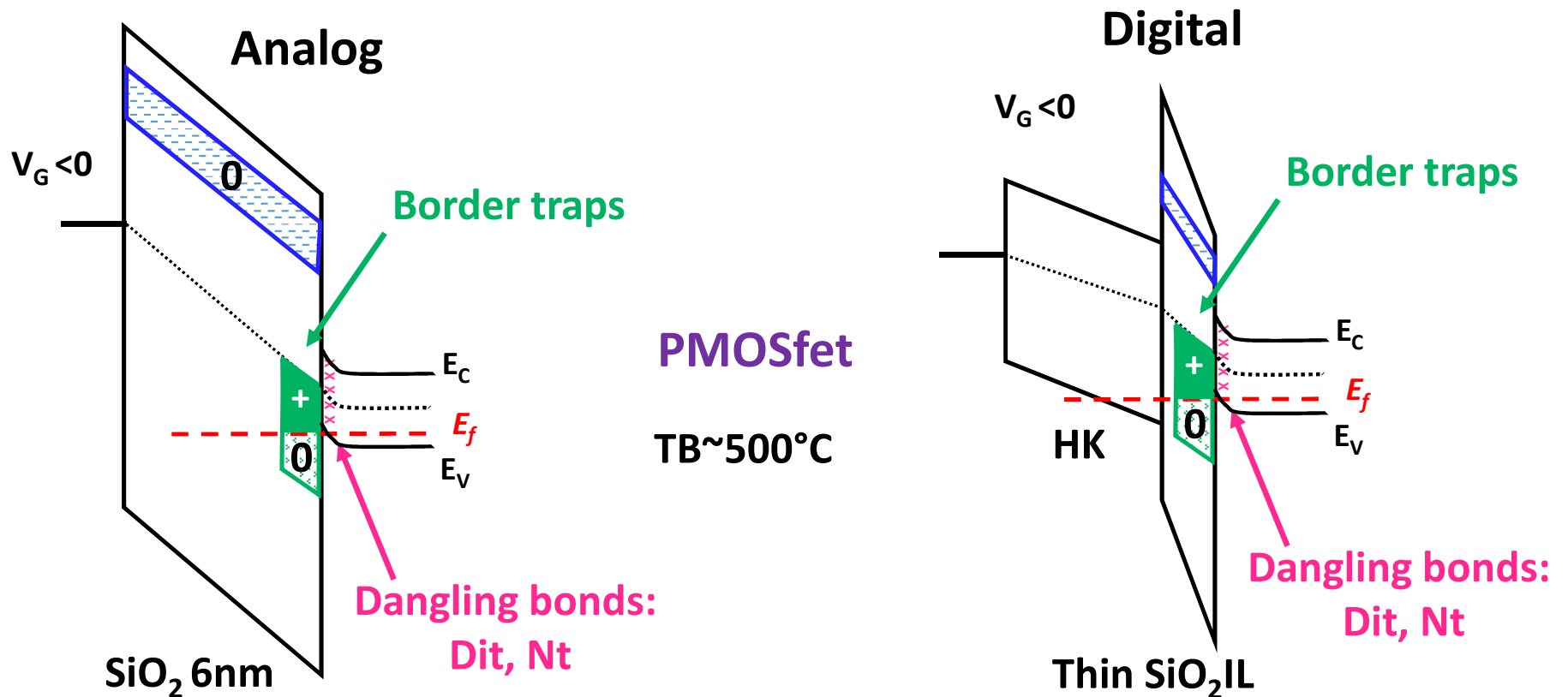
High Nt



Low NBTI lifetime

→ Great correlation between Dit, Noise and NBTI

Understanding of poor Low Temp PMOS reliability

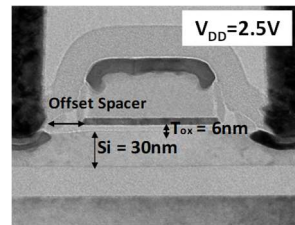


→ Same degradation for Analog & Digital gate stacks

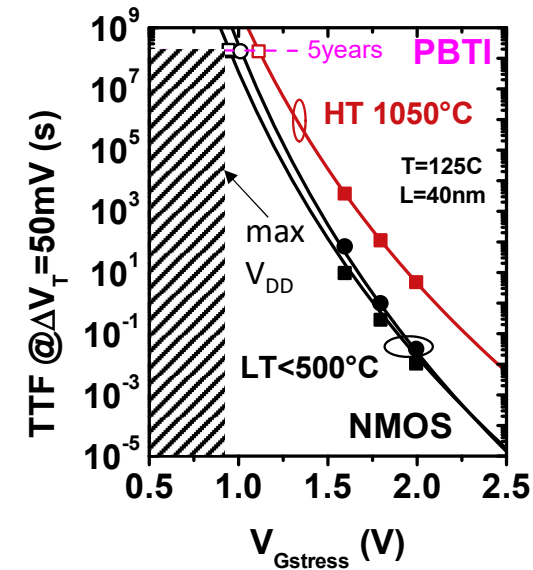
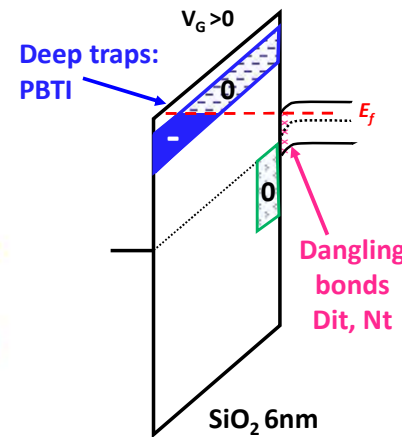
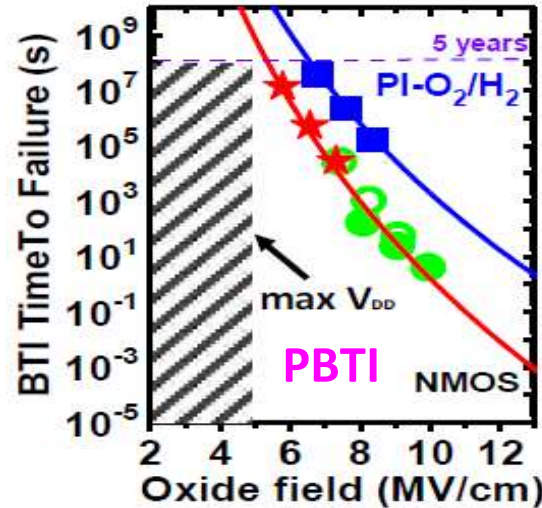
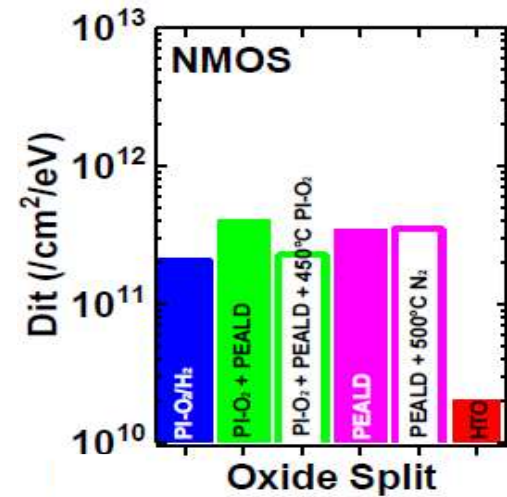
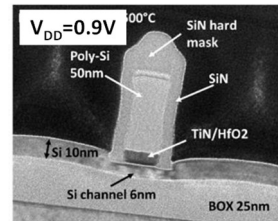
→ Higher Si Interface + Border Traps in SiO_2 or IL are responsible for poor PMOS reliability

NMOS reliability at low temperature

Analog



Digital



Dit ≠ PBTI traps

- PBTI reliability at $T < 500^\circ\text{C}$ due to deep traps in bulk SiO_2 or bulk HK
- meet the requirements for both digital & analog applications unlike NBTI

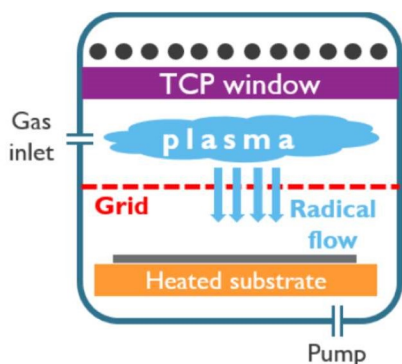
Gate stack reliability improvement strategies

- Multiple strategies to achieve sufficient BTI reliability in top-tier low temperature devices
 - Atomic hydrogen treatment (PMOS NBTI)
 - J-Less operation in accumulation mode → BTI improvement
 - Dipole insertion between SiO_2 and HfO_2
 - Back Bias forward in inv mode MOS → BTI improvement

Z. Wu et al, IEEE Trans on Elec Dev Vol 88, n°2, Feb 2021

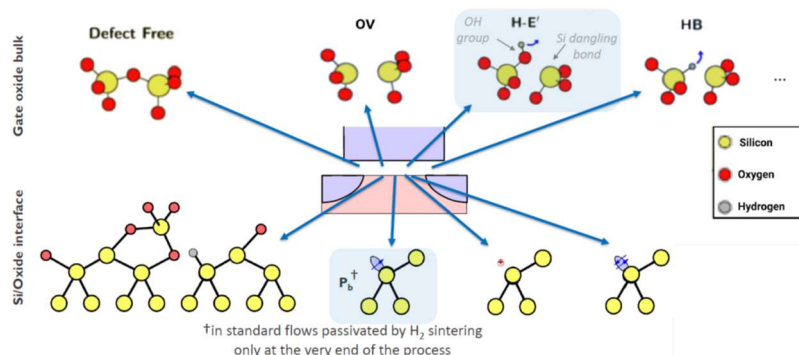
Multiple strategies to achieve sufficient BTI reliability in top-tier low temperature devices

NBTI solution - Low Temp Atomic Hydrogen anneal

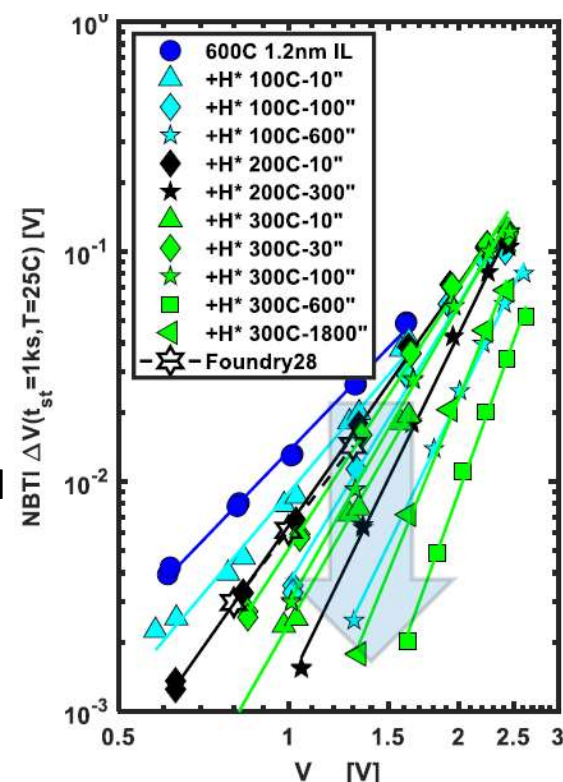


- IL formation
 - ISSG 600°C 1.2/1.8nm or chemOx 0.6nm
 - Additional ref.: ISSG 700°C, RTO 900°C
- H* exposure (remote H₂ plasma)
 - 100/200/300°C, 10"-1800"
- [Sint. H₂ 400°C-20' for EOT control] ←
- 1.8nm HfO₂ dep. (300°C)
- 5nm TiN (450°C) + 60nm W dep. (430°C)
- Gate patterning
- Sintering H₂ 400°C-20'

Microscopic defect structures in Si/SiO₂ system



Hydrogen radicals (H*) generated in a low-T remote plasma were used to passivate hole traps associated with the hydroxyl-E' (H-E') SiO₂ defects in 1.2nm thick interface layers (IL).

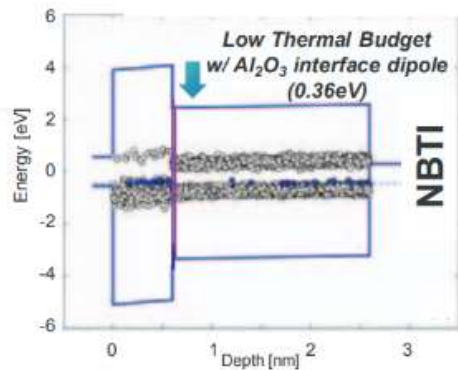


J. Franco et al., IEEE VLSI 2021 (IMEC)

→ Remote Hydrogen plasma improves NBTI

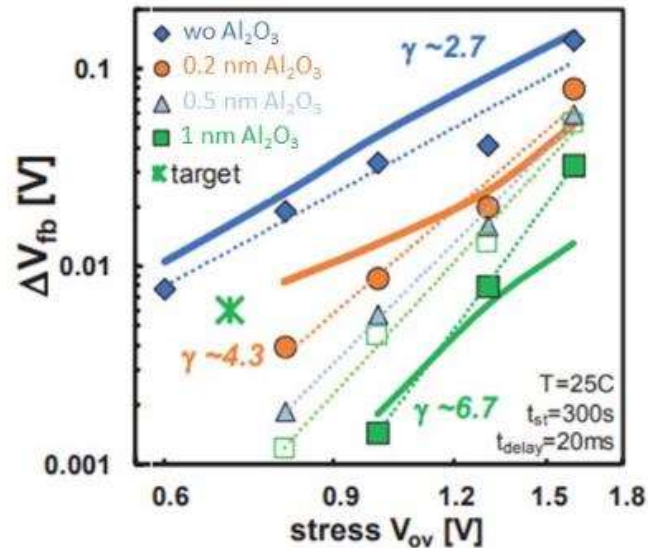
Other NBTI reliability solutions

Al₂O₃ Dipole insertion between SiO₂ and HfO₂

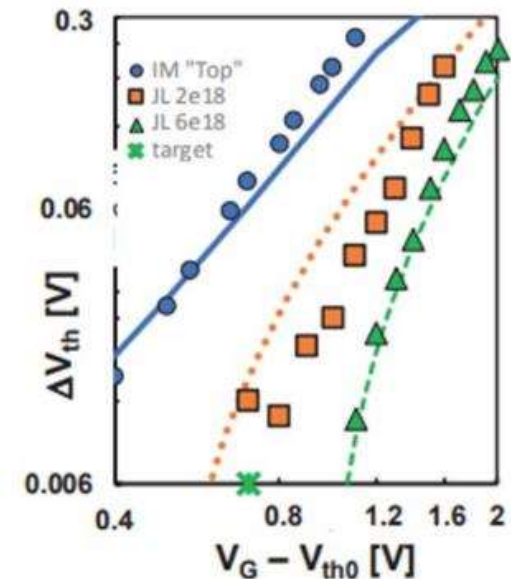


J. Franco, IEDM 2018 (imec)

Negative dipole former on SiO₂
Defect energy shift relatively to valence band
Shift of V_{fb} 0.4eV LaSiOx



Junction less device

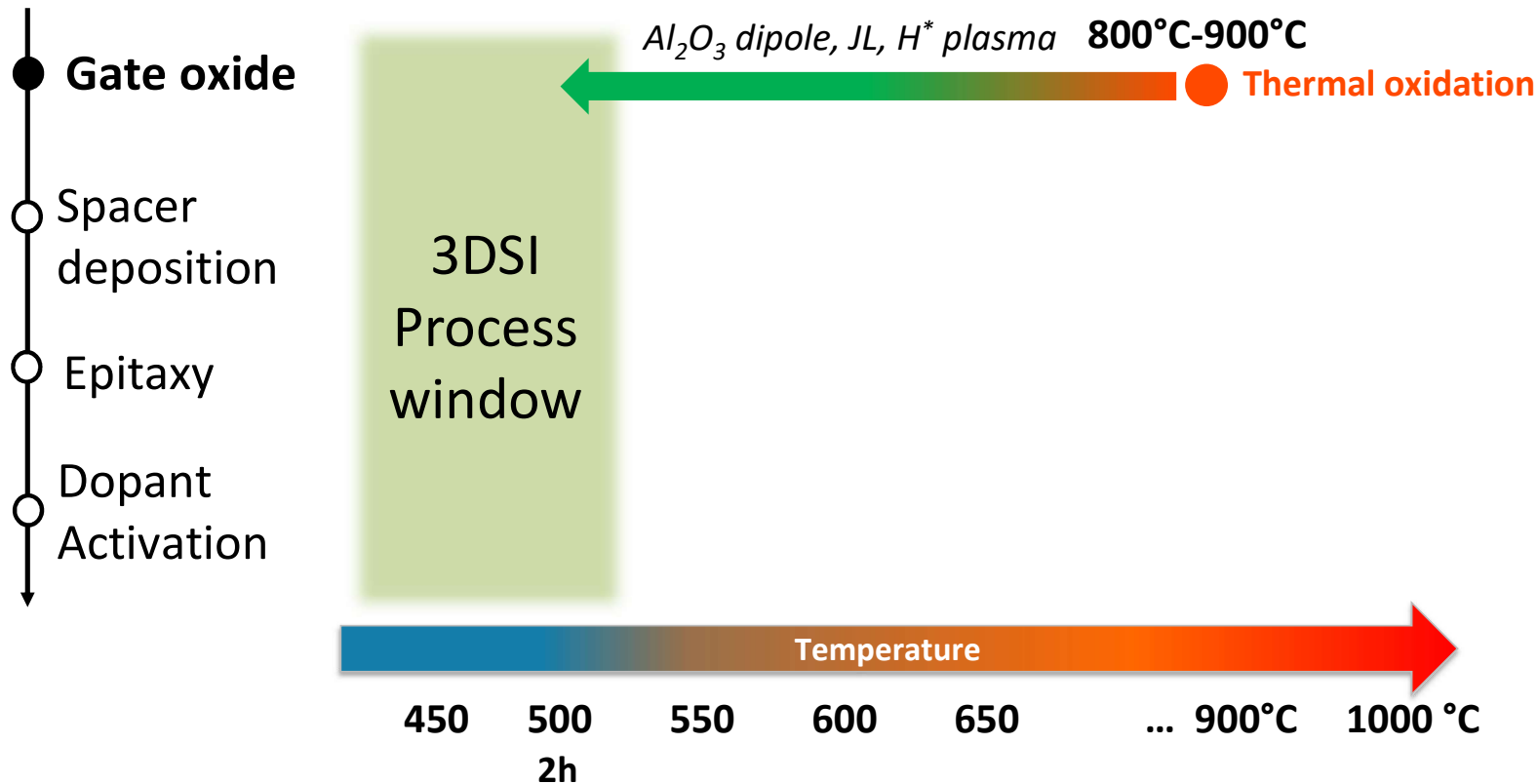


Highly-doped junctionless devices
Eox reduction in junctionless devices

J. Franco, VLSI 2018 (imec)

→ Investigations path have been identified to meet NBTI reliability targets at 525°C

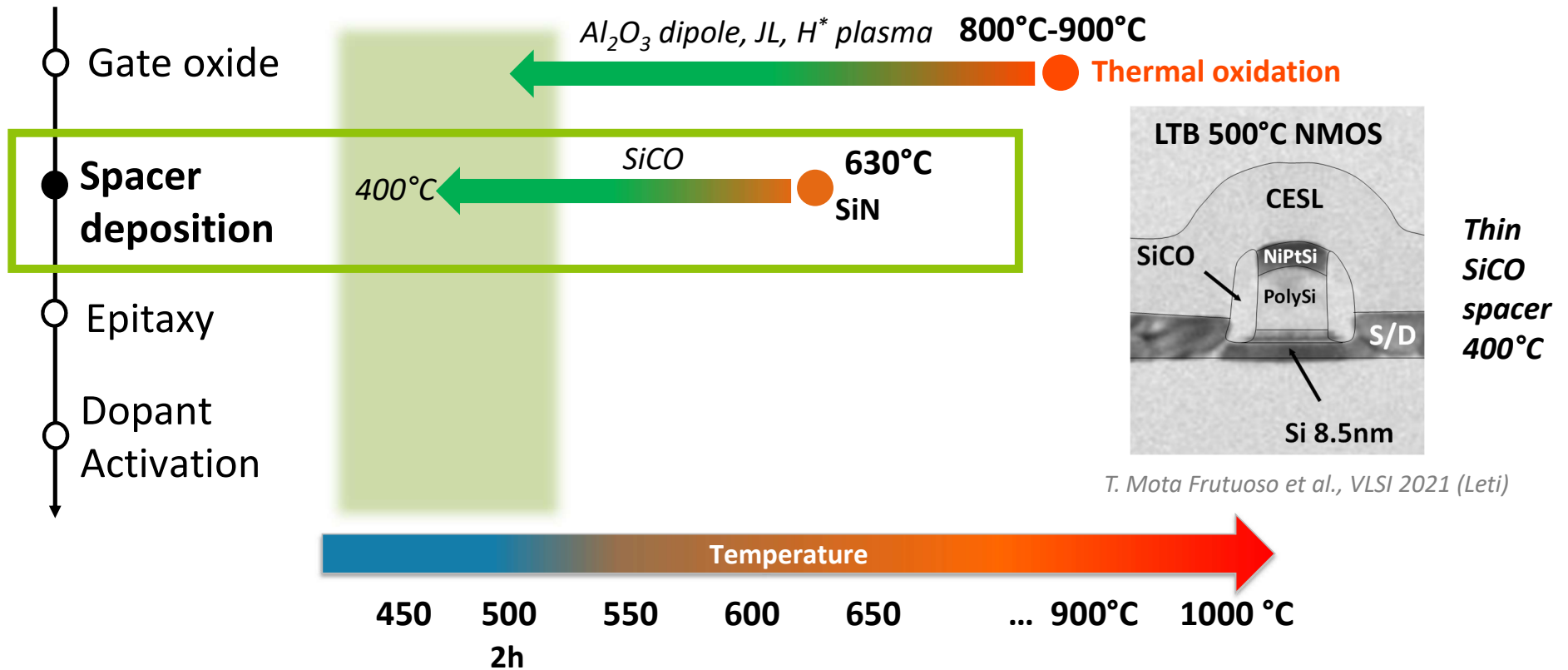
Summary on LT gate stack performance and reliability



→ Reducing TB of the gate oxide at 500°C is challenging mainly because of NBTI concern

→ But effective processes (dipole, H^* plasma) can be used to achieve an efficient and reliable gate stack

Low temperature process for Top Tier

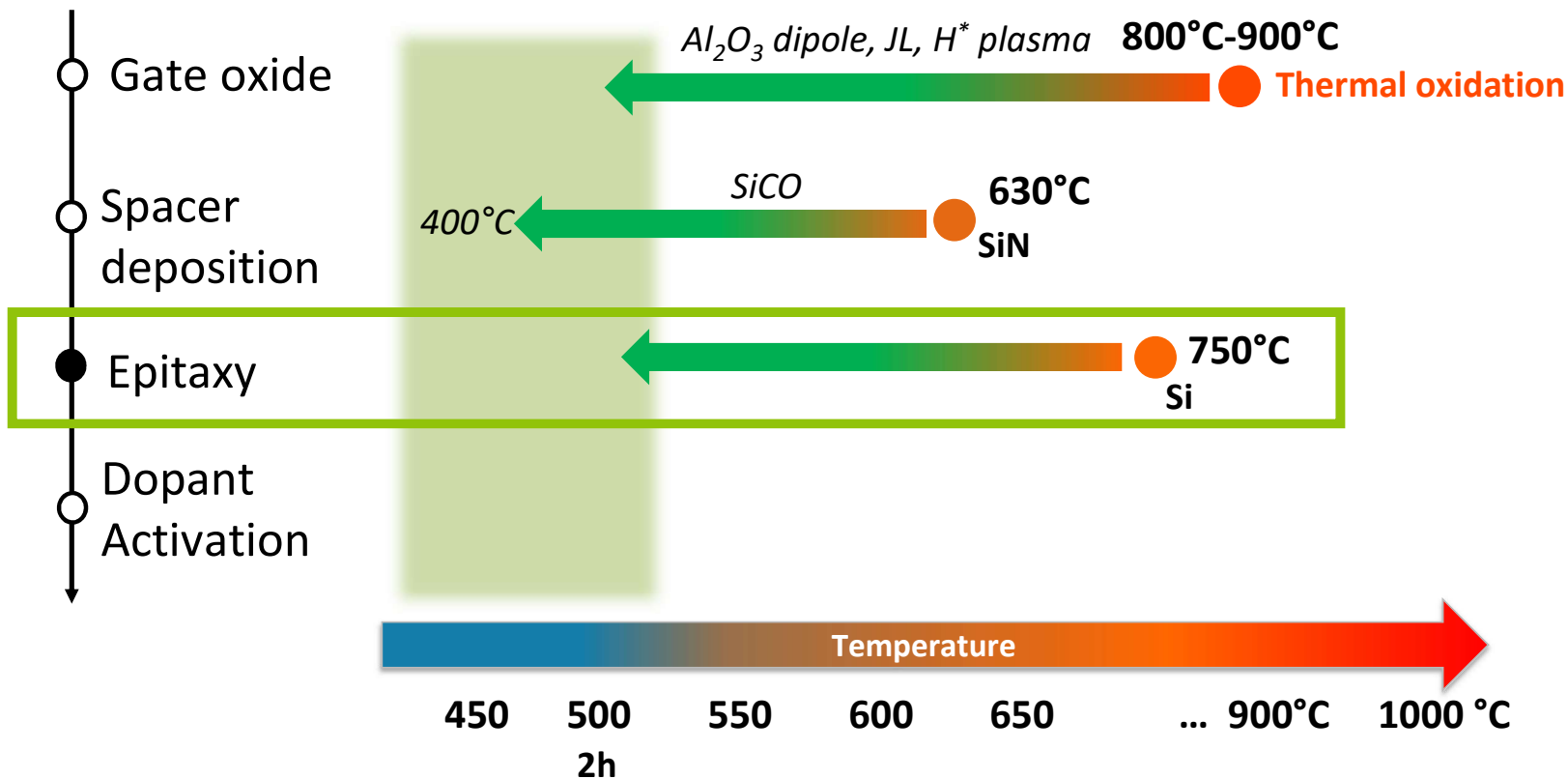


→ Low-k SiCO oxide deposited at 400°C can be used to replace 630°C SiN (see further)

Outline

- Introduction to 3D sequential integration
- Max thermal budget for the Top Tier
- Key process steps for a low temperature high performance 3DSi CMOS integration
 - Gate stack module
 - **Junction engineering**
 - Other processes required for RF applications
- Conclusion

Low temperature process for Top Tier

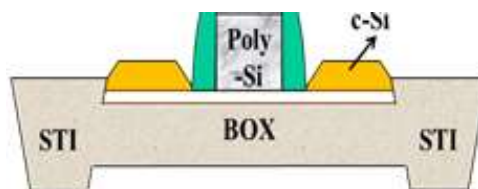


→ New developments to reduce the temperature of the Si epitaxy to 500°C

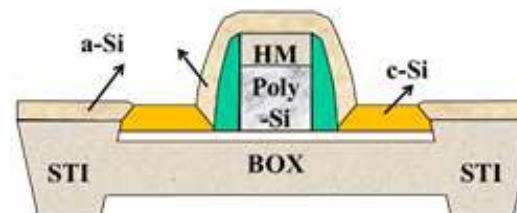
Low temperature epitaxy

	Standard selective Si epitaxy	$\leq 500^{\circ}\text{C}$ Si selective epitaxy
Surface preparation	HF last + bake (650°C and 800°C)	New strategy to be efficient at 500°C Siconi process removes surface oxide / in situ clean prior to epitaxy
Deposition precursor	DCS, SiH_4 , Si_2H_6 , and GeH_4	New precursors to obtain deposition rate of $\sim 1\text{nm}/\text{min}$ at 500°C
Epitaxy process	Coflow recipe: dep & etch at the same time	Cyclic and Deposition Etch (CDE) Poly Si gates Hard Mask introduction

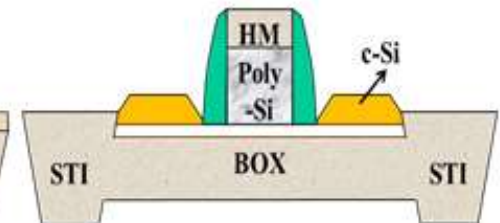
Selective Deposition



Non selective Deposition

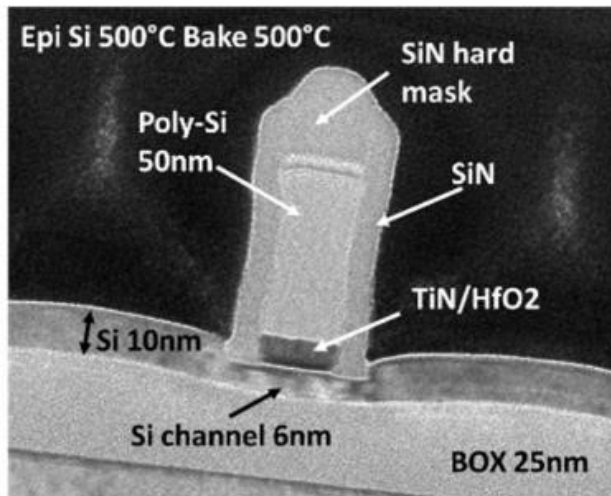


Selective a-Si etching



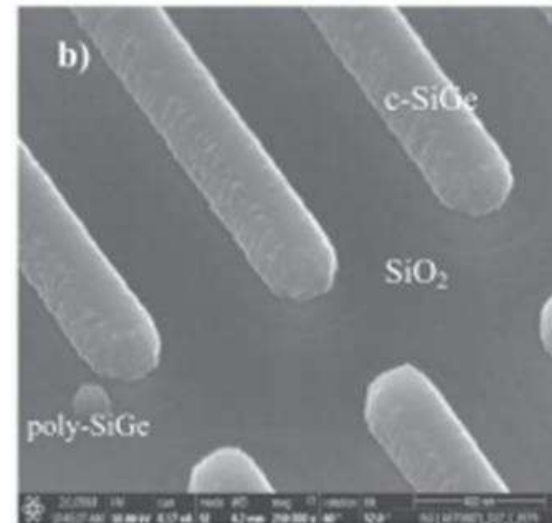
Low temperature epitaxy results

Si selective epitaxy



L. Brunet et al., IEDM 2018 (Leti, Applied Materials)

SiGe:B selective epitaxy

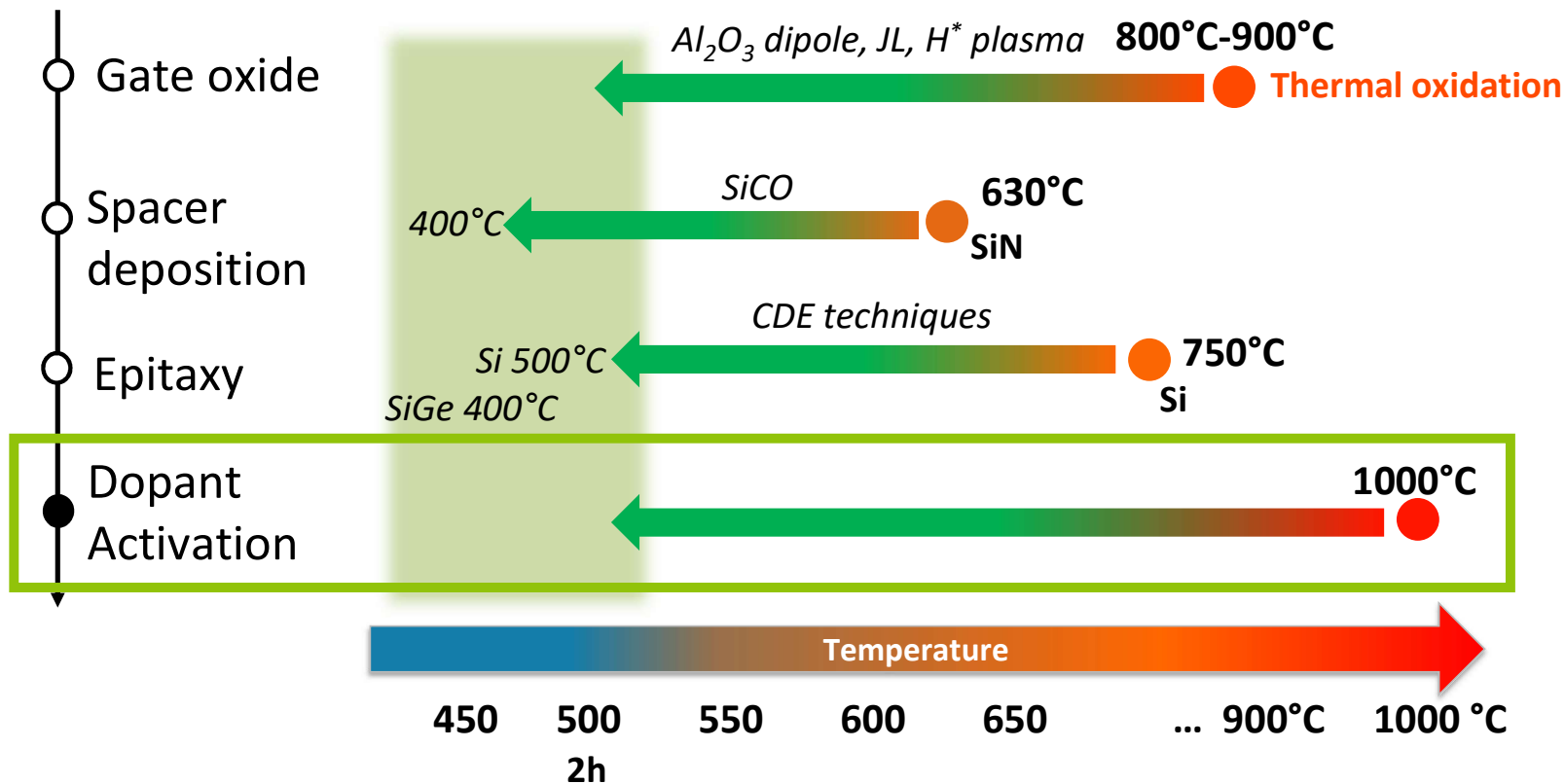


A. Hikavy et al., Semicond. Sci. Technol. 2019 (imec)

Si epitaxy at 500°C (including surface preparation) is demonstrated

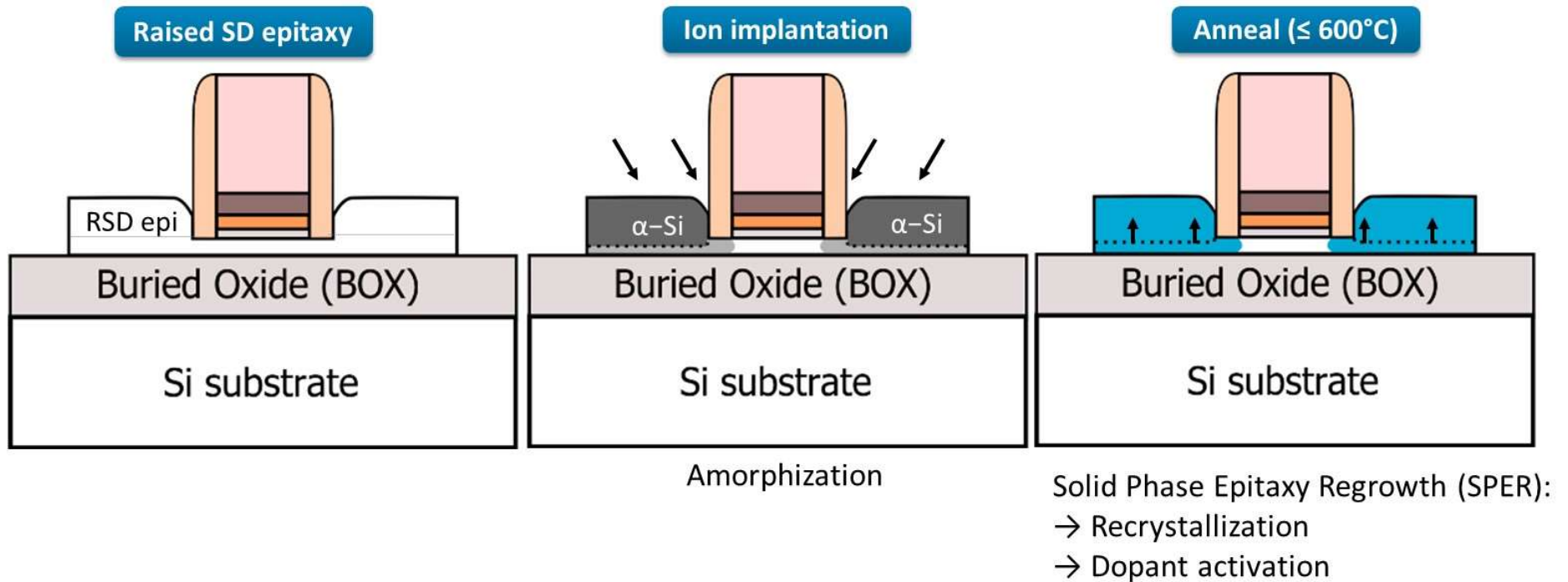
$\text{Si}_{0,3}\text{Ge}_{0,7}:\text{B} \ \& \ \text{P}$ epitaxy can be demonstrated at 400°C

Low temperature process for Top Tier



→ New developments to reduce the temperature of the Si epitaxy to 500°C

Solid Phase Epitaxy Regrowth - extension last « Xlast »

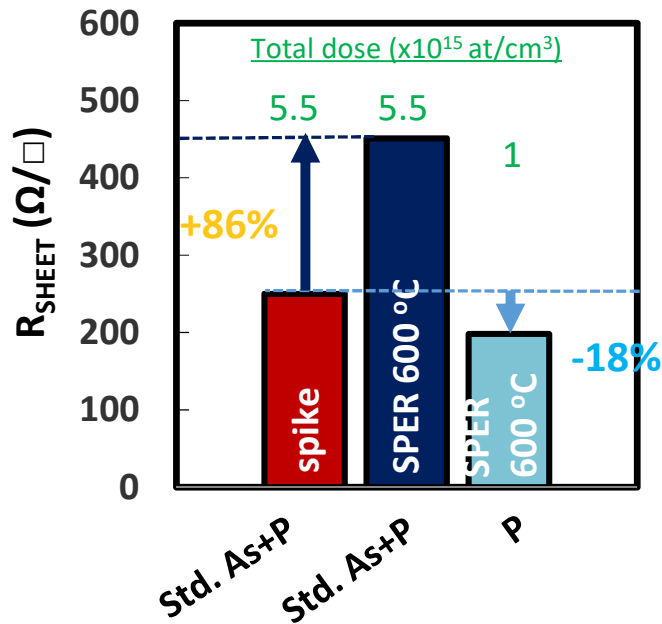


Junction formation → amorphization + SPER ($450^\circ\text{C} \leq T \leq 600^\circ\text{C}$)

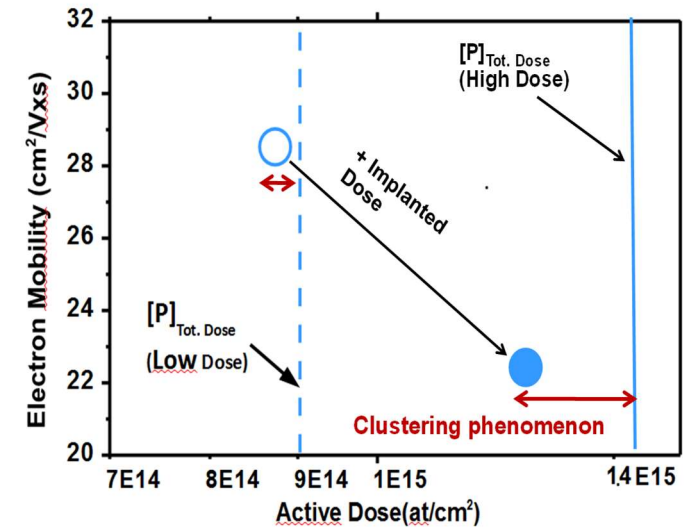
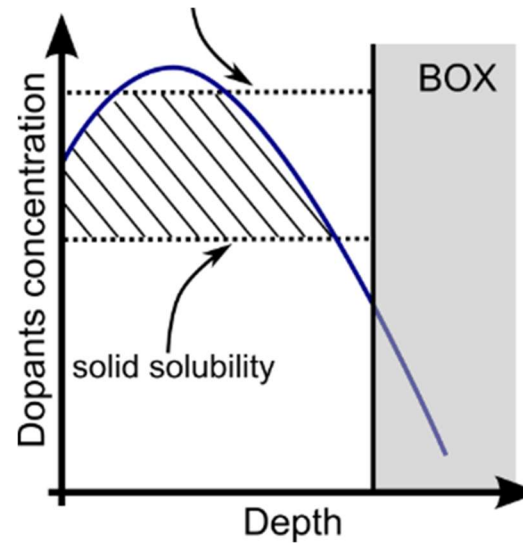
Main issue : lateral diffusion under the gate (overlap) → Access resistance optimization

High activation only in recrystallized region → Minimize Tseed

SPER activation

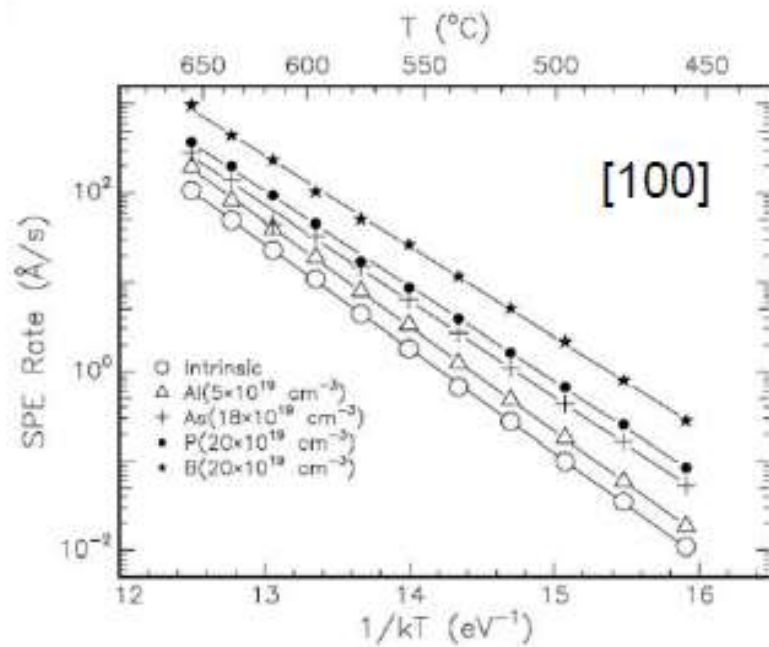


L. Pasini et al., IWJT 2014 (Leti)

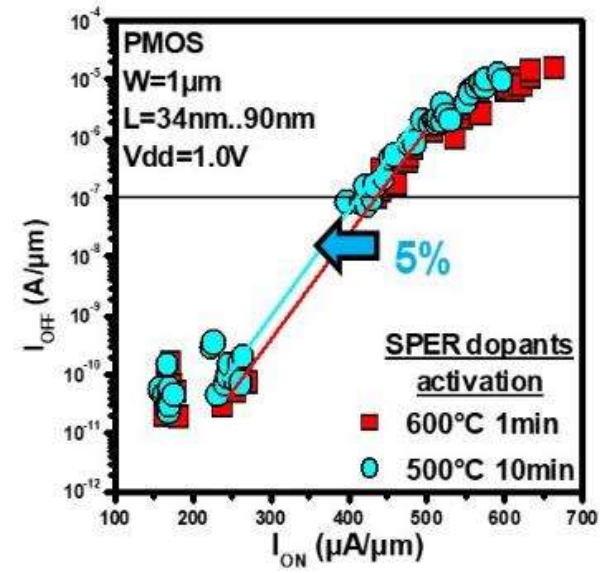


Doping profile need to be optimized due to weak diffusion & clusterization limit
 $C_{\text{Clusterization@ } 600^\circ\text{C}} \sim 3 \times 10^{20}$ at/cm 3 for Boron and $\sim 6 \times 10^{20}$ at/cm 3 for Phosphorous

Reducing SPER temperature



B-C. Johnson et al., Phys Rev B 2007

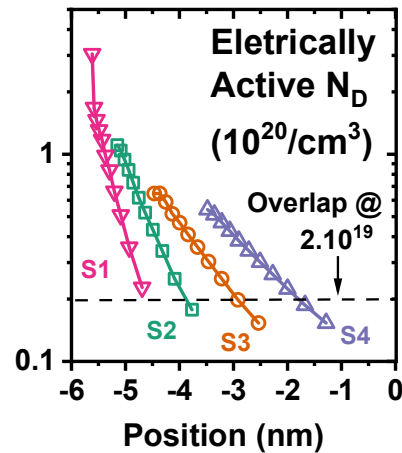
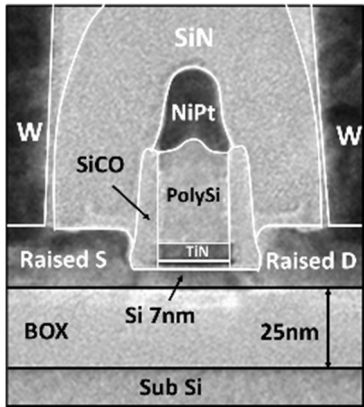


<100> oriented channel

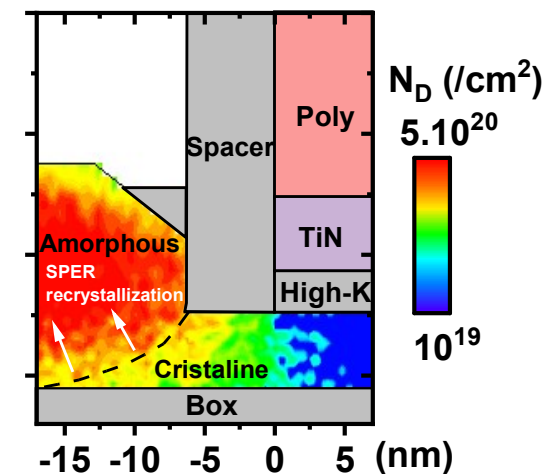
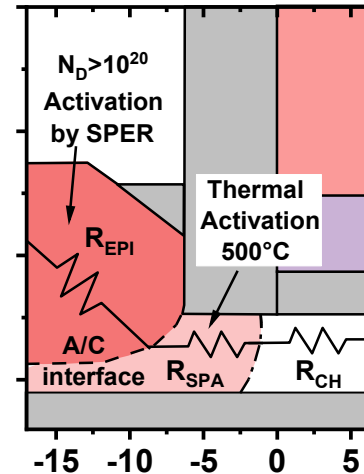
V. Lu et al., VLSI 2017 (Leti)

SPER rate depends on temperature, orientation, impurity type and concentration
SPER activation at 500°C validated on FDSOI devices

Junction optimization using SPER & Thermal Activation



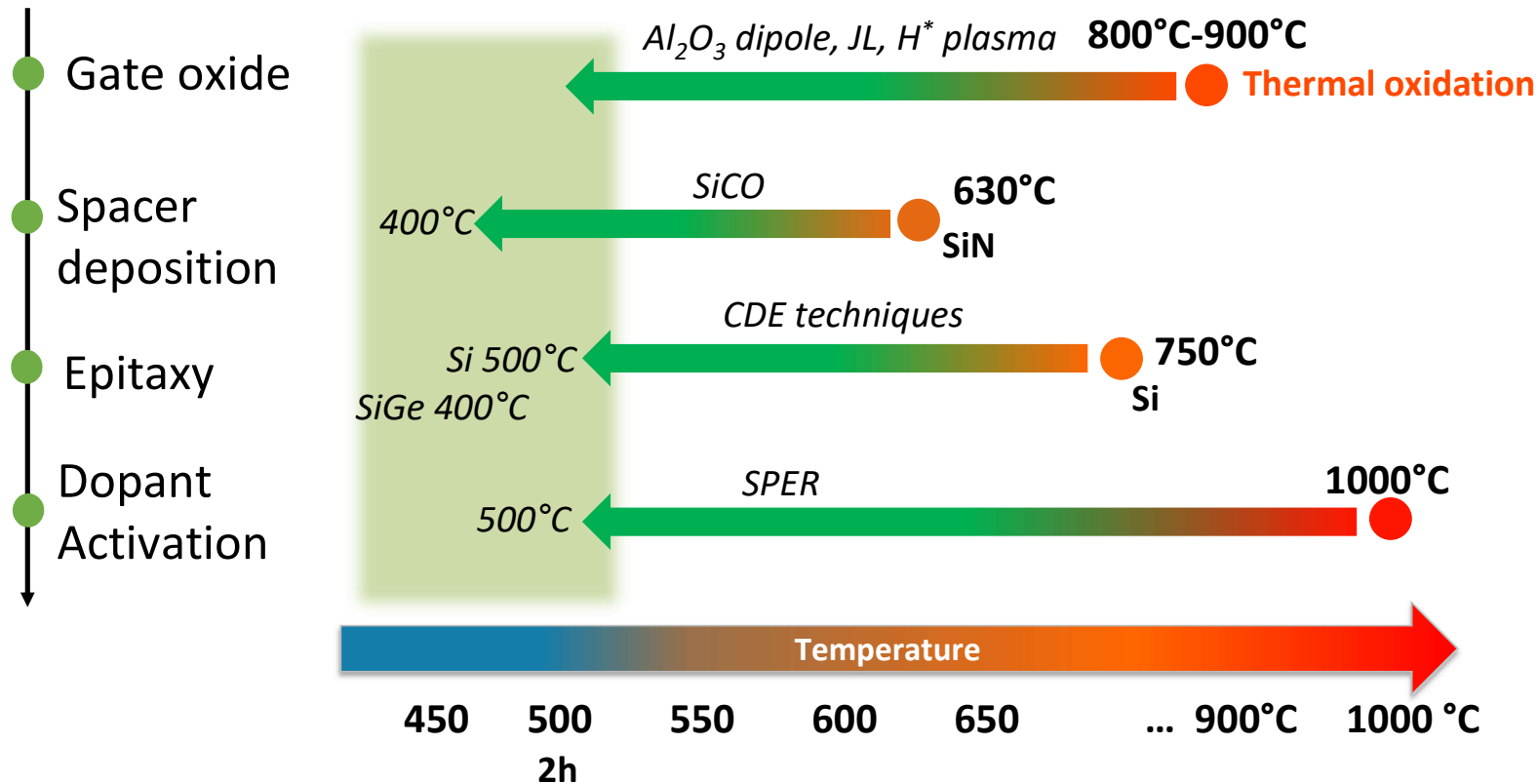
P imp.	Dose	Energy
S1	Low	Medium
S2	Medium	Low
S3	Medium	Medium
S4	Medium	High
S5	High	High



T. Mota Frutoso et al., VLSI 2022 (Leti)

→ Strategies to optimize junction profiles at $T > 500^\circ\text{C}$ → see student paper VLSI'22

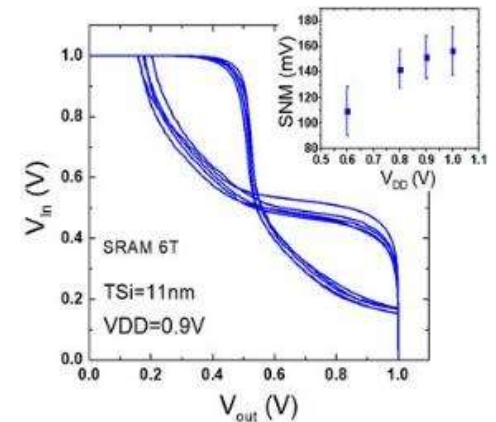
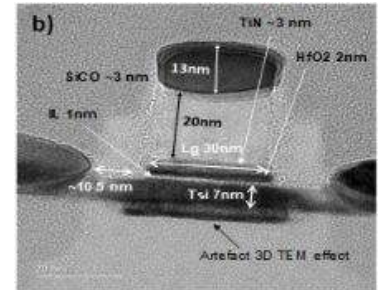
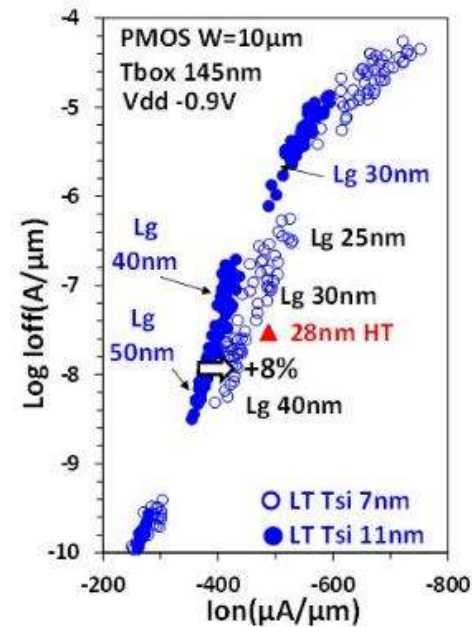
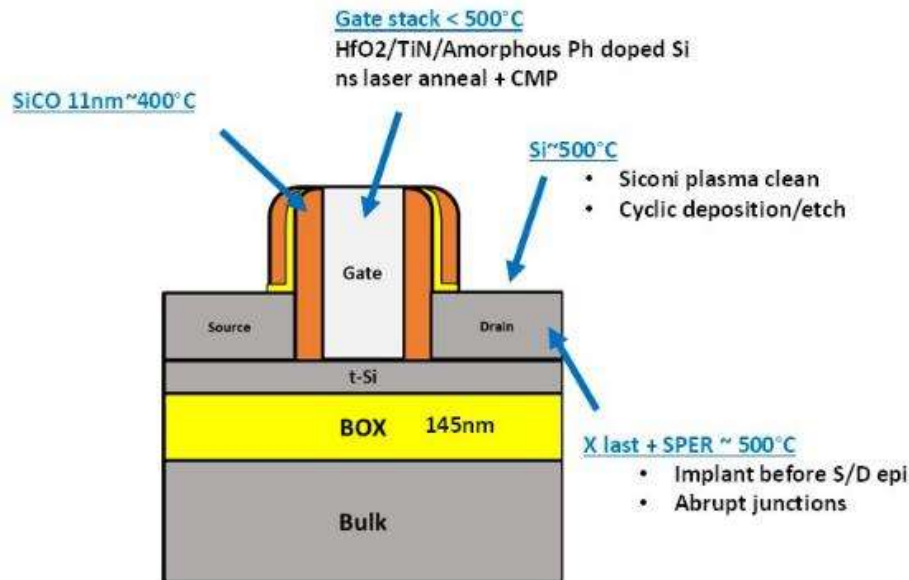
Low temperature process for Top Tier



→ New developments to reduce the temperature of the Si epitaxy to 500°C

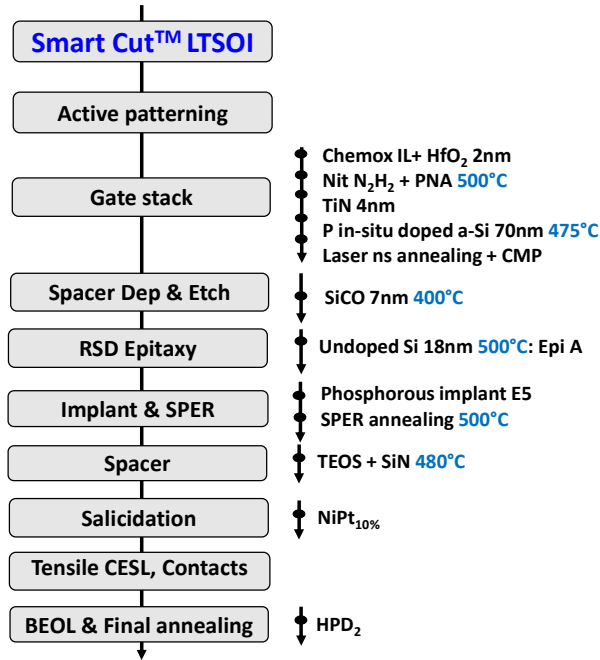
1st full 500°C CMOS FDSOI transistors

C. Fenouillet-Beranger et al., VLSI 2020 (Leti/Samsung)



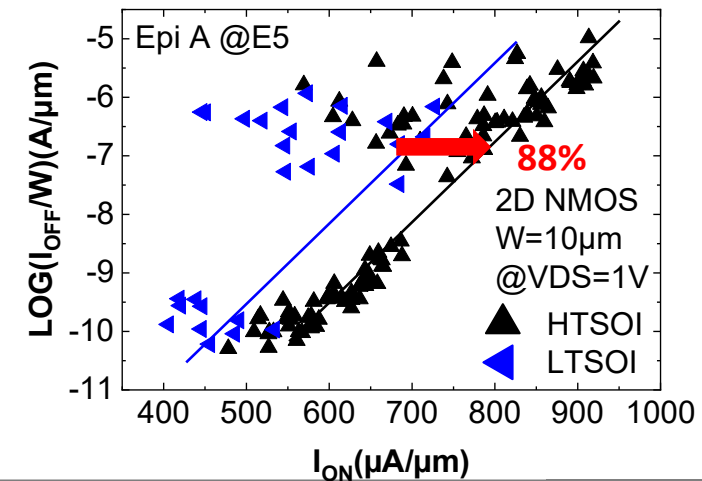
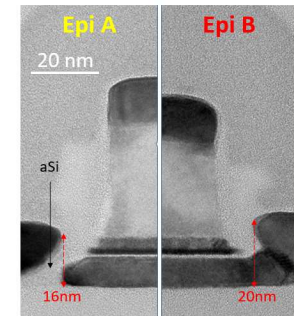
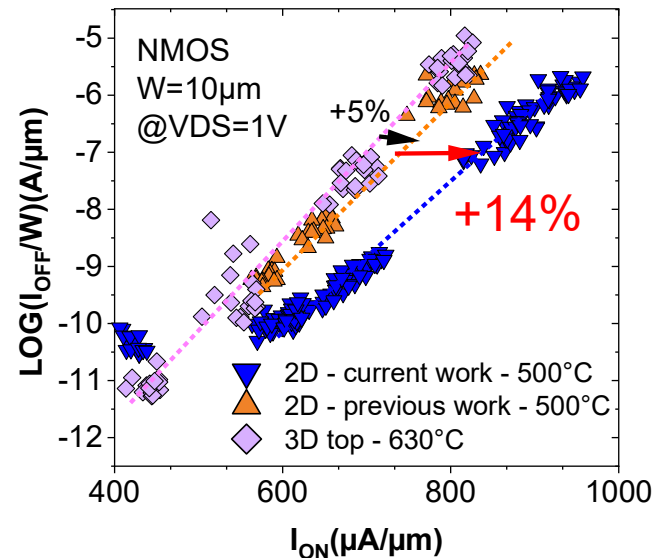
Full low temperature process for FDSOI devices ready
First functional CMOS FDSOI devices
RO and SRAM bitcell @ 500°C

Full 500°C NMOS FDSOI transistors on LTSOI substrate



L. Brunet et al., IEEE VLSI 2021 (Leti)

Comparison to previous work



At equivalent RSD thickness & Implantation energy, optimized RSD epitaxy with less facet (Epi B) allows a clear yield & performance increase
LT integration on LTSOI at 88% of the HT substrate reference

Outline

- Introduction to 3D sequential integration
- Max thermal budget for the Top Tier
- Key process steps for a low temperature high performance 3DSi CMOS integration
 - Gate oxide
 - Junction engineering
 - **Other processes required for RF applications**
- Conclusion

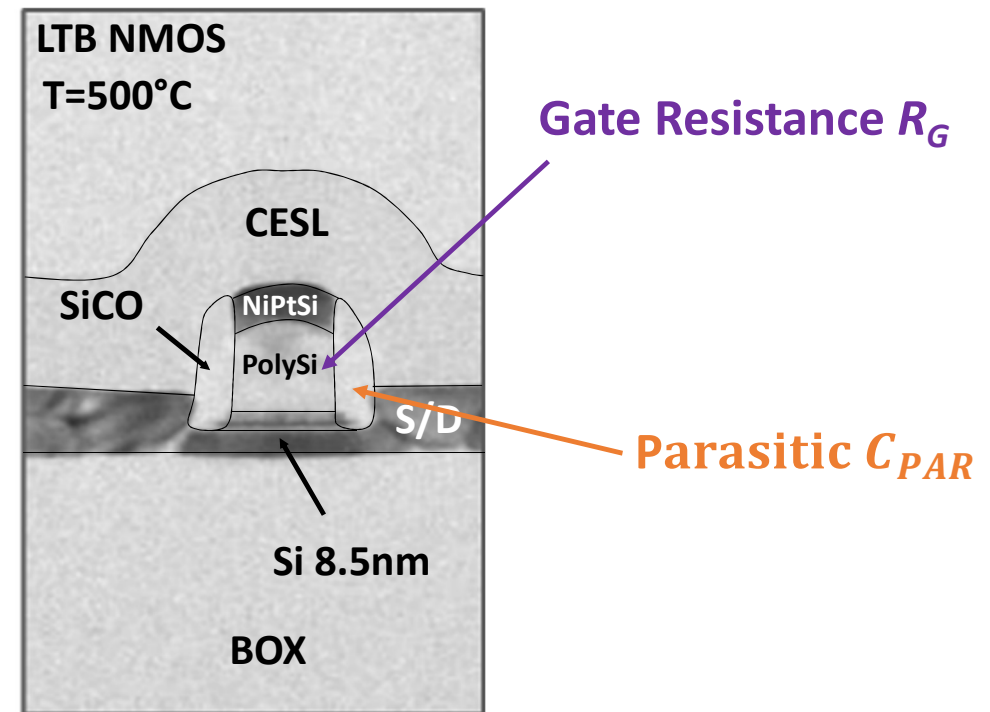
Other challenges for RF applications

RF FOMs

$$f_T = \frac{g_M}{2\pi \cdot C_{GG}} \propto \frac{1}{1 + \frac{C_{PAR}}{C_{OX}}}$$

$$f_{max} = \frac{f_T}{2\sqrt{R_G(G_{DS} + 2\pi f_T C_{GD})}} \propto \frac{1}{\sqrt{R_G}}$$

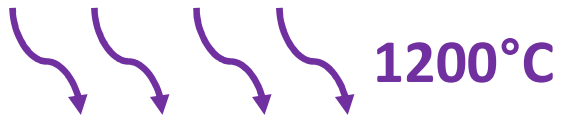
- also holds for dynamic operations in digital technologies



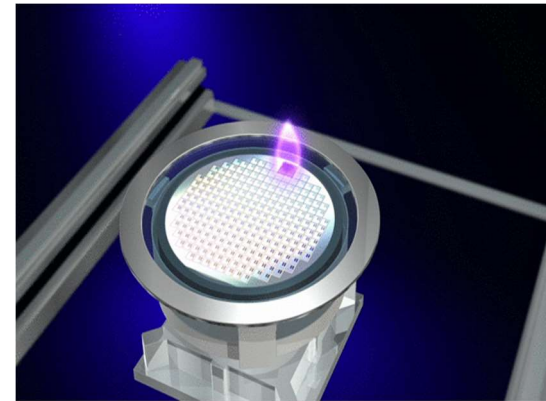
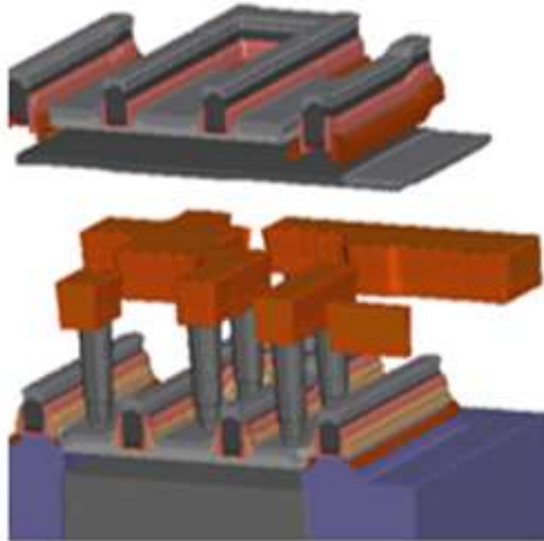
T. Mota Frutuoso et al., VLSI 2021 (Leti)

→ Must find solutions to reduce R_G and C_{PAR} at low temperature <500°C

Gate resistance reduction using ns Laser Anneal



Ex: Gate crystallization of the top tier

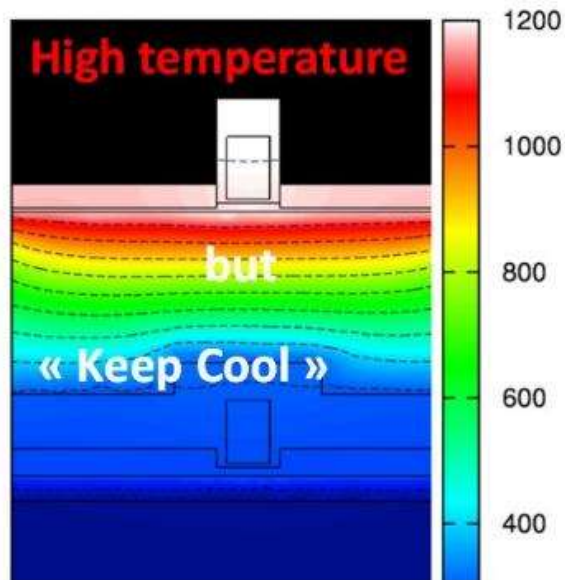


UV Nanosecond Laser Annealing (NLA)

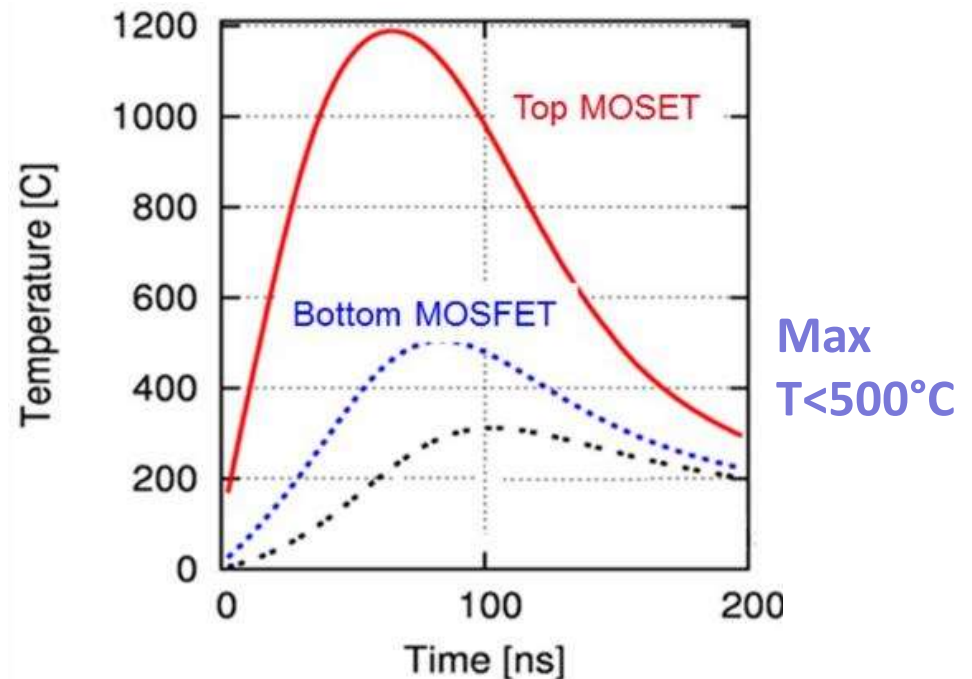
$\lambda = 308 \text{ nm}$, 160ns pulse duration

*L. Brunet et al, IEDM 2018; X. Garros et al., IEDM'19
S. Kerdiles et al, ECS Trans. 93, 2019.*

Interest of ns Laser Anneal – Local Annealing



C. Fenouillet-Beranger et al., IEDM 2014 (Leti, SCREEN-LASSE)



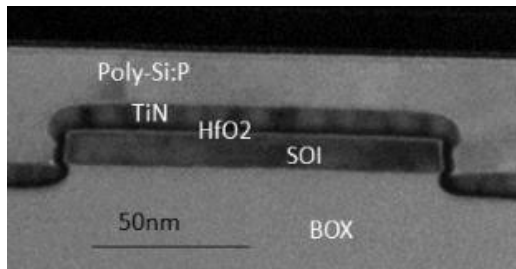
Main interest → preserves the stability of the Bottom Tier

Local laser anneal with 1200°C on top layer and <500°C on bottom layer is possible
UV laser (308nm) / 100ns pulse / Standard Interlayer dielectric (SiO₂) thickness₆₁

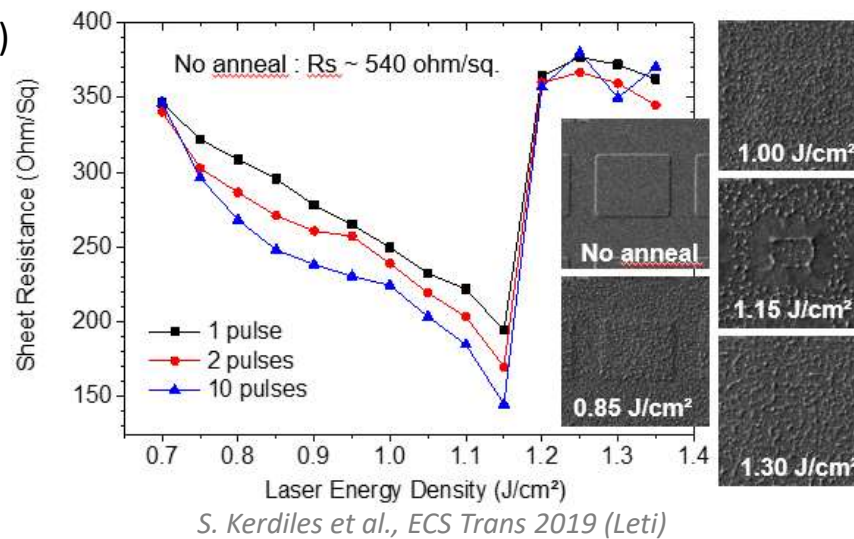
Gate resistance reduction using ns Laser Anneal

Amorphous in situ doped poly Si
melted by UV ns laser anneal

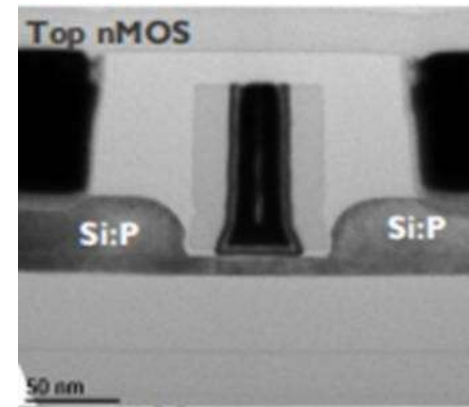
- Dopant activation
- Crystallization (100-300nm grain size)
- Post CMP required



L. Brunet et al., IEDM 2018 (Leti)



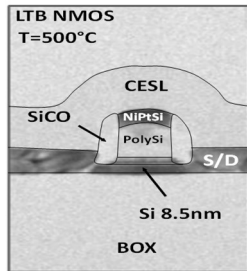
S. Kerdiles et al., ECS Trans 2019 (Leti)



A. Vandooren et al., VLSI 2018 (imec)

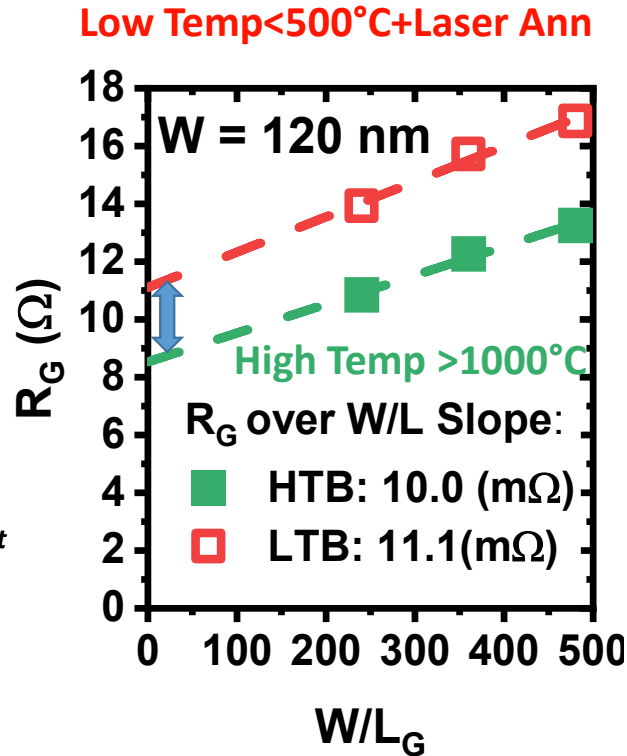
ns laser anneal is a potential solution for Poly gate stacks
Gate last process intrinsically offers low gate resistance

Gate resistance reduction using ns Laser Anneal

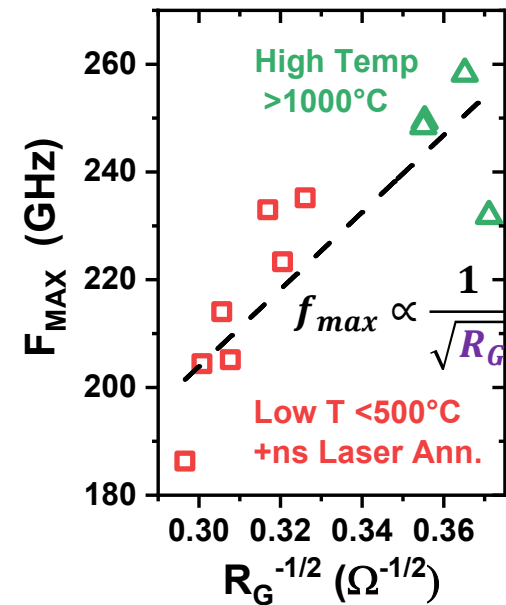
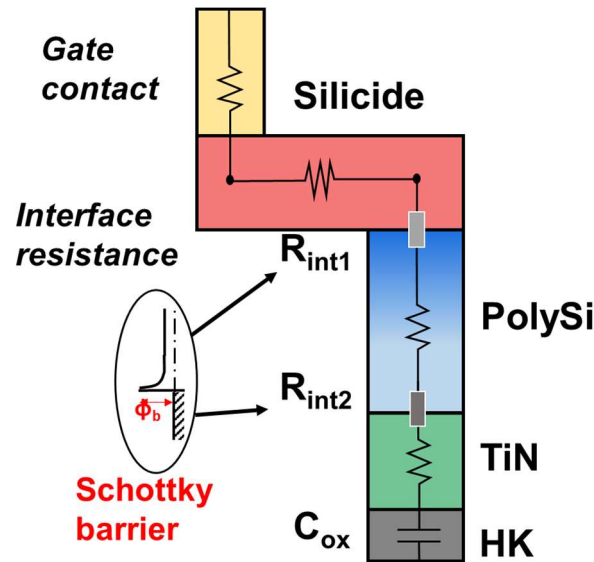


Same
slope $\approx R_{polySi}$

but $\neq$
Intercepts $\approx R_{int}$



T. Mota Frutuoso et al., VLSI 2021 (Leti)

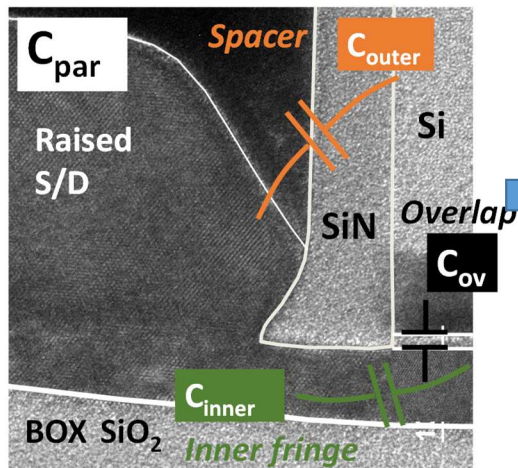


UV Laser anneal $\rightarrow$ allows to recover R_{polySi} of HT references
 $\rightarrow$ RF performance at $T=500^\circ$ close to HT references

Reduction of parasitic capacitances C_{par}

SiN spacer (630°C)

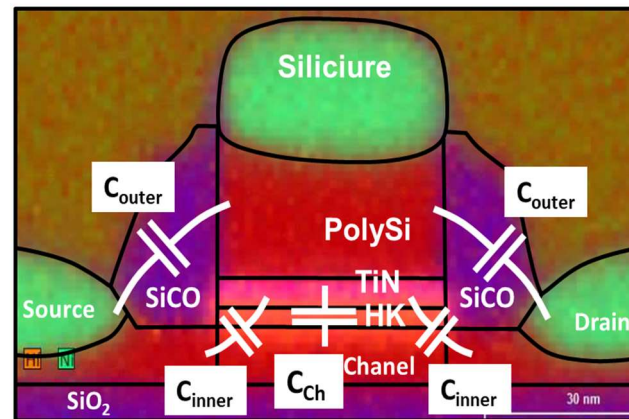
$$\epsilon_r SiN = 7.0$$



X. Garros et al., IEDM 2019 (Leti)

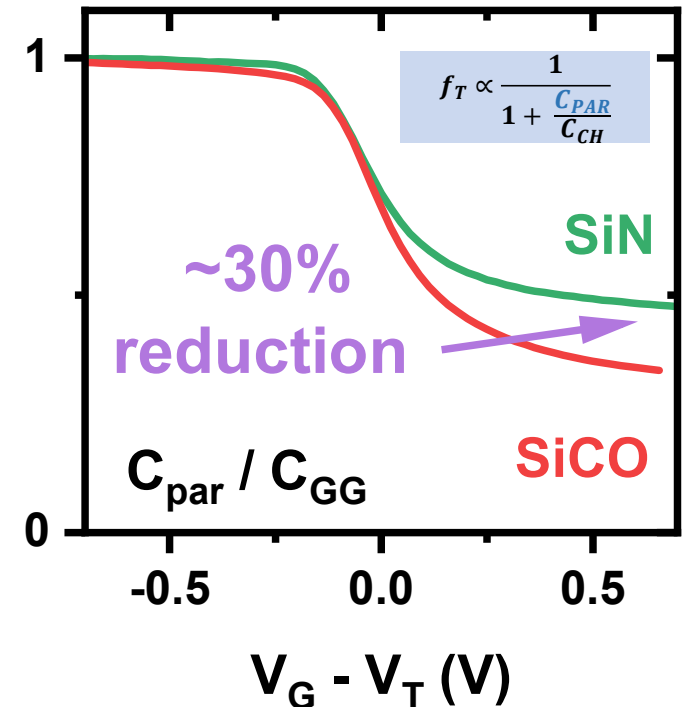
SiCO spacer (400°C)

$$\epsilon_r SiCO = 4.5$$



T. Mota Frutuoso et al., VLSI 2021 (Leti)

$$C_{par} = C_{outer} + C_{inner} + C_{ov}$$

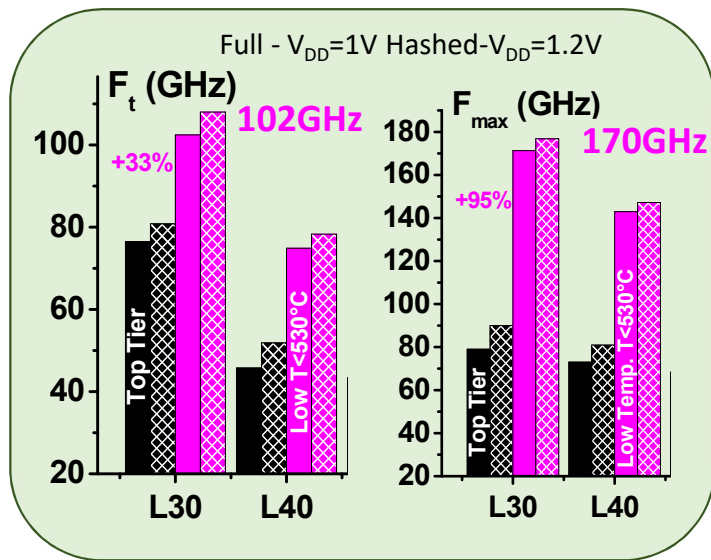


- Replacement of SiN spacer by SiCO oxide deposited at 400°C
- Reduction of parasitic capacitance C_{par} of $\sim 30\%$

RF performance of Si-based Low Temp. transistors

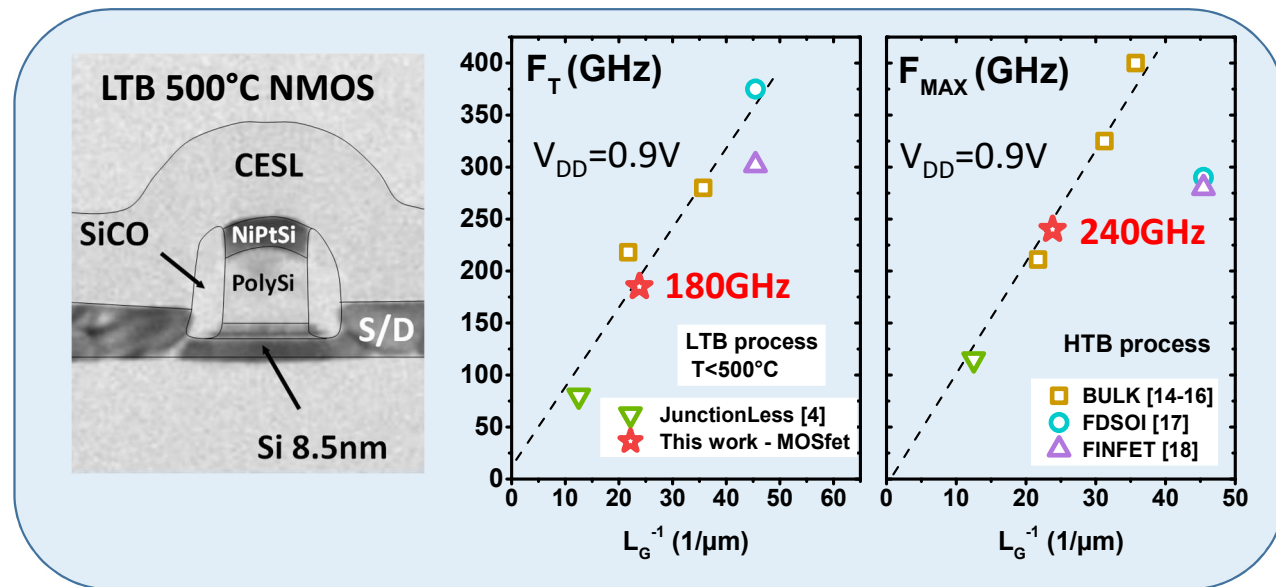
PMOS $T < 530^\circ\text{C}$

Digital



X. Garros et al., IEDM 2019 (Leti)

NMOS $T=500^\circ\text{C}$



T. Mota Frutuoso et al., VLSI 2021 (Leti)

→ Record RF performance for LTB technology, thanks to R_G & C_{par} reduction
 → already equivalent to Si-based HT references at same L_g

Outline

- Introduction to 3D sequential integration
- Max thermal budget for the Top Tier
- Key process steps for a low temperature high performance 3DSi CMOS integration
 - Gate stack module
 - Junction engineering
 - Other processes required for RF applications
- Conclusion

3D sequential motivations



Performance

CMOS over CMOS Wirelength reduction
Boost CMOS (N/P) with alternative channel materials

More Moore



Energy Efficiency

Near memory computing



Cost reduction

Smart partitioning
Peripheral functions : power gating



Smart Sensors

e.g. miniaturized sensor arrays

More than Moore

Top FET options diversity

2D materials
TMD, BN...

Oxide sc
IGZO, ITO...

CNT

Poly-Si

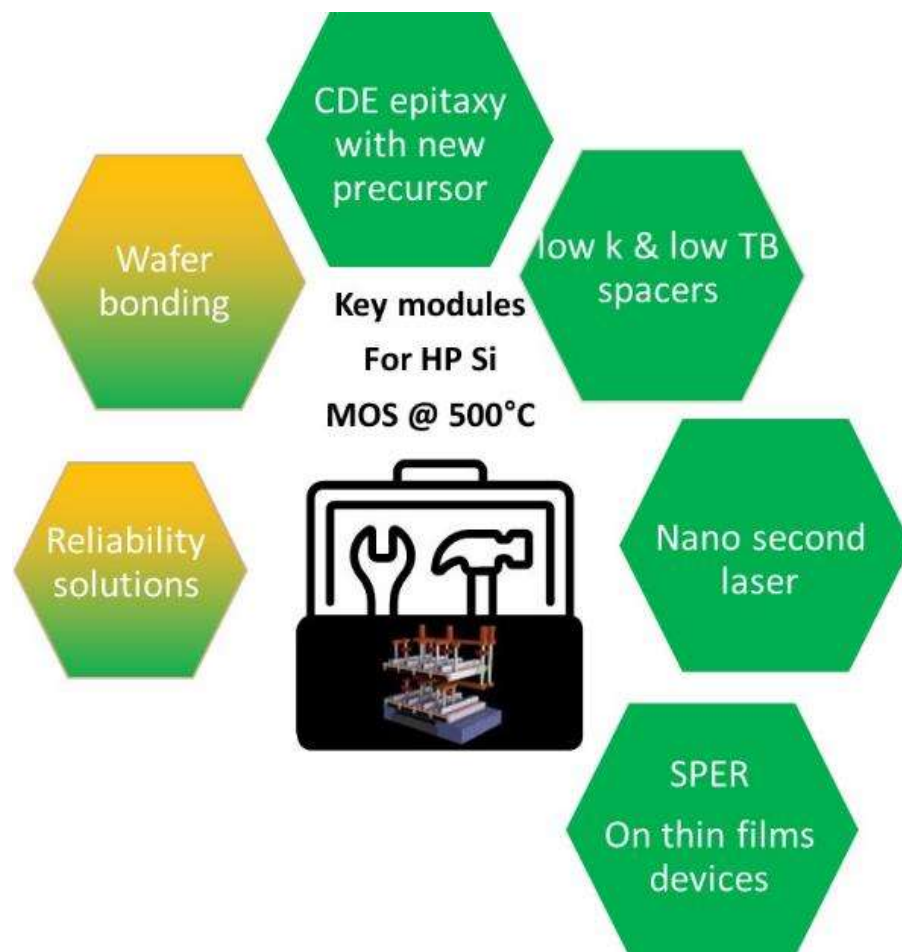
Mono-Si

High μ mat.
TMD

Summary of LT process integration

- LT 500°C tool BOX is ready and demonstrated
- 300mm 3D Si mono demonstrated with great performance (DC and RF)
- Full Low temperature 500°C 3D sequential with Si mono still to be demonstrated :
- Low temperature gate stack reliability still the main issue but solutions envisioned

	Introduction of Dipole between SiO ₂ and HfO ₂	Hydrogen treatment	J-Less transistor
NMOS	(Al ₂ O ₃) ++	++	++
PMOS	(LaSiOx) ++	++	++



Thank you for your attention

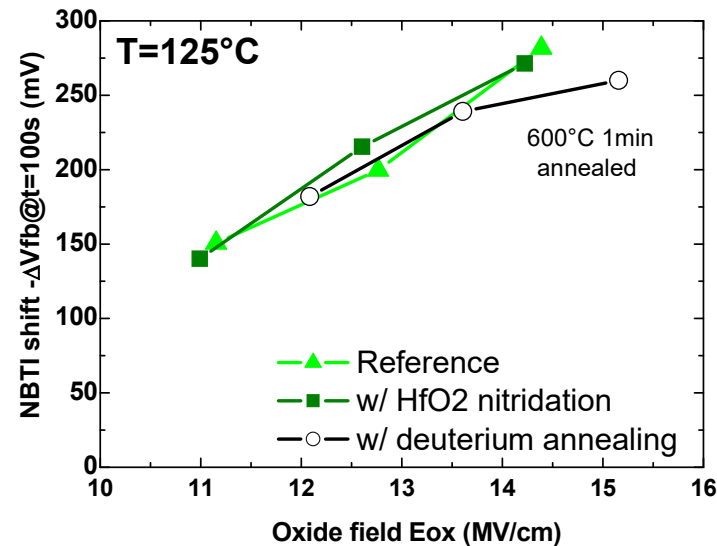
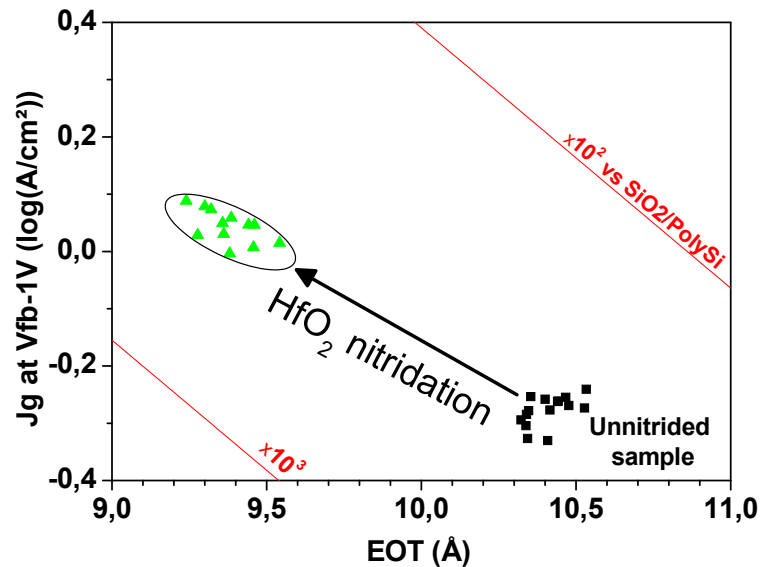
Thank you to all co-authors and colleagues that have been working on CoolCube™

in particular:

P. Batude, C. Fenouillet-Béranger, L. Brunet, D. Lattard, V. Lapras, F. Andrieu, M. Vinet, J. Arcamone
L. Brevard, M. Ribotta, B. Previtali, C. Tabone, F. Ponthenier, J.M. Pedini, A. Magalhaes-Luca, N. Rambal, E. Arnoux
C. Cavalcante, T. Mota-Frutoso, A. Tsiara, C-V. Lu, L. Pasini, F. Piegas Luce, F. Deprat, D. Bosch, P. Sideris, J. Micout, C. Xu, S. Beaurepaire
M. Casse, C. Theodorou, J. Lugo, B. Sklenard, B. Mathieu, J. Lacord
R. Gassilloud, P. Besson, F. Fournel, S. Kerdiles, P. Acosta-Alba, V. Mazzocchi, J-M. Hartmann, J. Kanyandekwe, F. Mazen, C. Guerin, C. Vizioz, A. Tavernier
S. Thuries, O. Billoint, P. Vivet, S. Cheramy, G. Sicard, G. Cibrario, M. Mouhdach, B. Giraud
X. Federspiel, D. Ney, P-O. Sassoulas

HfO₂ plasma nitridation for EOT reduction

HfO₂ nitridation in N₂/H₂ ambient at 250°C + PNA at 600°C 2min



Plasma nitridation
N₂/H₂

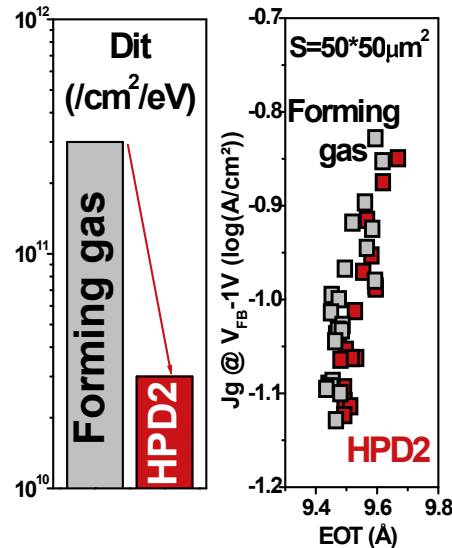
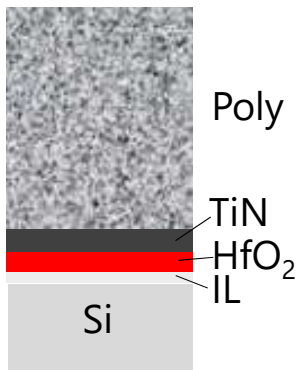


V. Lu et al., IEEE SISC 2015 (Leti)

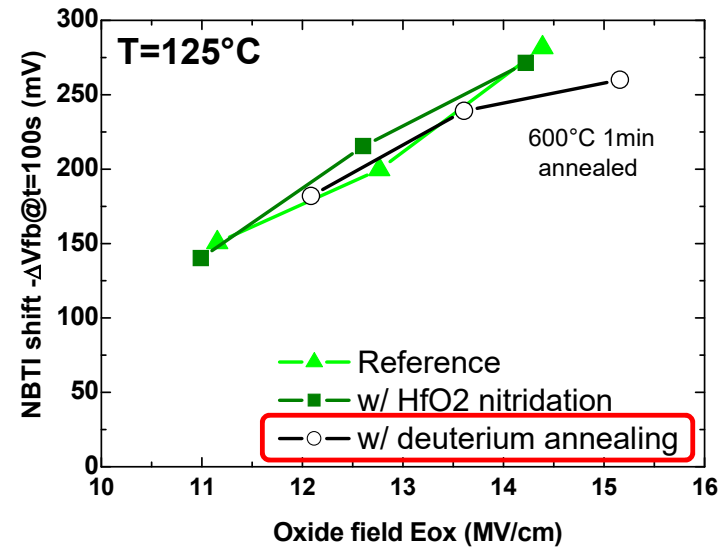
- Gain of ~1Å EOT thanks to thinner IL with incorporation of N
- But no NBTI reliability improvement

Forming gas Deuterium annealing

Digital device
LT gate stack



A. Tsiara IEEE VLSI 2018 (Leti)

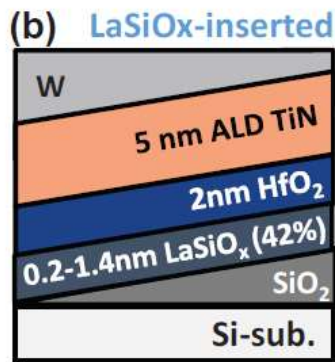


V. Lu et al., IEEE SISC 2015 (Leti)

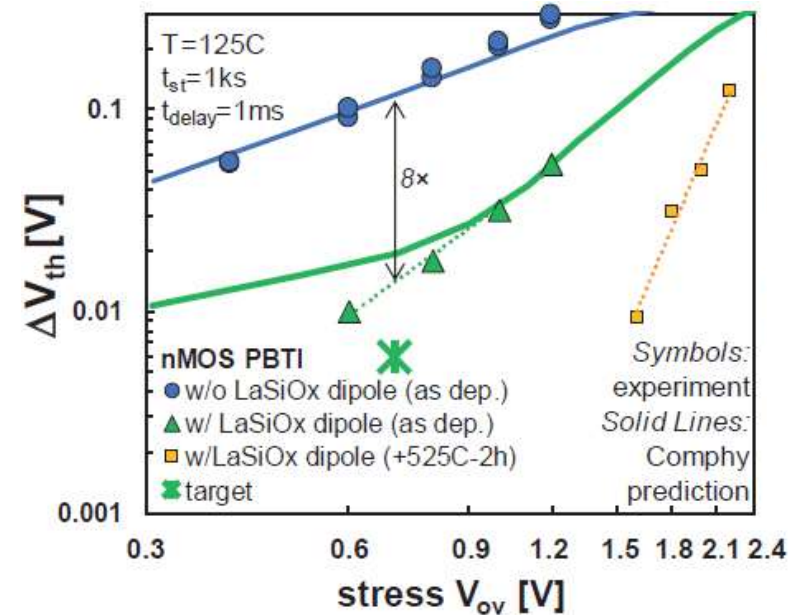
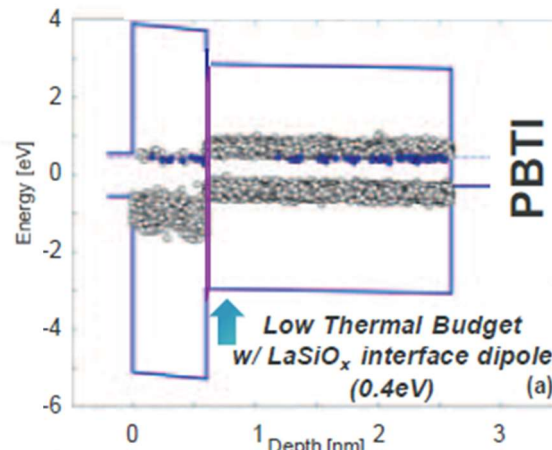
High Pressure Deuterium Anneal is efficient to heal interface traps on LT gate stack
→ allows to reach LFN requirements but no NBTI reliability improvement

PBTI reliability solutions

LaSiOx Dipole insertion between SiO₂ and HfO₂



J. Franco, IEEE IRPS 2017 (imec)



J. Franco, IEDM 2018 (imec)

Up Shift of V_{fb} 0.4eV with LaSiOx for PBTI improvement
V_{TH} reduction

→ Investigations path have been identified to meet NBTI reliability targets at 525°C