RF and mmW test activities at CEA-Leti

José Luis Gonzalez Jimenez, Christopher Mounet

Special Session on RF/5G Test

William R. Eisenstadt
Department of Electrial Engineering
University of Florida
Gainesville, FL, USA
wre@tec.ufl.edu

Manuel J. Barragan[1], Gildas Leger[2], Florent Cilici[3], Estelle Lauga-Larroze[1], Salvador Mir[1], Sylvain Bourdel[1]
[1]Univ. Grenoble Alpes, CNRS
Grenoble INP, TIMA
Grenoble, France
[2]IMSE-CNM, CSIC,
Universidad de Sevilla
Sevilla, Spain
[3]NXP,
Toulouse, France
manuel.barragan@univ-grenoble-alpes.fr

Mark Roos and Devin Morris
Roos Insruments
Santa Clara, CA, USA
mroos@roos.com

Marc Margalef-Rovira[1], Issa Alaji[1], Haitham Ghanem[1], Guillaume Ducournau[1], and Christophe Gaquiere[2]
[1]Univ. Lille, CNRS, Centrale Lille, Yncrea Lille
Univ. Polytechnique Hauts-de-France
Lille, France
[2]MC2-Technologies
Villeneuve-d'Ascq, France
marc.margalef-rovira@univ-grenoble-alpes.fr

José Luis GONZÁLEZ-JIMÉNEZ and Christopery MOUNET
Grenoble-Alpes University
CEA-Leti,
Grenoble, France
JoseLuis.GONZALEZJIMENEZ@cea.fr

Challenges of 5G Production Test

Mark Roos and Devin Morris

I. Introduction

The advent of 5G devices has placed greater importance on RF test and qualification in production test. The test cell incorporates many more microwave test resources in terms of both the test equipment but more specifically the interface between the tester and the device-under-test. The design of this interface is moving away from traditional multi-layer PCBs toward an integrated microwave test bench that incorporates traditional microwave cables and connectors as well as off-the-shelf microwave components. This microwave environment is more conducive to a conventional vector calibration scheme that can be cascaded across the different layers of the test system including the individual instruments, the specific configuration and the interface. This provides more flexibility in the setup in terms of frequency capability and increased measurement ports.

The increased performance requirements and challenges of higher frequencies are pushing the test industry to respond with novel and more comprehensive solutions to help bring 5G devices to market.

Our presentation will discuss the unique requirements, challenges and production test solutions of three examples: (1) Sub-6GHz 5G test, (2) 5G NR up to 30GHz and (3) Future 5G, the so called 5G+ or 6G. The presentation will be a comprehensive review of the topics we have listed.

978-1-6654-6706-3/22/$31.00 ©2022 IEEE

RF and mmW test activities at CEA-Leti

José Luis GONZÁLEZ-JIMÉNEZ and Christopher MOUNET

II. Introduction

Leti is one of the three institutes of the Technology Research and Development branch of (French's Commissariat à l'Enérgie Atomique et aux Enérgies Alternatives). It has been at the core of the development of microelectronic and nanoelectronic technologies in France and its major role is to fill the gap between fundamental/academic research and industry. It employs 2000 people in Grenoble, France and operates 10000 m^2 of cleanrooms. This talk is focused on the RF and mmW test activities developed at the RFIC Design and Test laboratories of Leti.

The specific role that the Leti plays in the technology transfer chain determines the test activities and the expertise developed during the last decades at our two laboratories. Our teams handle two different types of projects. In the first one, proof of concept and early ideas are implement in prototypes consisting in packaged or wafer-level RFICs developed mostly in CMOS and BiCMOS nodes for RF applications. In some cases, these prototypes are mounted on validation boards or modules including other components such at antennas or external sensors. This type of developments usually attain TRL 4 or 5. Some of these prototypes could evolve to higher maturity levels in the framework of industrial research and development projects that is the second type of project in which our teams work. In that case, some of the circuit developed could attain the product or pre-product level (TRL 7 to 9). For this second type of project we are usually concerned by industrial test development and we deliver volumes in the order of 10 000 good dies to our customers.

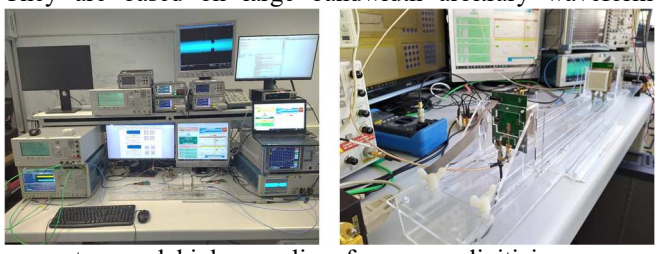
III. Industrial test equipment at Leti

Our test laboratory is equipped with an Advantest V93000 tester (see Figure 1) combined with an automatic prober (for on-wafer test) and a pick and place handler (for final test in package), that can be used for production test. Our teams have developed specific testing methodologies around this equipment in order to apply test routines adapted to two different type of RF products. For low volume products with high added value, the focus is put on high yield and test coverage. In that case, for frequencies up to a few GHz fully functional tests are performed, arriving up to measure of the EVM (error vector magnitude) of modulated signal. This type of test requires longer test times, but can be accepted in this case. For the second type of RF products for cost-driven markets, test time could be a significant contributor of the product cost and therefore simplified test routines are developed trying to capture the RF performance from simpler test signals at DC or lower frequencies.

Figure 1. Industrial test equipment at CEA-Leti.

IV. Specific Challenges of mmW Testing

Even for low volume testing, frequencies in the mmW range pose an important constraint on test strategies since most of industrial testers do not have enough frequency BW to directly measure the highest frequency nodes of mmW circuits. Current 5G and 5G+ standards are using frequencies in the range 28 to 40 GHz, and higher frequencies above 100 GHz are being proposed for the front and back-haul section of the network. In that case, the test strategy should be anticipated early during the design phases. Furthermore, functional test could become prohibitive in terms of test time due to the complex modulation types and frame duration involved. This is the way hardware in the loop validation platform, as the one shown in Figure 2, have been developed. The hardware in the loop validation platforms are designed in a flexible way so that several parts of the RF transceiver can be tested individually, the rest of the transceiver being replaced by off-the-shelf components and lab equipment. They are based on large bandwidth arbitrary waveform



generators and high sampling frequency digitizing scopes. The complete physical layer can be run off-line so that the full link including the device under test (DUT) is validated. This approach allows correlating circuit level variables (internal DC voltages or other DC or low frequency signatures) with link level figures of merit such as EVM or BER. This information is used in the industrialization phase of those prototypes to optimize the testing approach. In addition, this information is also used to implement calibration and self-healing strategies, the later required in some specific applications such as harsh environment equipment or space electronics.

Figure 2. Example of hardware-in-the loop test and validation platform for 140 GHz circuitry.

In addition to the high RF frequency of 5G, 5G+ and future 6G systems, the circuit architectures involved are becoming more and more complex. Most of the transceivers involve multiple frequency ranges, starting at large bands (a few GHz) at baseband. In the RF section, high frequency local oscillators are also required, on the order of a few tens of GHz and the RF signal over the air can be as high as a few hundreds of GHz. The high RF signal frequencies constrain to tightly integrate the electronic transceivers with the antennas, involving in general many identical ICs mounted on top of antenna arrays in complex planar structures implementing phased arrays. In the context of these complex assemblies, it is not enough to address the single die testing but the overall array should be tested, considering potential assembly defaults in some of the IC units or antenna elements. This brings the

design of the testing and calibration strategy to an unprecedented degree of complexity.

Several techniques can be used on-chip to alleviate the testing and calibration complexity. Loop-back test can be implemented either intentionally with couplers between the Tx output and the Rx input, or using the non-zero isolation of TRX switches. Our experience is that these types of loop-back provide qualitative observability but it is very difficult to know the exact Tx output power level in all process corners so that quantitative characterization of the Rx is usually not possible with this approach. Other techniques such as power sensors and DC bias probes are routinely included, complemented with extensive on-chip bias generation and monitoring with a single analog bus connected to a circuit output (see Figure 3), that can used in a similar way as the digital section scan path test bus.

Finally, some RF features can be observed at lower frequency using some signal-processing tricks. For example, sub-sampling can be used to integrate the spectra around the expected oscillator frequency. The resulting low frequency signal can be used as a signature of phase noise or locking state for testing and/or calibration purposes. Temperature sensors can be used as homodyne or heterodyne down-converters to obtained low-frequency signatures of RF operation. These techniques can be used to indirectly measure the bandwidth and center frequency of high-frequency blocks without having an electrical contact to the sensitive nodes. They have also been demonstrated for the determination of the efficiency and loading state of power amplifiers, which would allow detecting connection issues to the antennas in the context of complex assemblies.

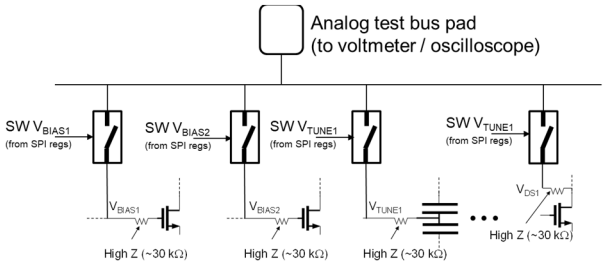


Figure 3. Illustration of an on-chip analog test bus used in RF ICs for observability of DC bias and other internal low frequency signals.

Feature selection techniques for indirect test and statistical calibration of mm-wave integrated circuits

Manuel J. Barragan, Gildas Leger, Florent Cilici, Estelle Lauga-Larroze, Salvador Mir, Sylvain Bourdel

I. Introduction

Nowadays, the constant evolution of CMOS technologies towards smaller design nodes and higher transitions frequencies, together with the development of optimized back-end-of-line (BEOL) options, make possible the co-integration of complex RF and mm-wave circuits in a single silicon substrate. However, these advanced integration nodes are prone to large process variations and manufacturing defects that may result in a significant –sometimes catastrophic– performance degradation and low fabrication yield. Extensive production test and calibration procedures are required to guarantee the performance of integrated RF and mm-wave circuitry, which, due to the complex nature of at-speed functional test, results in expensive and long test and calibration cycles that may stall the production line.

Leveraging the power of machine learning techniques has been proposed as a promising solution to alleviate these issues. These techniques are aimed at replacing the direct measurement of complex functional specifications by simpler observables, usually called signatures, that are strongly correlated to the target specifications. Machine learning regression algorithms are then employed to map the signatures to the target specifications. Since signatures are designed to be simpler and cheaper to extract –in many cases even using some sort of simple on-chip test instruments– the overall test complexity and cost are greatly reduced. This is the basis of the so-called alternate test [1]-[2] , where supervised machine learning models are used to replace the classical functional test. Supervised machine learning models are applied in two phases: a training phase, where the model is inferred from a set of training data containing both the input signatures and the target specifications; and a testing phase, where only the signatures are measured and the target performance is predicted using the previously inferred machine learning regressor.

Indirect test based on machine learning regression is an elegant solution to simplify the complexity of analog functional testing while still addressing the issue of characterizing the circuit performance and comparing it against classical performance acceptance windows. Moreover, this technique can be easily extended to performance calibration applications. Indeed, provided that the circuit has some tuning knobs, the machine learning regressor can be trained to predict the optimum positions of the tuning knob, rather than the nominal performance [3]-[5].

However, machine learning-based test and calibration are not free of shortcomings and potential pitfalls that should be addressed for a successful implementation. In this special session we will focus on one of the main issues for the adoption of these techniques: the choice of a meaningful set of input signatures. It is clear that finding appropriate signatures that are strongly correlated to the target performances is a key point of this test strategy. Actually, early works on this topic explored an automated signature generation technique based on optimizing a piecewise-linear test stimulus to recover meaningful output signatures [6]. While this is a sound strategy, the nature of the test stimulus is fixed which may limit the information that can be recovered from the output signatures. In this special session we will explore a more general solution to the definition of appropriate signature sets based on advanced feature selection algorithms. First, we will introduce the concept of feature selection, describing the potential advantages and disadvantages of different techniques. Then, we will present some case studies to illustrate the application of feature selection techniques to different scenarios in the context of mm-wave ICs.

II. Feature Selection Techniques

Given a set of input features and a set of target specifications, the goal of a feature selection algorithm is to find the minimum subset of input features that can be used to regress the target specifications within a predefined prediction error. In practice, signature sets are either proposed *ad hoc* based on expert design knowledge or generated by following an *ad hoc* procedure such as [6]. As a result, the initial signature set is usually suboptimal: it may contain redundant information, noise, or even information that is uncorrelated to the target specifications. A variety of feature selection techniques have been proposed in the literature for cleaning up the input signature space in indirect test applications [7]-[14]. Generally speaking, we can classify these proposals in three main feature selection families: a) Wrappers, b) Filters, and c) Hybrid feature selection.

A. Feature selection using wrappers

The wrapper approach to feature selection considers the selection as an optimization problem. Wrapper feature selection algorithms employ the machine learning regressor as a black box within an optimization loop. An optimizer is used to explore the input feature space and find the optimum set that minimizes the prediction error. The main advantage of the wrapper approach is the direct estimation of the prediction error, while the main disadvantage is the computational cost, as training and evaluation have to be repeated in each step of the optimization loop. For large data sets, a full search in the input feature space becomes impossible, and smart search strategies must be used [7].

B. Feature selection using filters

Filters are aimed at selecting or removing signatures from the initial feature set based on a statistical observation, without the need of training a machine learning model. In general, we can distinguish two families of filters: unsupervised and supervised filters.

Supervised filters rank the candidate features in the input feature space according to their correlation to the target performance. Complex multidimensional and/or nonlinear correlation metrics that go beyond Pearson's classic

correlation have been explored in recent literature, including Kendall's tau [11], Brownian distance correlation [10], minimal-redundancy-maximal-relevance criterion [8], etc. Unsupervised filters, on the other hand, do not consider the information in the target space. Instead, they analyze the information structure in the feature space. The most common example of unsupervised filter is the Principal Component Analysis (PCA), that tries to identify the directions in the feature space that best explain the variation observed in the data, supposing that the underlying structure in the data is linear [12]. The main advantage of filtering techniques is the low computational cost. However, they do not offer any estimations of the prediction error that can be expected in the regression.

C. Hybrid feature selection techniques

Hybrid techniques were proposed in [8] as a way of combining the advantages of wrappers and filters. The main idea is to use a correlation metric, such as the Brownian distance correlation, to guide the selection of new features in a classical wrapper loop. In this scheme, a feature is selected if it can explain the prediction error in the previous iteration of the wrapper loop. This way, only one training stage is required per iteration and the selection is naturally biased to add features that are meaningful for improving the predictions.

III. Case Studies

A. Nonintrusive indirect test of mm-wave circuits [15]

Our first case study is aimed at the systematic design of an indirect test program for a mm-wave DUT based on nonintrusive process monitors. Nonintrusive process monitors are stand-alone circuits that are integrated in the close proximity of the DUT, but that are not electrically connected to it. These monitors provide a low-frequency or DC signature that is strongly correlated to the variation of a given process parameter. It should be clear that by carefully choosing relevant process monitors, we could be able to train a machine learning regressor that would be able to predict the performance of the DUT by measuring only the signatures provided by the process monitors. Early works on nonintrusive test proposed process monitor circuits that mimic DUT circuit structures [16]-[18], however this may result in subobtimum performance prediction as only first-order performance degradation mechanisms may be covered based just on a visual inspection of the design architecture [18].

Feature selection techniques can be used to systematize the design of process monitors, as demonstrated in [7], [15]. In this regard, we can use a feature selection algorithm to explore, in a simulation environment, the space of process parameters defined in the Monte Carlo and corner models in the PDK of the technology, in order to find the parameters that are actually relevant for the DUT performance. Once identified, we can target the design of process monitors that provide signatures of these parameters. The interested reader is referred to [15] for a detailed description of the proposed feature search technique.

The proposed technique has been successfully applied to a 65 GHz PA case study fabricated in STMicroelectronics 55nm CMOS technology. A feature selection algorithm based on a hybrid selection technique was employed to explore the space of process parameters of the technology, containing more that 500 independent parameters. Hybrid selection allowed the identification of only 11 relevant parameters, which guided the design of appropriate process monitors. The feasibility of the resulting indirect test was validated in a set of 21 fabricated samples. Table I shows the relative RMS prediction error obtained in the prediction of the main PA specifications from the nonintrusive signatures. As it can be seen, a significant precision is achieved for all the considered specifications.

TABLE I. Relative RMS Prediction Error

Specification	Relative RMS prediction error (%)
S_{21}@65GHz	1.4
S_{11}@65GHz	1.6
S_{22}@65GHz	2.0
P_{sat}	0.7
CP_{1dB}	1.3
PAE	2.0
I_{DC}	0.65

B. One-shot statistical calibration of mm-wave circuits using nonintrusive performance monitoring [19]

Our second case study is aimed at designing a one-shot calibration strategy for yield enhancement of a mm-wave DUT, based again on nonintrusive process monitors. Since process monitors track process variations, assuming that appropriate tuning knobs are included in the DUT, it would be possible to correlate the output of the monitors to the optimum calibration code, i.e., the positions of the tuning knobs that minimizes performance degradation due to process variation. This strategy has the advantage of avoiding costly and lengthy test-and-tune calibration loops.

Again, feature selection algorithms are a key element for defining this calibration strategy. Feature selection can be used to explore the multidimensional space of process parameters in search of the relevant process parameters for predicting the calibration code, while at the same time can guide the design of appropriate tuning knobs by unveiling the main root causes of performance variation in the DUT. The interested reader is referred to [19] for a detailed description.

The proposed technique has been applied to a 69 GHz PA case study fabricated in STMicroelectronics 55nm CMOS technology. The feasibility and performance of the proposed calibration is demonstrated on a set of 39 fabricated samples. Table II shows the yield before and after calibration for each of the considered PA specifications. It is clear to see a dramatic yield improvement due to the proposed one-shot calibration solution.

TABLE II. Yield Enhancement

Specification	Yield before calibration (%)	Yield after calibration (%)
S_{21}@69GHz	51	100
S_{11}@69GHz	90	100
S_{12}@69GHz	100	100
P_{sat}	74	95
CP_{1dB}	77	100
PAE	31	100
IDC	72	97
Overall yield	5	92

References

[1] P. N. Variyam and A. Chatterjee, "Enhancing test effectiveness for analog circuits using synthesized measurements," in *VLSI Test Symposium*, 1998, pp. 132–137.

[2] G. Leger and M. J. Barragan, "Mixed-signal test automation: Are we there yet?," 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 2018, pp. 1-5.

[3] N. Kupp, H. Huang, Y. Makris, and P. Drineas, "Improving Analog and RF Device Yield through Performance Calibration," *IEEE Design & Test of Computers*, vol. 28, no. 3, pp. 64–75, May 2011.

[4] M. Andraud, H. Stratigopoulos, and E. Simeu, "One-Shot Non-Intrusive Calibration Against Process Variations for Analog/RF Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 2022–2035, Nov 2016.

[5] A. Zjajo, M. J. Barragan, and J. P. d. Gyvez, "Low-Power Die-Level Process Variation and Temperature Monitors for Yield Analysis and Optimization in Deep-Submicron CMOS," *IEEE Trans. on Inst. and Meas.*, vol. 61, no. 8, pp. 2212–2221, Aug. 2012.

[6] P.N.Variyametal.,"Prediction of analog performance parameters using fast transient testing," Trans. on Computer-Aided Design of Int. Circ. and Syst., vol. 21, no. 3, pp. 349-361, 2002.

[7] M. Barragan and G. Leger, "A Procedure for Alternate Test Feature Design and Selection," *IEEE Design & Test*, vol. 32, no. 1, pp. 18–25, Feb. 2015.

[8] G. Leger and M. J. Barragan, "Brownian distance correlation-directed search: A fast feature selection technique for alternate test," *Integration, the VLSI Journal*, vol. 55, pp. 401–414, Sep. 2016.

[9] H.-G. Stratigopoulos *et al.*, "RF Specification Test Compaction Using Learning Machines," *Trans. on VLSI Systems*, 2009.

[10] M. J. Barragan and G. Leger, "Efficient selection of signatures for analog/RF alternate test," in *European Test Symposium*, 2013.

[11] A. Gomez-Pau, L. Balado, and J. Figueras, "Efficient Production Binning Using Octree Tessellation in the Alternate Measurements Space," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 35, no. 8, pp. 1386–1395, 2016.

[12] H. Ayari *et al.*, "Smart selection of indirect parameters for DC-based alternate RF IC testing," in *VLSI Test Symposium*, 2012, pp. 19–24.

[13] S. Larguech *et al.*, "Efficiency evaluation of analog/RF alternate test: Comparative study of indirect measurement selection strategies," *Microelectronics Journal*, vol. 46, no. 11, pp. 1091–1102, Nov. 2015.

[14] M. J. Barragan, G. Leger, F. Cilici, E. Lauga-Larroze, S. Bourdel and S. Mir, "On the use of causal feature selection in the context of machine-learning indirect test," 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, 2019, pp. 276-279.

[15] F. Cilici et al., "A Nonintrusive Machine Learning-Based Test Methodology for Millimeter-Wave Integrated Circuits," in IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 8, pp. 3565-3579, Aug. 2020.

[16] A. Zjajo, M. J. Barragan and J. P. de Gyvez, "BIST Method for Die-Level Process Parameter Variation Monitoring in Analog/Mixed-Signal Integrated Circuits," 2007 Design, Automation & Test in Europe Conference & Exhibition, Nice, France, 2007, pp. 1-6.

[17] L. Abdallah, H. Stratigopoulos and S. Mir, "True non-intrusive sensors for RF built-in test," 2013 IEEE International Test Conference (ITC), Anaheim, CA, USA, 2013, pp. 1-10.

[18] A. Dimakos, H. -G. Stratigopoulos, A. Siligaris, S. Mir and E. De Foucauld, "Built-in test of millimeter-Wave circuits based on non-intrusive sensors," 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, Germany, 2016, pp. 505-510.

[19] F. Cilici, M. J. Barragan, S. Mir, E. Lauga-Larroze, S. Bourdel and G. Leger, "Yield Recovery of mm-Wave Power Amplifiers using Variable Decoupling Cells and One-Shot Statistical Calibration," 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 2019, pp. 1-5.

Integrated Characterization Solutions for ICs and Devices Beyond 100 GHz

M. Margalef-Rovira, I. Alaji, H. Ghanem, G. Ducournau, and C. Gaquiere

***Abstract*—This paper presents an innovative integrated load-pull bench at 160 GHz. The proposed system, which is designed in a 55-nm BiCMOS technology, is tailored to deal with all of the measurement functions including signal generation, shaping, and magnitude and phase measurement. This system will allow precise characterization of Devices-Under-Test (DUTs) (i.e., circuits and/or devices) when integrated together with the DUT. In addition, the proposed system could also be envisioned as a System-on-Chip (SoC) that, when reported into an RF probe, could serve as a test bench for any integrated circuit.**

***Keywords*—mm-Wave, BiCMOS, active load-pull, impedance tuner, power meter.**

I. Introduction

The current evolution of CMOS-based technological nodes has allowed to tackle frequencies in the millimeter- and submillimeter-wave range (i.e., from 30 GHz to beyond 300 GHz) [1]. However, building resilient models and precise characterization of devices and circuits integrated in these technologies remains an issue. There are many reasons that give raise to these issues. However, some of the most obvious are: (i) the increase of losses in the characterization setup [2] and, (ii) the undesired coupling of the measurement instruments with the Device-Under-Test (DUT) [3].

Hence, in order to avoid those issues, a new approach has to be taken. The most straightforward approach is to design the test bench in the same die where the DUT is located (e.g., [2]). In this approach – and to avoid any interference with the DUT – the test bench is directly connected to the DUT. Hence, dramatically limiting the reusability of the test bench for different DUTs. However, the design of a generic test bench which could later be integrated in an RF probe as a System-on-Chip (SoC) opens the door to precise and low-cost measurement equipment.

One of the test benches that is rapidly limited in performance as frequencies increase is the load-pull. Indeed, the losses in the RF probes and associated waveguide-based transitions, for frequencies beyond 110 GHz, greatly decreases the amount of available power at the input/output of the DUT. In this work, we have designed an active load-pull test bench in a 55-nm BiCMOS technology aiming at the characterization of devices at 160 GHz.

This paper is organized as follows: section II presents the designed architecture and all of its building blocks. Finally, in section III, the main conclusions of this work are given.

II. Proposed System

Fig. 1 presents the proposed topology. The system is constituted by an 80-GHz differential amplifier, a differential frequency doubler, two continuous-tuning attenuators, a phase shifter, a 2-stage power amplifier, a 3-stage power amplifier and two phase and magnitude detection units. The system is divided into two branches. As depicted in

Fig. 1, the left branch of the test bench is used to inject a RF signal to the input of the DUT, whose amplitude can be modulated, while the right branch is used to modulate the amplitude and phase, effectively synthesizing a phase- and magnitude-tunable reflection coefficient.

A. Signal generation unit

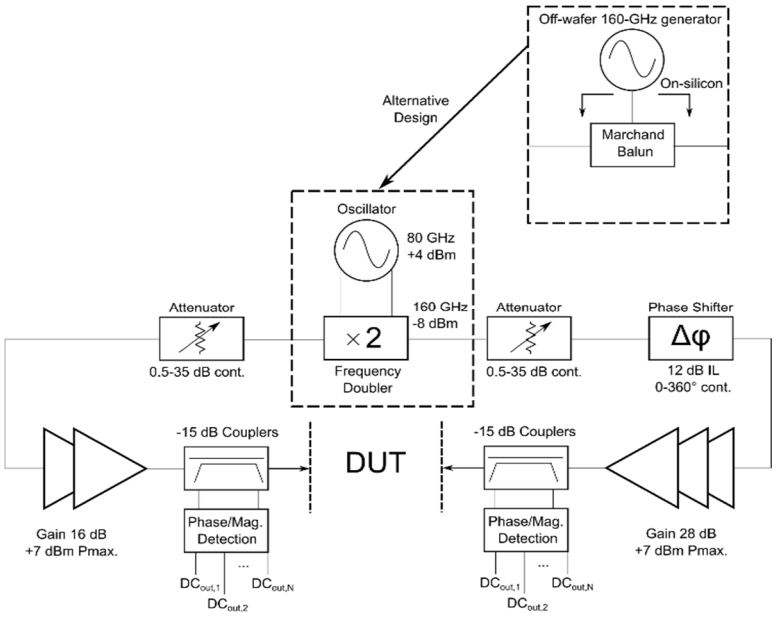


Fig. 1. Proposed integrated load-pull system.

The signal generation unit consists in a 80-GHz oscillator and a frequency doubler. Even though active load-pull is theoretically possible using two different RF sources, the use of a single RF source eliminates the risk of non-coherence between both RF signals. Hence, a single 80-GHz oscillator was used. The designed oscillator uses a topology similar to the Voltage-Controlled Oscillator (VCO) in [4]. Some modifications in the slow-wave transmission line resonating tank and the elimination of the varactors allow a high-power output of around +4 dBm. To ensure a high-power output and reduced impact of the parasitic capacitances of the transistors in the cross-coupled pair, the oscillator was designed at 80 GHz and subsequently fed into a frequency doubler.

This frequency doubler, that presents a 12-dB conversion loss is based on a passive differential mixer (e.g., [5]) using PMOS and NMOS transistors. At the output of this unit, a signal with a power of -8 dBm at 160 GHz is found.

In addition to this design, a stand-alone Marchand balun based on the couplers presented in [6] was designed. This balun could effectively substitute the need of the VCO and the frequency doubler if an external RF source was used.

B. Signal-shaping unit

The signal-shaping unit is constituted by the attenuator and the phase shifter. The left branch of the circuit presented in

Fig. 1, only contains the attenuator that allows tuning the amplitude of the injected signal. On the other hand, the right branch also includes a continuous-tuning 0-360° phase shifter to allow control on the relative phase between the signals injected in the input and output of the DUT.

Both attenuators are based on the *through-load* architecture presented in [7] and can achieve a continuously-tunable attenuation in the 0.5-35 dB range with a single control voltage. On the other hand, the phase shifter is constituted of two architectures: (i) a two-bit switched-line phase shifter (e.g., [8]), which allows achieving a resolution of 90°, and (ii) a Reflection-Type Phase Shifter (RTPS) that can cover the 0-90° in a continuous manner. The reflective load used for this RTPS is based on the Inversion-MOS varactor presented in [9]. The three stages of the phase shifter lead to a total insertion loss of 12 dB (i.e., a FoM of 30 dB/°).

In addition, the linearity of the structure was also studied, revealing that the proposed phase shifter is resilient against undesired non-linearities.

C. Power Amplification

The system is composed of a 2-stage power amplifier on the left branch and a 3-stage power amplifier located in the right branch. These power amplifiers present a small-signal gain of 16 and 28 dB, respectively. Their power gain and saturation input power have been carefully designed so that when the attenuation level of the attenuators is at the minimum, those stages are driven into saturation, yielding a total output power of +7 dBm at 160 GHz.

D. Phase and magnitude detection unit

In order to obtain a signal output that can be easily read by the external user, zero-bias power detectors, similar to the ones used in [10], were integrated in each branch together with a microstrip-based coupled-line coupler. Those integrated power detectors yield a DC voltage, which is a function of the input power.

This approach avoids the integration of mixers that would dramatically increase the complexity of the design and its sources of measurement uncertainties. In addition, adding mixers would also require additional RF signal generation and/or splitting.

Thanks to a clever placing of the power detectors along the 15-dB coupler, it can be demonstrated that the magnitude and phase of the injected/reflected RF signals can be retrieved solely from the measurement of the DC voltages generated in the power detectors.

III. Conclusion

This paper has presented an integrated architecture of active load-pull test bench at 160 GHz. The proposed tuner includes all the functions of a single-tone active load-pull test bench. The presented bench could be integrated together with a DUT to perform on-wafer characterization. In addition, the proposed test bench could be massively produced at a relative low cost and included into RF probes, greatly reducing the cost of a similar off-wafer bench and also allowing to increase the precision of current load-pull benches at 160 GHz.

Acknowledgement

This work has been partially funded by the NANO2022 project.

References

[1] T. Zimmer *et al.*, "SiGe HBTs and BiCMOS Technology for Present and Future Millimeter-Wave Systems," *IEEE J. Microwaves*, vol. 1, no. 1, pp. 288–298, 2021, doi: 10.1109/jmw.2020.3031831.

[2] C. Maye *et al.*, "Load-Pull Setup Development at 185 GHz for On-Wafer Characterization of SiGe HBT in BiCMOS 55 nm Technology," *IEEE Trans. Microw. Theory Tech.*, vol. 70, no. 1, pp. 444–452, 2022, doi: 10.1109/TMTT.2021.3111170.

[3] S. Fregonese *et al.*, "On-Wafer Characterization of Silicon Transistors Up To 500 GHz and Analysis of Measurement Discontinuities Between the Frequency Bands," *IEEE Trans. Microw. Theory Tech.*, vol. 66, no. 7, pp. 3332–3341, 2018, doi: 10.1109/TMTT.2018.2832067.

[4] E. Sharma *et al.*, "Design of a 77-GHz LC-VCO with a slow-wave coplanar stripline-based inductor," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 67, no. 2, pp. 378–388, 2020, doi: 10.1109/TCSI.2019.2926415.

[5] D. Ozis, N. M. Neihart, and D. J. Allstot, "Differential VCO and passive frequency doubler in 0.18 /spl mu/m CMOS for 24 GHz applications," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2006*, 2006, pp. 4 pp.-, doi: 10.1109/RFIC.2006.1651084.

[6] M. Margalef-Rovira *et al.*, "Design of mm-Wave Slow-Wave-Coupled Coplanar Waveguides," *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 12, pp. 5014–5028, 2020, doi: 10.1109/TMTT.2020.3015974.

[7] M. Margalef-Rovira *et al.*, "Mm-Wave Through-Load Element for On-Wafer Measurement Applications," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 68, no. 8, pp. 3170–3183, 2021, doi: 10.1109/TCSI.2021.3072097.

[8] J. C. S. Chieh, J. Rowland, and S. Sharma, "Four-bit W-band switched line phase shifter in 90 nm SiGe," *Electron. Lett.*, vol. 54, no. 17, pp. 1040–1041, 2018, doi: 10.1049/el.2018.5380.

[9] M. Margalef-Rovira *et al.*, "Highly Tunable High-Q Inversion-Mode MOS Varactor in the 1-325-GHz Band," *IEEE Trans. Electron Devices*, vol. 67, no. 6, pp. 2263–2269, 2020, doi: 10.1109/TED.2020.2989726.

[10] I. Alaji, S. Lépilliet, D. Gloria, G. Ducournau, and C. Gaquière, "Design and Characterization of (140–220) GHz Frequency Compensated Power Detector," *IEEE Trans. Microw. Theory Tech.*, vol. 69, no. 4, pp. 2352–2356, 2021, doi:

10.1109/TMTT.2021.3062054.