Highly robust and reliable power amplifiers in 22FDX and 45RFSOI technologies

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***Abstract*—This paper reports the VSWR (Voltage Standing Wave Ratio) ruggedness and aging measurements of two power amplifiers designed in 22FDX and 45RFSOI technologies. The PA is one of the most critical function in a front-end module as it is operating at high power and directly impacted by mismatch load. De-rating of 20% is applied on the supply voltage to ensure the operation and durability of the power amplifiers for a 10 years lifetime. The measured and modelled degradation versus time are presented and show excellent results on both technologies.**

Keywords—Reliability, Aging, power amplifier, 5G, 22FDX, 45RFSOI

I. Introduction

Reliability and aging are a main concern for power amplifiers, which is the module in the RF transceiver that delivers the highest output power. This implies voltages across transistors that could be more than two-times higher than the recommended foundry Vdd_{max} when used at maximum power operation. Important design margins must be considered to keep the transistor in a safe area to prevent breakdown and quick degradation over time. In beamforming 5G transceiver, the required output power per transceiver depends on the number of elements for a given EIRP (Effective Isotropic Radiated Power) [1]. For large antenna array, a III-V front end module is not required, but advanced silicon technologies are preferred for PAs (40nm node or below) in order to be integrated into the RF transceiver (SoC) and to provide enough gain and PAE at mmW frequencies. The SOI (Silicon On Insulator) technologies are good candidates to answer these needs for low cost, good gain (f_{MAX}) and power handling capabilities. In that context, this work proposes to evaluate the ruggedness and aging of the 45RFSOI and the 22FDX technologies from GlobalFoundries.

II. Power Amplifiers in 22FDX and 45RFSOI

Implementing >200 mW power PA in sub-micron CMOS technology at 40 GHz is a challenging task due to the low transistor breakdown voltage as well as losses of passive silicon components. There are currently several topologies proposed by the designer community to generate high output power. In typical beamforming applications, the output power levels of multiple low to medium power PAs are combined to generate a total high output power at a low supply voltage. However, the effectiveness of power combining techniques is limited due to the losses linked to the substrate and the low thickness of the metals of CMOS technology inducing high series resistances. A combination of 4 to 8 outputs is a maximum. One of the most efficient topology is the transformer-based combiner due to its small size and its ability to perform the function of combiner and impedance transformer simultaneously, reducing the additional losses generated by a matching network (Fig. 1.a). Another possibility is to stack transistors in a cascode configuration, with 2 or more transistors, to use a larger supply voltage and reduce the risks of breakdown (BD) at high mismatches. Therefore, a voltage combination is performed instead of a power/current combination. The use of thick oxide transistor is a good way to increase the BV but should be limited to the stacked transistor due to its limited performance in mmW. On the other hand, increasing the number of stacks decreases the overall efficiency showing a structural limit to the use of thin oxide transistors in a stack greater than 3 as designed Fig. 1.b [2]. In this paper, two architectures are evaluated, using the voltage combination in 22FDX and the stacking technique in 45RFSOI and presented Fig. 1.

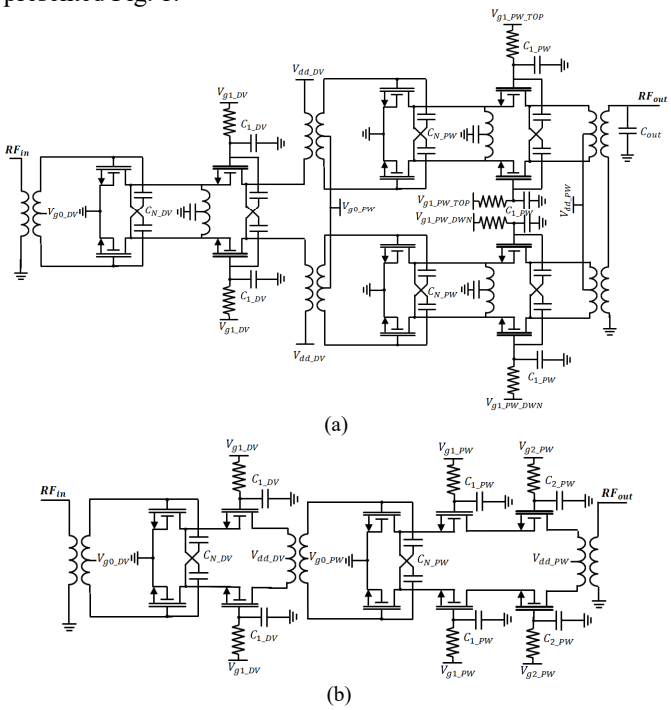


Fig. 1 : Power amplifiers schematics in 22FDX (a) and in 45RFSOI (b)

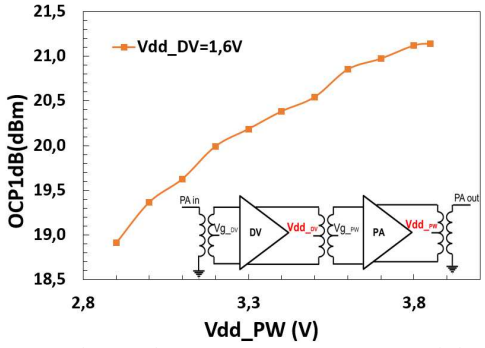


Fig. 2 : Measured OCP1dB versus V_{DD_PW} at 39 GHz of the 45RFSOI power amplifier for different V_{DD_DV}

Any devices biased at nominal technology voltage is exposed to reliability issues in large signal operation, making them sensitive to Hot Carrier Injection (HCI) and Time Dependent Dielectric Breakdown (TDDB). It appears that

most designs are biased at the upper limit to reach higher output power as show Fig. 2. In our case, increasing V_{dd_PW} by 1V (2nd stage PA45RFSOI Fig. 1.a) improves the measured OCP1dB by 3dBm, but the supply voltage is not compliant in the context of industrial use.

In these designs, a de-rating of 20% is applied on the supply voltage to ensure the operation and durability of the power amplifiers for a 10 years lifetime as described TABLE 1.

TABLE 1 : MAXIMUM Vdd VOLTAGE FOR 22FDX AND 45RFSOI TECHNOLOGY AT 125°C

FET	L (nm)	Vdd (V) Max @125 °C	Vdd (V) with a de-rating of 20%
SLVT 22FDX	20	0,8	**0,64**
EGSLVT 22FDX	150	1,8	**1,44**
FB Regular Vt nfet, pfet 45RFSOI	40	1,1	**0,88**
FB 1.5V FETs tonfet, topfet 45RFSOI	112	1,65	**1,32**

III. AGING AND VSWR RUGGEDNESS METHODOLOGY

A. *Ageing methodology*

The ageing deals with the degradation of a device that occurs because of exposure to high voltages over time. This degradation is induced by two physical mechanisms: TDDB and HCI. A drain current drop I_{dsat} of more than 10% (~0,5dBm RF output drop) is chosen as a critical degradation since the current trend line is exponential after reaching this point. The RF stress sequence is summarized on Fig. 3. An initial power sweep is performed at t_0 and the source power is searched in order to get the appropriate P_{out_stress} and P_{out_BO}. The power is then set to the stress level desired and left as is, while the power levels, currents and voltages are monitored periodically. At specific moments following a logarithmic sampling, the input power is lowered to monitor the back-off performance before returning to stress level. At the end of the RF stress, another power sweep is performed. The RF and DC feed are cut off, a new probe contact and another power sweep are performed in order to verify potential probe contact issues during the stress, due to pad oxidation. The total stress time is limited to 9h, which corresponds to a compromise between total stress time and potential contact issues.

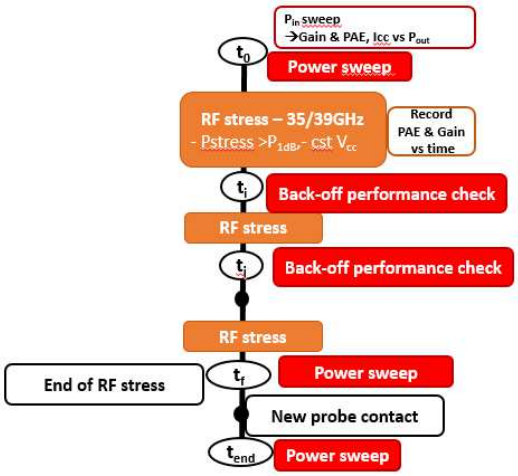
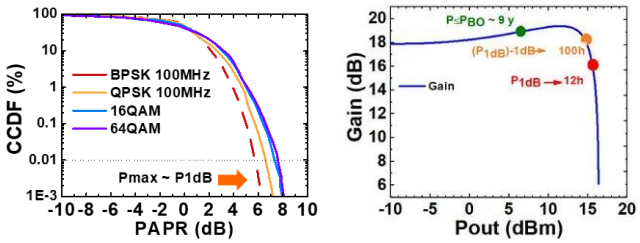


Fig. 3 : RF Stress algorithm

In order to evaluate the power amplifier ageing through a modulated mission profile, an output power-based acceleration model is used. The power dynamic under modulation is presented on Fig. 4. Most of the PA operating time is spent at ~8-9dB back-off or even less while power peaks up to P1dB represent only a very short cumulated time. Considering a 10 years lifetime, always ON for simplicity purposes, the amplifier will spend approximately 9 years at back-off (Peak to Average power ratio or PAPR = 0dB), 100 hours at P1dB-3dB and 13 hours at P1dB.



(a) (b)

Fig. 4 : CCDF of a power amplifier for various modulation profiles (a) Gain, PAE vs Pout of the 45RFSOI power amplifier, with time passed @PBO, P1dB -3dB & P1dB for a 10 years 100% ON mission profile under OFDM modulation (b)

The large signal performance drift is measured for continuous wave (CW) stresses at different output power, chosen above P1dB for acceleration purposes. The parameter drift ($Gain_{BO}$ and/or P_{stress}) versus time is then modelled using a saturated power law (eq.1), which is a common model used in reliability [3]. This model depends on a saturation parameter *sat*, a scaling factor *A*, an output power acceleration factor γ and the time to the power *n*. Three different stress for each PA is a minimum requirement in order to model accurately the output power acceleration and is described next part. Eq.1 represent the degradation of a parameter under RF stress, following a saturated power law.

$$\Delta Parameter(dB\ or\%) = \frac{1}{\frac{1}{sat} + \frac{1}{10^{A}.P_{out}{}^{\gamma}.t^{n}}} \quad (1)$$

B. *VSWR ruggedness methodology*

In the product lifetime in 5G telecommunication, antenna impedance mismatches may occur, inducing high VSWR on the PA. The transistors will function at higher Vd & Id compared to the matched condition, running the risk of inducing higher HCI degradation or even TDDB. The measurement verification for the breakdown voltage (BVDS) and the circuit ruggedness to VSWR are then essential. In FDSOI the FETs are not sensitive to parasitic bipolar activation as the channel is fully depleted, compare to the PDSOI technology. The Vds limit is defined for $V_{G=0V}$ and V_{dgmax}. Based on gate length and a temperature of 25°C, Vds limit in 22FDX is 3,25V for slvt FET and 4,6V for the egslvt FET. In 45RFSOI the Vds limit is 1,8V for the adnfet and 2,35V for the tonFET. Simulation are performed on the PA in 45RFSOI for a VSWR of 4:1, the worst-case voltage across transistors are on the 2nd stage Fig. 1.a, with V_{ds3max}=3.5V for the upper thick oxide transistor, and V_{ds2max}=2V / V_{ds1max}=1.6 V for the two adnfet thin oxide common base and common source transistor respectively. Compare to the V_{dsmax} of thick and thin oxide transistors of 2.35 V and 1.8 V, the voltages seen by the transistors are

49% and 11% higher than the recommended voltage for the tonFET and adnFET respectively.

Two reliability measurements are performed on the power amplifiers based on [4] to see if any break down occurs: a soft stress test corresponding to a short 27 min of stress loading VSWR 4:1 and a hard test corresponding to 15 hours of stress, same load.

IV. MEASUREMENTS RESULTS

A. *Measurements Ageing CW results*

The two different PA architectures (22FDX PA and 45RFSOI PA) were stressed at three different power levels and on a fresh die each time.

- Pout=P1dB at 25°C for 9h, Vdd nominal
- Pout=P1dB+**1dB** at 25°C for 9h, Vdd nominal
- Pout=P1dB+**2dB** at 25°C for 9h, Vdd nominal

From these measurements the gain at back-off, the P_{stress}, the currents I_{DV}, I_{PW} and I_{gates} vs time are extracted. Fig. 5 describes a power sweep before/after stress and with a new contact afterwards. The new contact is used in order to de-correlate a potential contact issue on the RF probes and may retrieve some performances. If a large drift is initially observed and is then recovered with a new probe contact, the data are not considered and another die is stressed for the same condition, or with a lower stress power.

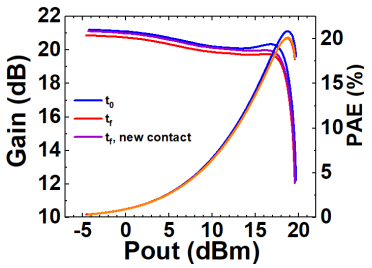
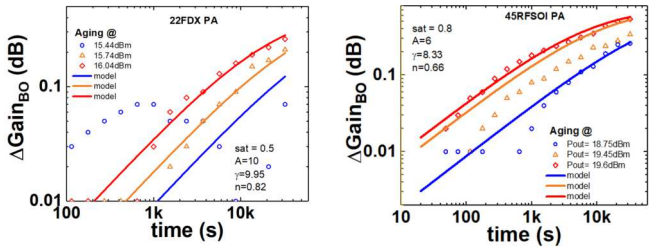


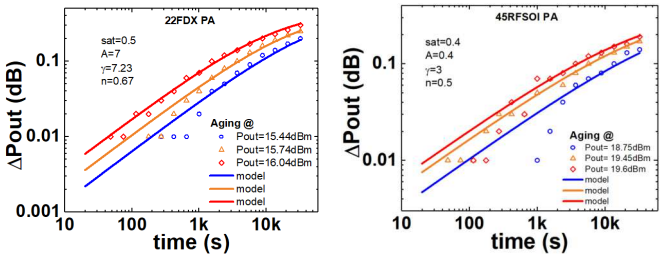
Fig. 5 : Gain, PAE vs Pout before, after stress, and with a new contact (45RFSOI PA)

The measured and modelled degradation versus time are presented on Fig. 6 and Fig. 7 for back-off Gain and Pout. The G_{BO} drift is relatively difficult to model because the drift window is very small and some of the measurements that are not consistent with the others (lower power level on Fig. 6.a or middle level on Fig. 6.b). The limitation in test time and dies to stress is not allowing many different conditions and dies for statistics. However, the modeling is successful on the P_{out} vs time degradation (output power at P_{stress}, in compression). A general P_{out} drift model is extracted, with a saturation value close to 0.5 dB for both power amplifiers.



(a) (b)

Fig. 6 : Back-off gain versus time degradation and modeling for both PAs



(a) (b)

Fig. 7 : Pout (in saturation) versus time degradation and modeling for both PAs

It is then possible to estimate the Pout degradation for 9 years at back-off, 100 hours at P1dB-3dB and 13h at P1dB separately. These estimations are presented in TABLE 2.

TABLE 2 : POUT DEGRADATION ESTIMATED FOR DIFFERENT OUTPUT POWER LEVELS FOR THE TWO POWER AMPLIFIERS

	22FDX PA P_{out} drift	45RFSOI PA P_{out} drift
9 years @ 9dB BO	0	0.02dB
100h @ P_{1dB}-3dB	-0.17dB	-0.16dB
13h @ P_{1dB}	-0.2dB	-0.13dB

A graphical representation of these CW-like RF stress modeling is presented on Fig. 8. For the 45RFSOI power amplifier, the output power acceleration factor is relatively low (γ=3), which explains why the degradation simulated for 13h @P1dB is comparable compared to 100h with 3dB less output power. The 22FDX PA seems to be more accelerated with power compared to the 45RFSOI PA. This may be explained by the technology node (22nm vs 45nm) which implies more HCI acceleration with equivalent voltage but is also very design dependent.

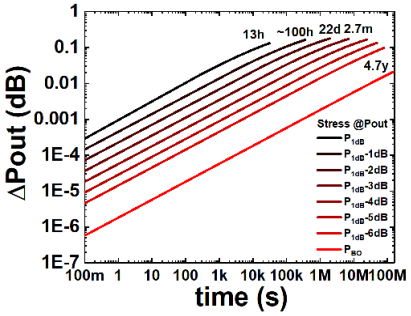


Fig. 8 : Estimated Pout degradation for PA 45RFSOI, with different power levels and for time interval corresponding to CCDF under 64QAM mission profile.

In order to obtain the real estimated degradation under modulation, a proper sum of the degradation along a typical 5G modulation profile must be conducted.

B. *Ageing simulation on modulated data*

The non-linear characteristics of both 22FDX and 45RFSOI PAs are measured on wafer using Vector Network Analyzer. From these data, AM/AM and AM/PM polynomial model are extracted by curve fitting. A 6th order model is enough to fit the characteristics with low discrepancies. Then a 5GNR-FR2 waveform feeds those PA nonlinear models to get the signal distribution by simulation. The waveform corresponds to a 1ms frame with numerology 2, modulated with OFDM 64QAM and sampled at 245.76MHz. Then the waveform is up-converted to 39.32GHz (Fs/4) in the FR2 band. The mmW signal is adjusted in amplitude to be set to 9dB input power back off

from P1dB. Due to PA compression, the signal spectrum exhibits regrowth, and the power distribution is truncated close to the saturation. The modulated signal power at PA output (Pout) is recorded and feeds the ageing model.

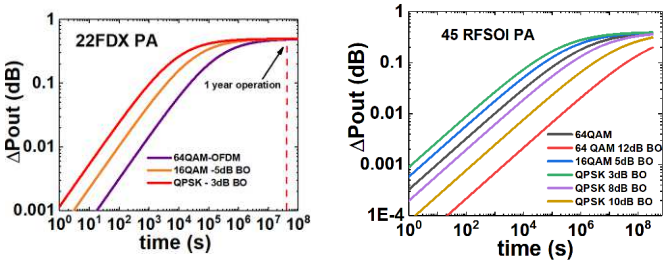
Using the extracted Pout vs time samples and the quasi-static approximation, it is then possible to estimate the degradation for each PA under the 5G modulation profile. First, the degradation rate is calculated for each power in the sample eq. (2), using the CW aging model generated previously (parameters A, γ and n).

$$Degradation\ rate(t) = (10^{A}.P_{out}(t)^{\gamma})^{\frac{1}{n}} \qquad (2)$$

Then, the degradation for the total samples is calculated using the sum of degradation rates multiplied by the time sampling. Finally, the estimated degradation under 5G modulation profile is calculated following eq. (3) for N x 100µs samples, where *sat* and *n* are respectively the saturation and time dependence parameters in the CW aging model and *D* is the total degradation for one 100µs sample.

$$\Delta P_{out}(t) = \frac{1}{\frac{1}{sat} + \frac{1}{(D.N)^{n}}} \qquad (3)$$

The estimated PA degradation under various modulation schemes are presented on Fig. 9 for a total ON time of 10 years. In practice, the actual mission profile of a PA would be around ~50% of that time in order to switch to the receiver (Rx) path. Most of the degradation is visible during the first year of operation, afterwards the Pout drift saturates around 0.5 dB. The degradation rate is highly dependent on the back-off level : the higher the back-off, the lower the degradation rate observed for HCI degradation, as the PA spends less time at high output powers, where most of the degradation occurs. However, this model does not take into account TDDB lifetime even if the same behavior might be expected, as high power is consistent with large voltages seen by the transistors. For all modulation schemes, the absolute level of degradation remains quite low and is consistent with the reliability margins taken in the design phase.



(a) (b)

Fig. 9 : Saturated output power degradation versus time simulated for various modulation schemes for both PAs

The saturation parameter accuracy is crucial for a reliable degradation estimation in the long term. CW stress tests gives evidence of this saturation but its absolute value may be subject to discussion as the test time is limited by probe contact resistance degradation.

C. *Ruggedness measurements results*

Circuit ruggedness are tested using VSWR conditions from 4:1 to a maximum of 7:1 which is the limitation of the tuner capability at 40 GHz. The different time stress on both power amplifiers are shown Fig. 10. The test performed on the 45RFSOI power amplifier is done as follow: the input power is first fixed at IP1dB, the gamma_mag is set to VSWR 4:1 and the gamma phase is swept 3 times from 0 to 350 degree by 10 deg. A 15 sec waiting time is set at every point leading to a total stress of 27 min. Same operation is performed for hard test with gamma phase swept 100 times leading to a total stress of 15h. No breakdown is observed even after 15h of 4:1 VSWR applied. The output power of the 22FDX power amplifier was measured during 60 min VSWR 4:1, also here no breakdown was observed. However, mismatch load on the power amplifiers leads to a degradation over time. The 22FDX amplifier shows an output power degradation of 0.3 dB after 27 min of 4:1 VSWR stress and 0,36 dB after 1 hour. On the 45RFSOI power amplifier, at t0 + 27h VSWR 4:1 an output power degradation of 0,2 dB is observed, and at t0 + 15h VSWR 4:1, a degradation of 0,8 dB.

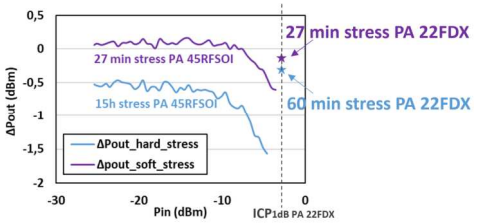


Fig. 10 : pre and post 27 min and 15h VSWR 4:1 stress test: ΔPout (dB) vs. Pin (dBm) for the PA in 45RFSOI(a) and the PA in 22FDX(b)

These measurements show an excellent robustness above expectation up to 7:1 VSWR.

V. Conclusion

Two different power amplifiers in recent node technologies <40 nm in 22FDX and 45RFSOI are tested for reliability and ageing for 10 years use. They are stressed in CW operation and their degradation are modelled using a saturated power law. The 20% de-rating on V_{DD} allows a low stress window as the PA are designed for reliability purposes. The results demonstrate very good reliability and ageing performances. The saturated Pout degradation can be estimated in CW mode. A 5G modulation scheme has been simulated on these circuits and fed to the reliability model. The estimated output power degradation has been calculated for a 10 years operation with this modulated profile, showing a maximum drift of 0.5dB in the worst case, which is very acceptable for the application.

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