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A highly rugged 39 GHz 19.3 dBm Power Amplifier for 5G Applications in 45nm SOI Technology

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***Abstract* —This paper describes a highly rugged power-amplifier for the fifth generation (5G) FR2 new radio (NR) application implemented in a 45nm SOI process (45RFSOI). By using device stacking technique together with an optimized supply voltage reduction, the power amplifier achieves 20 dBm P_{sat} and 23 % PAE_{max}. A P_{avg} of 10 dBm and a PAE_{avg} of 8% is achieved in 64-QAM 200MHz bandwidth OFDM at EVM_{avg} of 6.2% (-24.1dB) without the use of digital predistortion. The 4:1 VSWR measurement shows an excellent PA reliability even under the worst mismatch condition. These results enable an efficient, high power and highly reliable power amplifier for 5G applications.**

***Keywords* — power amplifier, 5G OFDM, 45RFSOI, stacking, realiability**

I. INTRODUCTION

While early 5G systems use the sub-6 GHz frequency band (FR1), with one PA operating at high power to amplify a single-beam omnidirectional signal, the 5G FR2 working at millimeter-wave frequencies uses a different approach. Indeed, most 5G mm-wave applications use phased array antennas to focus and steer multiple beams. This ability to divide the transmission among multiple beams implies that each PA operates at lower power making possible to use silicon technologies instead of GaAs. Among these technologies, the partially depleted CMOS SOI (or RFSOI) has already demonstrated its ability to address handset switches, LNA and antenna tuners. Indeed, thanks to SOI substrate with trap rich layer, sub-6 GHz functions have been drastically improved over years. A better performance for switches linearity, RF-Digital isolation or passive component quality factor has been proved [2]. The remain question is does such type of technology can be used for integrated front-end devices needed for 5G mm-wave handsets, access points or base stations ? This work proposes to demonstrate that a 20 dBm output power at the highest 5G frequency band of 40 GHz can be carry out with a high level of robustness with the 45RFSOI technology.

This paper first discuss on circuit design and specificities of this work. Then, the measured performances in nominal and under stress condition are presented. Finally, a comparison with the state of the art is presented.

II. POWER AMPLIFIER DESIGN

Implementing a >20 dBm level efficient PA in deep sub-micron CMOS at 40 GHz is a challenging task due to the low breakdown voltage of these technologies 0,9 – 1 V. One strategy to generate high output power is to combine or stack unit power cells to achieve the maximum output power.

In this work, we present a two stages PA based on the stack topology using the recently added PAFET drain extended devices that present improved hot carrier injection (HCI) performances and an improved off-state junction breakdown [1]. In any power amplifier in class A, AB or B, the drain to source RF voltage swing of the output stage is $2xV_{supply}$. Therefore, any devices biased at nominal technology voltage is exposed to reliability issue in large signal operation, making them sensitive to HCI and time dependent dielectric breakdown TDDB. It appears that most designs are biased at upper limit, or even boosted sometimes [5][6][7][8]. To design a PA conform for manufacturing, this aspect must be take into account when RF performances are benchmarked. In that work, to solve that issue, power supply is derated by 20 % to secure aging and reliability.

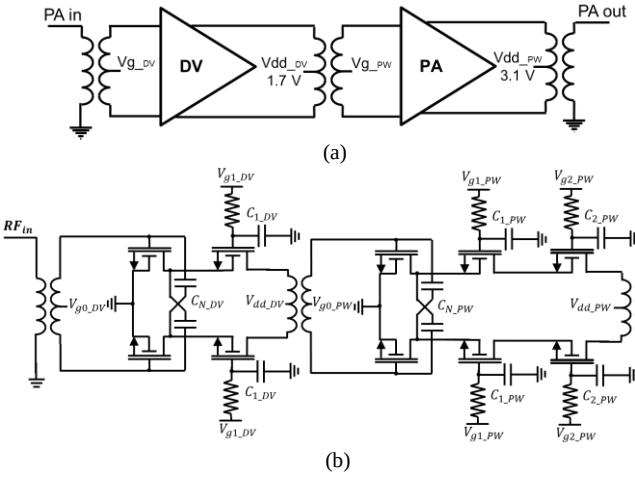


Fig. 1. Power amplifier synoptic (a) and detailed schematic with the DC voltages names (b).

The power amplifier Fig. 1 is composed of a driver stage followed by a power stage to meet both gain and high output power performances. The cascode driver stage is composed of two stacked thin oxide adnfet. The power stage is based on three stacks transistors, two thin oxide L=32 nm PAFET and one thick oxide L=112 nm tonfet. A stack of three transistors alleviates breakdown voltage limits by dividing the voltage swing across several devices. Thanks to the high resistivity substrate, phase variation and losses from one cell of the stack

to another are reduced offering a better power efficiency for stacked power amplifier design [2]. The voltage distribution is obtain with a proper biasing and loading, performed with the gate capacitors on the common gate stages. C_{1_PW} and C_{2_PW} with C_{gs1_PW} and C_{gs2_PW} form a voltage divider that distribute the voltage and respect the breakdown V_{ds} limits and the recommended maximum oxide voltage to secure TDDB degradation.

Common source transistor are stabilized thanks to the neutralization capacitance C_N. The 45RFSOI technology advocate a maximum Vdd voltage of 1.1 V for a thin-oxide transistor and 1.65 V for a thick oxide transistor. De-rating of 20 % is applied on these values giving $V_{dd\_nfet\_max}$=0.88 V and $V_{dd\_tonfet\_max}$=1.32 V. Optimization sizing of transistors size lead to a total width of 200 um for the low voltage FETs and a total width of 300 um for the high voltage FET. The custom-made optimum transformers for matching networks are shown Fig. 2.

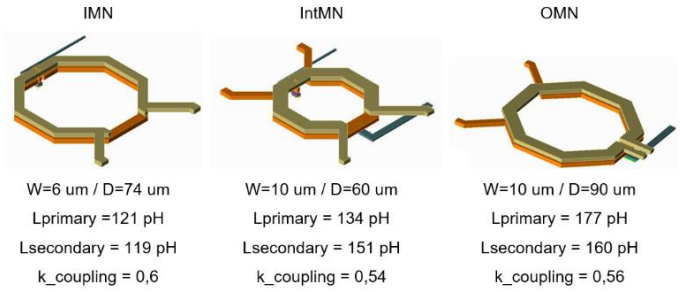
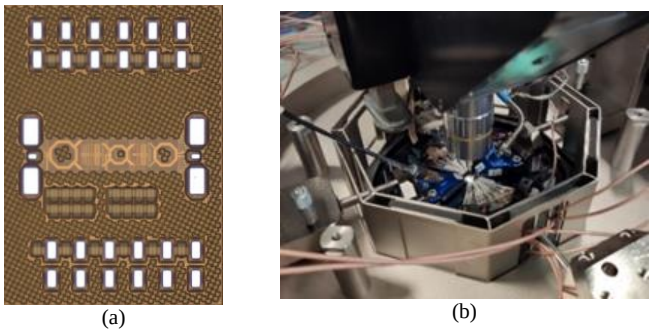


Fig. 2. Matching Network transformers of the Power Amplifier.

III. Measurement Results

The PA is fabricated in 45RFSOI process and occupies a 0.5x0.28 mm² core area (Fig. 3).

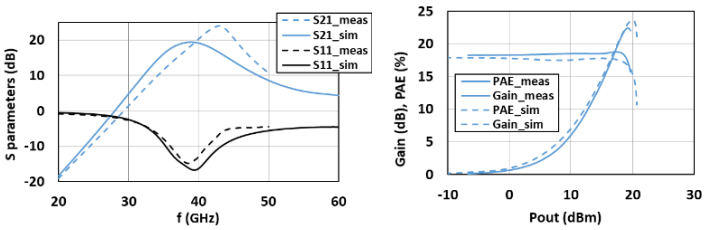


(a) (b)

Fig. 3. Die micrograph of the fabricated PA chip in 45-nm CMOS SOI process (a) and on wafer probing setup (b).

A. Small and Large Signal performance

Small signal measurement are performed with a vector network analyzer (R&S ZVA67). Dedicated coplanar probes are used for 39 GHz measurement. The DC measured current of the driver and power stage are 12 mA and 42 mA respectively. The simulated and measured S-parameters are presented Fig. 4.

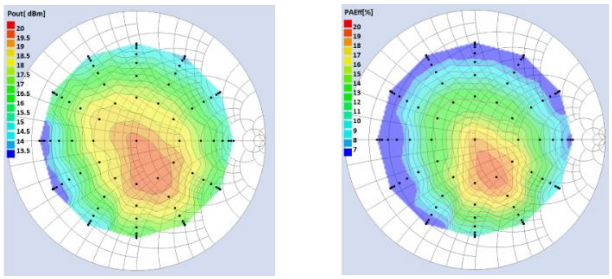


(a) (b)

Fig. 4. S parameters (dB) vs. frequency (GHz) (a) and Gain and PAE vs. Pout of the PA biased at V_{g0_DV}=0,2V, V_{g1_DV}=1.2V, V_{dd_DV}=1.7V, V_{g0_PW}=0.32V, V_{g1_PW}=1.22V, V_{g2_PW}=2.45V, V_{dd_DV}=3.1 V (b).

The power amplifier achieved 19.3 dBm output compression point OCP1dB and saturated power of 20 dBm at 39 GHz (Fig. 4.b). The measured gain is 18.5/23.4 dB at 39/42 GHz and the input return loss S_{11} is <−10 dB over the 36 - 41.3 GHz bandwidth (Fig. 4.a). The maximum PAE is 23 %.

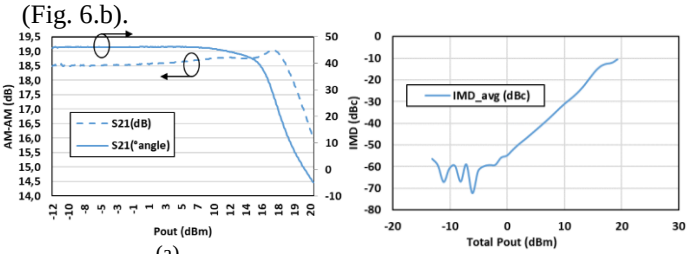
Optimum Z_{opt} is verified by a large-signal load-pull measurement using tuner (Fig. 5) where it can be observed that the PA is well adapted to max output power and efficiency.



(a) (b)

Fig. 5. Load pull measurement at 39 GHz. Power contour level (a) and PAE contour level (b).

On Fig. 6.a AM-AM and AM-PM variations are represented and show less than 0.5 dB and 5° up to 14 dBm. For the IMD measurement, two continuous wave (CW) tones with equal tone power and spaced by 100 MHz are applied to the PA input. The IMD obtain is -30.8 dBc at 10 dBm output (Fig. 6.b).



(a) (b)

Fig. 6. Measured AM-AM (dB) and AM-PM (deg) vs. Pout (a) and IMD3 vs. Pout (b)

B. Dynamic Performance

For modulation measurements, an arbitrary waveform generator (AWG Tektronix 7122C) is used to generate baseband I/Q signals (Fig. 7). The signals are up-converted to 39 GHz using an external mixer with a signal generator to feed the Power Amplifier under Test. The chip output is down converted and analyzed using a real-time oscilloscope

(Tektronix 70 GHz) and Matlab post-processing for OFDM demodulation. The PA is tested using FR2 5G NR OFDM signals with no Digital Pre Distortion and no equalization is applied before demodulation. The PA non linearity contribution to EVM is extracted from the total EVM, as the setup generated unwanted impairments.

Fig. 8 shows modulation tests of 5G NR FR5 200 MHz frame at 39 GHz, modulated with OFDM 64QAM signal. For a power back-off of 9 dB on ICP1dB, the measured Poutavg is 10 dBm and PAEavg is 8 %, while the nonlinear contribution of the PA to EVM is less than 3 % at 39 GHz.

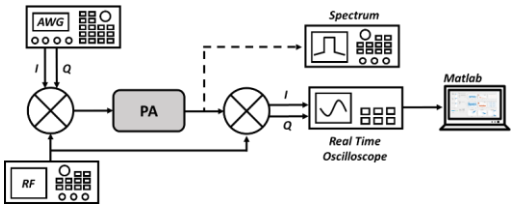
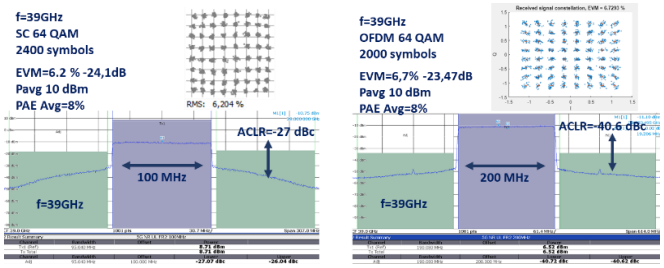


Fig. 7. setup of OFDM modulated measurement.



(a) (b)

Fig. 8. Modulation PA measurement results with SC 64 QAM signal BW=100 MHz (a) and with OFDM 64 QAM BW=200 MHz modulation measurement results at 39 GHz (b).

The Fig 9 shows the EVM degradation induced by the PA function of its power input back off. As a comparison in ETSI TS 138 104, the EVM requirement for Base Station is 8% for 64QAM, measured on 50 MHz bandwidth.

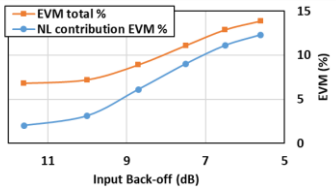
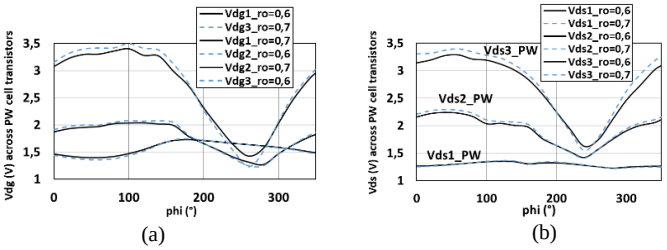


Fig. 9. Measured PA contribution on EVM (%) vs. power input Back Off for OFDM 64QAM modulation, 200MHz Bandwidth.

C. *Reliability Measurements*

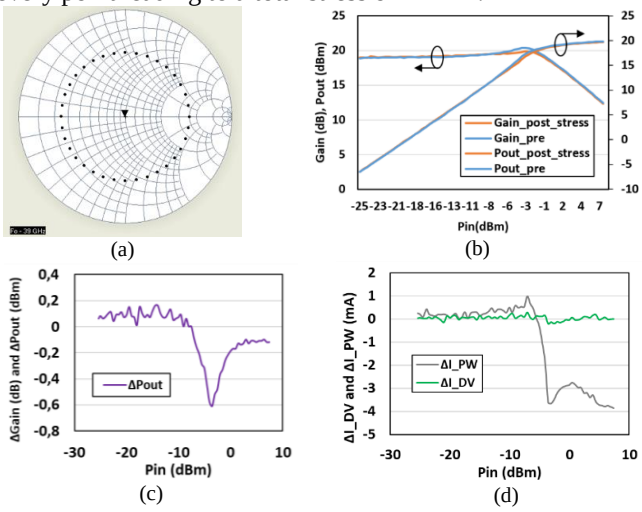


(a) (b)

Fig. 10. Simulation of expected Vds max voltage across power cell stage for different impedances at VSWR 4:1 (rho=0,6) and VSWR 6:1 (rho=0,7) for Vds_PW (a) and Vdg_PW (b).

In a use-case environment, the power amplifier is the latest stage before antenna, making this bloc highly sensitive to load variation. Independently of its performance, its robustness to impedance variation VSWR is of most concern to ensure its functionality. Indeed, the voltage variation expected across transistors versus load impedance can far exceeds the recommended V_{ds} operating voltage.

The simulation Fig. 10 is performed at $P_{out}=P_{1dB}$ for rho=0.6 and 0.7 and covering all phases. The upper thick oxide transistor sees a max V_{ds3max}=3.5 V / V_{dg3max}=3.3 V, and the two cascoded thin oxide transistor a max V_{ds2max}=2 V / V_{dg2max}=2.4 V and V_{ds1}=1.6 V / V_{dg1}=0.8 V. The V_{dsmax} of thick and thin oxide transistors are 2.35 V and 1.8 V respectively. Considering the CCDF of the 5G FR2 modulation scheme, a 0.1-year lifetime at P1dB is evaluated. Therefore, the max voltage should be V_{dgmax} 2.79 V and 1.73 V. Two tests have been performed. A soft stress of 27 min loading presented in Fig. 11, and a hard test corresponding to a longer 15 hours stress in Fig. 12. Blue curves show results before stress and orange curves the results after stress. In Fig. 11, the input power is first fixed at IP1dB, the gamma_mag is set to VSWR 4:1 and the gamma phase is swept 3 times from 0 to 350 degree by 10 deg. A 15 sec waiting time is set at every point leading to a total stress of 27 min.



(a) (b) (c) (d)

Fig. 11. pre and post 27 min VSWR 4:1 stress test (a): Gain (dB) and Pout (dBm) vs. Pin (b), ΔGain (dB) and ΔPout (dB) vs. Pin (c), ΔI_PW (mA) and ΔI_PW (mA) vs. Pin (d).

Same operation in Fig. 12 is performed for hard test with gamma phase swept 100 times leading to a total stress of 15 h. No breakdown is observed even after 15h of 4:1 VSWR, which show a very good robustness against load impedance variation. This measurement was also performed up to 7:1 for 30 min with no breakdown observed. At OCP1dB, after 15h of stress, a degradation of 0.6 dB for the gain and 1.2 % for the PAE is measured and almost no degradation at P_{avg}. However, a more significant degradation is measured before compression. The decrease of this current linearize the PA changing its class of operation. The measurements were made on five PA chips and are perfectly reproducible. Almost no current degradation is observed on the driver current, as this stage is well isolated from output load variation because of the

power call stage between. Degradation can be expected if upper limit supply voltage is applied. Consequently, to insure a given lifetime for a specific power amplifier, the DC and RF voltage must be examined carefully and not over-stressed.

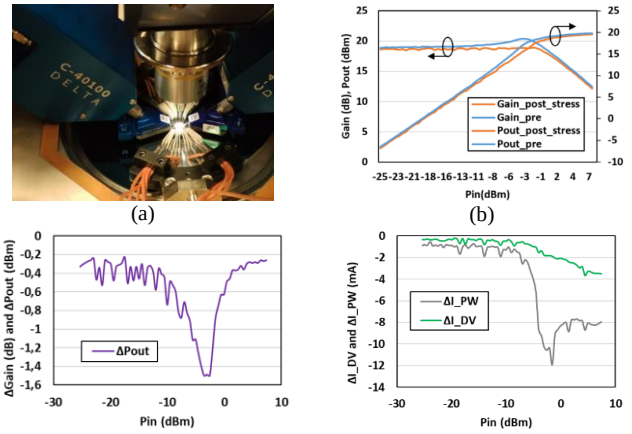


Fig. 12. loadpull setup (a), pre and post 15h VSWR 4:1 stress test: Gain (dB) and Pout (dBm) vs. Pin (b), ΔGain (dB) and ΔPout (dB) vs. Pin (c), ΔI_PW (mA) and ΔI_PW (mA) vs. Pin (d).

IV. Conclusion

Table 1. Summary and comparison of measured performances.

	[4]	[5]	[6]	[7]	[8]	This work
freq. (GHz)	39	38.5	39	39	39	39
Tech.	65nm CMOS	28nm CMOS	22nm SOI CMOS	28nm CMOS	45nm SOI CMOS	45nm SOI CMOS
Process nom. Voltage (V)	1.2	0.9+0.9*	0.8+0.8*	0.9+0.9*	1+1*	1+1.5+1.5*
Supply (V)	-	1.8	1.6	2.2	2	3.1
Gain (dB)	20.3	25.8	15	38	20.5	18.5
P_{sat} (dBm)	16.7	16.8	20.4	26	19.1	19.7
OCP1 (dBm)	13.5	14.9	17.8	21.5	18	19.3
PAE_{max} (%)	22.2	32.9	25.6	26.6	38.6	23
PAE_{P1dB} (%)	14.9	28.8	20.9	13.5	37.3	22.5
Mod. scheme	64QAM	64-QAM 200MHz OFDM	64QAM	5G NR FR2 64-QAM 50MHz OFDM	5G NR FR2 64-QAM 800MHz OFDM	5G NR FR2 64-QAM 200MHz OFDM
EVM (dB)	-26.3**	-25.3	-25	-26	-25.1	-24.1
ACPR (dBc)	-	-30	-24.5	-33	-26.1	-27
P_{avg} (dBm)	7.1**	10.3	13.5	14.7	10.2	10
PAE_{avg} (%)	-	16.9	10.6	-	13.4	8
Core Area (mm^2)	-	0.07	-	-	0.21	0.14

*Added values when devices are stacked, **At 28GHz

Table 1 summarizes the performances of this work and the recently reported 5G SOI/Bulk CMOS PA power amplifiers in the mmW 39 GHz band. The presented PA has been characterized with true 5G NR FR2 modulation scheme and verified under VSWR 4:1 to accurately evaluate the robustness and the capability of the technology.

Maximum output power requirement for beamforming system reduces as number of elements increases, making SOI technologies a good candidate for 5G applications. Aging and reliability are most concern: power amplifier must be robust from environment variation while keeping good performances over time. In this paper, a highly rugged 39 GHz power amplifier with an output power at P_{1dB} of 19.3 dBm, 18.5 dB gain and a PAE_{P1dB} of 22.5 % is presented. These good results were achieved thanks to stacking device technique, offering high output power while securing FET from breakdown. As the author's knowledge, this is the only PA published at 39 GHz meeting 5G required performances with derating supply voltage and where reliability has been verified.

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