Influence of substrate resistivity on porous silicon small-signal RF properties

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***Abstract*— This article provides guidelines to design porous silicon (PS) layers regarding optimization of small-signal properties in passive structures for radio frequency (RF): insertion loss and crosstalk. Results are based on high-frequency measurements on 200-mm wafers and electromagnetic simulations up to 40 GHz. Using substrate resistivity below 1 Ω cm allows the best tradeoff with minimized PS thickness.**

***Index Terms*— Crosstalk, linear attenuation coefficient, porous silicon (PS), S-parameters, substrate resistivity.**

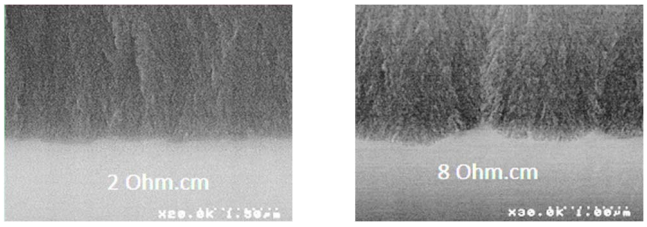

Fig. 1. Cross-sectional imaging of the Si/PS interface for two distinct substrate resistivities, using scanning electron microscopy.

I. Introduction

With the advent of pervasive mobile and wireless devices, porous silicon (PS), a long studied material [1]–[3], attracts a renewed interest as blanket or local substrate material for radio frequency (RF) applications [4]–[6]: it is compatible with Si technology and offers lower permittivity and higher resistivity than Si.

The latter helps to reduce signal propagation loss (attenuation). Using PS benefits a wide range of devices including coplanar waveguides (CPWs), inductors, and filters [6]. There are reports indicating that for a given device geometry, increased PS thickness improves device performance [7], [8]. However, the systematic effect of starting bulk silicon resistivity on RF small-signal properties has not yet been described with PS.

In this article, we report for the first time on the impact of silicon resistivity on substrate loss of CPW made on PS. First, we fabricated CPW on PS variants (made with different thicknesses on silicon with variable resistivity). We then measured the S-parameters of CPW fabricated on these substrates up to 40 GHz. A simple high frequency structure simulator (HFSS) [9] model reproduces these measurement results. This model enables predicting the impact of substrate resistivity on CPW substrate loss and crosstalk, allowing to draw guidelines for the design of future RF PS layers.

II. Experimental

A. PS Fabrication

We prepared blanked PS layers starting from 200-mm p-type doped silicon wafers with resistivity in the 1–2-Ω · cm and 5–10-Ω · cm ranges, respectively. For each resistivity, Si substrates were electrochemically anodized in hydrofluoric acid (35%) with isopropanol as surfactant and a current density of 14 mA/cm^2. The thickness and porosity of these layers were determined using differential weighting and cross section scanning electron microscopy. Fig. 1 illustrates the morphology of these layers. For each resistivity, layers of 12- and 20-μm thickness were fabricated. In all samples, porosity was estimated close to 50%.

B. CPW Fabrication

After PS formation, a thin (400 nm) silicon dioxide layer was deposited by plasma-enhanced chemical vapor deposition

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Fig. 2. Material stack used in the fabrication of CPW on PS.

at 260 °C. The wafers were then coated with 100 nm of titanium and 1 μm of gold. Photolithography and wet etching lead to the patterning of this metal stack into CPW transmission lines (see Fig. 2). RF probing pads with 100-μm pitch allow CPW connection.

C. S-Parameter Measurements and Parameter Extraction

Scattering parameters were measured between 100 MHz and 40 GHz using an Anritsu 37369A Vectorial Network Analyzer and ground–signal–ground (GSG) probes from Cascade. Measurements were carried out on different CPW pairs differing only by their lengths (500 and 1500 μm). RF pad parasitic contributions were removed using Mangan's method proposed in [10]. Losses were calculated as follows:

$$\alpha_C = R/2Z_0 \quad (1)$$

$$\alpha_G = GZ_0/2 \quad (2)$$

$$\alpha_{\text{total}} = \alpha_G + \alpha_C \quad (3)$$

where α_C and α_G are the respective contributions of metallic conductor and substrate material to α_{total}, the total loss of the CPW. R and G are the linear resistance and conductance values of the *resistance–inductance–capacitance–conductance* (*RLCG*) equivalent model of the transmission line and Z_0 relates to its characteristic impedance.

III. Results and Discussion

A. Choice of CPW Dimensions

Losses were extracted on two contrasting CPW geometries: a narrow signal line with small signal-to-ground gap (S/G = 10 μm/4.6 μm) and a wide signal line with a large signal-to-ground gap (S/G = 70 μm/42 μm). Both CPW lines have a 50-Ω characteristic impedance for a 3-kΩ · cm Si substrate without PS. Fig. 3 presents the results obtained on two different Si substrate resistivities.

For the compact CPW, it is noticeable that conductor contribution dominates losses. This originates both from the higher linear resistance of the signal line and from reduced substrate losses, as electromagnetic fields are mainly confined within the low-loss PS layer. In contrast, in the wide signal-line and large gap configuration, the substrate component (including bulk Si contribution) determines CPW linear loss. For this reason, the investigation of substrate resistivity impact focuses on the larger layout.

B. HFSS Electromagnetic Simulations

Different configurations were implemented in the HFSS software [9], using parameter values listed in Tables I and II.

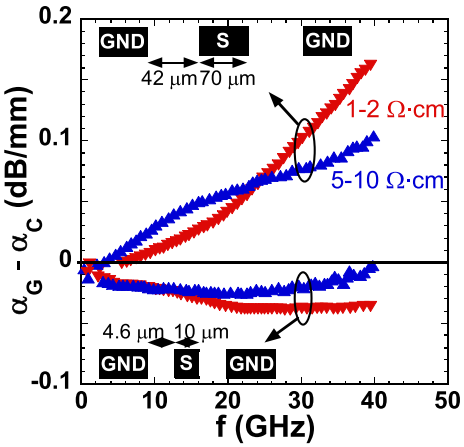

Fig. 3. Experimental difference between conductor and substrate contribution to propagation linear loss versus frequency, on 20-μm-thick PS layers, as a function of CPW geometry and substrate resistivity.

TABLE I
Stack Description

Thickness (µm)				
Au	*Ti*	*SiO₂*	*PS*	*Si Substrate*
1.0	0.1	0.4	5→200	700

TABLE II
Electrical Properties

Intrinsic properties at 824 MHz					
Layer	*Au*	*Ti*	*SiO₂*	*PS*	*Si*
ε_r	1.0	1.0	3.9	4.5	11.9
ρ (Ω·cm)	$2.30\cdot10^{-6}$	$4.17\cdot10^{-5}$	$1.0\cdot10^{18}$	$10^6\cdot\rho_{Si}$	10^{-2}→50

In these structures, the substrate resistivity was chosen to be 1.5 and 7.5 Ω · cm for hardware in the respective 1–2-Ω · cm and 5–10-Ω · cm resistivity ranges. PS layer resistivity value was set in agreement with [11]. The relative permittivity value of 4.5 originates from [12] and best describes the permittivity around 50% porosity.

Fig. 4 compares measured and simulated losses as a function of frequency, on CPW structures with the same dimensions: 70-μm-wide signal line, 308-μm-wide surrounding ground lines separated by a 42-μm-wide gap. Two variants of silicon resistivity are combined with two variants of PS layer thickness (12 and 20 μm).

The loss values in this work are of the same order of magnitude as literature data with similar stacks: in [7], losses of 1.5 dB/mm at 40 GHz have been reported on 15-μm-thick PS on 1–3-Ω · cm Si and with a gap of 2.5 μm. In this work, this value is obtained with a 20-μm PS layer. The difference is due to CPW geometry: in our case, this was selected in order to maximize substrate impact, not to optimize performance (which would require narrower line-to-ground gaps as in [7]).

The obtained trend agrees with literature data showing that increasing PS thickness yields attenuated losses [7]. Comparing at 16 GHz, increasing PS thickness from

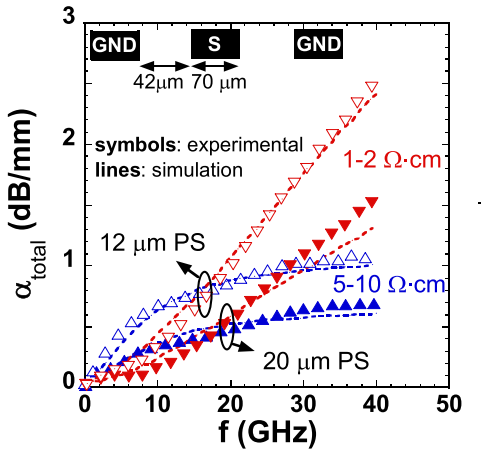

Fig. 4. Total linear propagation loss as a function of frequency, on 12- and 20-μm PS layers, for two different substrate resistivities. Symbols denote measurement results and dashed lines denote HFSS simulation output.

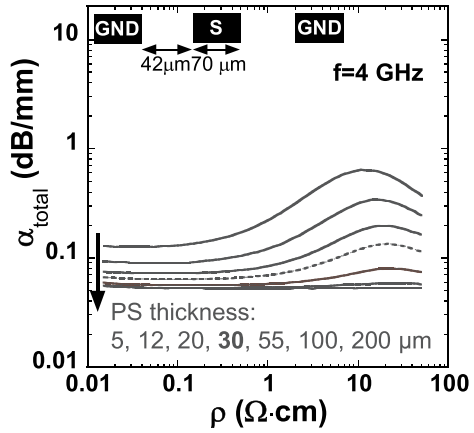

Fig. 5. HFSS simulated total attenuation as a function of substrate resistivity, for various PS thickness values, at 4 GHz.

12 to 20 μm decreases attenuation coefficients from 0.8 to 0.4 dB/mm.

The change in substrate doping has a strong impact on the attenuation dependence on frequency. Below 16 GHz, for a given PS thickness, it is more favorable to use 1.5 than 7.5 $\Omega \cdot$ cm. This trend reverses at higher frequencies, especially with thinner PS.

In all cases, the simulations capture the observed dependence on PS thickness and Si substrate resistivity. In order to have a better insight of these trends, HFSS simulations were performed to investigate wider parameter ranges.

C. Simulated Dependence of Loss on Resistivity

Fig. 5 presents simulated attenuation coefficients for PS layers between 5- and 200-μm thickness, on Si substrates in the 10–50-$\Omega \cdot$ cm resistivity range, at a fixed frequency of 4 GHz.

For those thickness and resistivity ranges, the variation of the characteristic impedance of the chosen coplanar line is between 30 and 80 Ω.

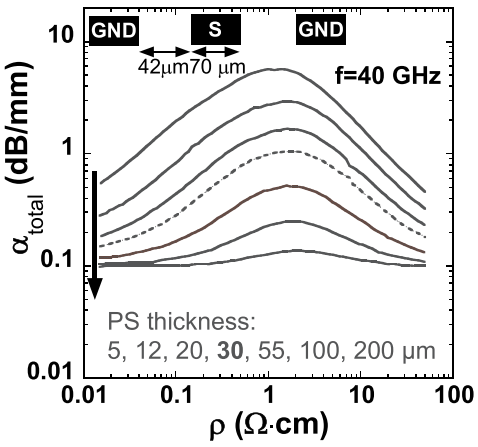

Fig. 6. HFSS simulated total attenuation as a function of substrate resistivity, for various PS thickness values, at 40 GHz.

Both PS thickness and substrate resistivity appear to influence the observed trends.

For each PS layer thickness, attenuation reaches a peak value in the 10–20-$\Omega \cdot$ cm resistivity range.

1) For higher resistivity values, eddy currents fade, reducing losses.
2) For lower resistivity values, the electromagnetic field is mainly confined into the PS layer, which also dims eddy currents.

The 10–20-$\Omega \cdot$ cm resistivity range leads to a worst case regime where both mechanisms are most ineffective.

The effect of substrate resistivity is amplified in the case of thin PS layers. Conversely, substrate resistivity influence on losses decreases as soon as PS layer thickness reaches a sufficiently high value (which is around the same order of magnitude as CPW signal-to-ground spacing).

The exercise was repeated at 40 GHz. Fig. 6 summarizes the corresponding main results.

Worst case attenuation values appear in the 1–2-$\Omega \cdot$ cm resistivity range, which is one order of magnitude lower than the 4 GHz case.

In that resistivity range, the peak attenuation value increases with frequency (about 10-fold higher than at 4 GHz). The dependence of the peak attenuation value on PS layer thickness seems relatively unchanged.

Minimum attenuation appears for the thickest PS layers and is weakly dependent on substrate doping. This minimum level is higher than in the case of 4 GHz operation. Both observations can be explained by the fact that metallic conductor contribution determines the minimum value and skin effect sets its frequency dependence.

D. Simulated Dependence of Crosstalk on Resistivity

Fig. 7 compares the simulated magnitude of S_{21} versus frequency between 100 MHz and 40 GHz, for three different substrate resistivities, with 20-μm-thick PS layer, on a coplanar test structure with 25-μm coupling distance and 150-μm coupling width, as described in the inset of Fig. 7.

While S_{21} bears a weak dependence on substrate resistivity below 1 GHz, only the 0.15-$\Omega \cdot$ cm resistivity case shows

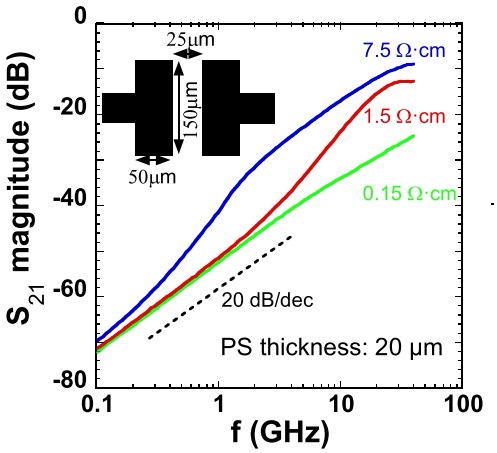

Fig. 7. HFSS simulated S_{21} magnitude as a function of frequency for three different substrate resistivities, using a 20-μm PS layer, extracted on a coplanar structure.

a 20-dB/decade capacitive coupling behavior over the whole frequency range. It is thus mandatory to use low-resistivity ($<$1 $\Omega\cdot$cm) silicon in order to minimize 25-μm-range crosstalk up to 40 GHz.

E. Guidelines for PS Layer Design

At a given frequency and for a given PS layer thickness, Figs. 5 and 6 suggest that a given loss target value could be achieved with different substrate resistivities in the 10^{-2}–50-$\Omega\cdot$cm range.

However, it might be preferable to use low-resistivity silicon as a default starting material.

1) It requires relatively thin PS layers for low-frequency operation.
2) It contributes in minimizing crosstalk over the whole frequency range.
3) It allows keeping the same PS features, as changing Si resistivity can affect PS morphology [13].

IV. Conclusion

This article reports the first systematic evaluation of substrate resistivity influence on the attenuation coefficient of CPWs fabricated on various thicknesses of PS.

First, we fabricated CPW on PS variants (with different thicknesses and made on silicon substrates with variable resistivity). We then measured the S-parameters of CPW fabricated on these substrates up to 40 GHz. HFSS simulation reproduces these measurement results. This enables the prediction of the substrate resistivity impact on CPW substrate loss and crosstalk.

At each frequency, there is a substrate resistivity range in which attenuation is maximal, suggesting that either low or high resistivity could provide well-controlled attenuation values with minimum PS thickness. At the same time, simulations suggest that low substrate resistivity is necessary to minimize crosstalk up to high frequencies.

While 1-$\Omega\cdot$cm substrate resistivity is suitable for PS to operate in the sub-6-GHz domain, we recommend using lower resistivity silicon if the PS layers are meant to be compatible with a wider range of operating frequencies.

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