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A Self-referenced and regulated sensing solution for PCM with OTS selector

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Abstract— Phase change memory (PCM) device associated with Ovonic Threshold Switch (OTS) selector is a proven solution to fill the gap between DRAM and mass storage. This technology also has the potential to be embedded in a high-end microcontroller. However, programming and reading phases efficiency is directly linked to the selector's leakage current and the sneak-path management. To tackle this challenge, we propose in this paper, a new sense amplifier able to generate an auto-reference taking into account leakage current of unselected cell, including a regulation loop to compensate voltage drop due to reading current sensing. This auto-referenced sense, built on the charge-sharing principle, is designed on a 28nm FDSOI technology and validated through extensive Monte-Carlo and corner cases simulations. From the simulation results, our sense amplifier is demonstrated to be robust for an ultra-large range of sneak-path current and consequently for a large range of memory array size, suitable for embedded memory in high-end microcontroller.

Keywords— PCM, OTS, non-volatile memory sensing, sneak-path compensation.

I. INTRODUCTION

The evolution of edge computing, with A.I. and data-intensive treatment, exacerbates the requirement in terms of performances and memory capacity on edge devices, such as the high-end Micro Controller Unit (MCU). In this context, high-density memory based on emerging concept could replace actual solutions such as 1.5T NOR Flash memory or 1T1R Phase Change Memory (PCM) [1-7]. In this context, to decrease drastically the bit cell footprint, a back-end selector solution could be adopted. Doing so, this new embedded solution could rely on the most mature back-end memory solution namely Phase Change Memory (1R) associated with Ovonic Threshold Switch (OTS) selector (1S) [8-12], forming an 1S1R bit cell. However, due to process compatibility in an embedded context, OTS may require specific adjustments. Beyond the well-known feature of PCM cells already demonstrated in the literature, i.e. a large resistance ratio of 10^3 , a low variability thanks to a bulk phase change (crystalline and amorphous state), a mature process, and a large endurance 10^9 [4-7], the performances of memory with OTS as selector is mainly driven by the OTS selectivity. Regarding the OTS selectivity feature, numerous papers have reported very different performances [9][13][14], with selectivity ranging from 10^3 to 10^7 .

The impact of the selectivity of the OTS at array level is characterized by the level of the leakage current on the

unselected cells during the programming and the reading operations. Thus to compensate for the impact of this leakage, defined also as sneak-path current, some design techniques have been already proposed:

- The first technique proposed to limit the sneak-path current impact is based on well-chosen biasing conditions applied on the unselected row or column in the memory array. These techniques are namely $V/2$ and $V/3$ biasing solutions [15].
- The second technique is based on sneak-path current measurement during a first pre-programming or pre-reading phase in order to adapt the biasing voltage to compensate for the amount of sneak current [16].
- The third technique consists in collecting a mean sneak current coming from a compensation port and subtract it from a reference [17] during the operation.

As shown, compensation schemes are must-have solutions when dealing with crossbar array, but to the best of our knowledge, sensing circuit solution with auto-compensation of the leaky current and autoregulation of the row and column biasing has never been proposed at circuit level targeting a large range of OTS selectivity. In this context, the main contributions of this paper are as follows:

- We introduce, for the first time, an auto-referenced sense amplifier for PCM associated with OTS as a selector, where sensing reference is self-adapted to the leakage level. (sec. II & III)
- We also introduce a regulation loop to dynamically change the biasing conditions of the lines in the array depending on the sneak-path current but also on the reading current through the selected cell. (sec. II & III)
- We carry out functional (sec. III) and extensive Monte-Carlo simulations taking into account global and local variability, as well as corner cases PVT, to demonstrate the robustness of our solution for a large range of OTS selectivity (sec. IV).

II. PROPOSED SENSING SOLUTION OVERVIEW

In array consisting of 1S1R bit cell, as presented in the introduction, using a half bias ($V/2$) strategy during a read operation, the cells sharing the same column and the same row as the accessed cell are half biased, inducing sneak-path currents. The consequence is twofold:

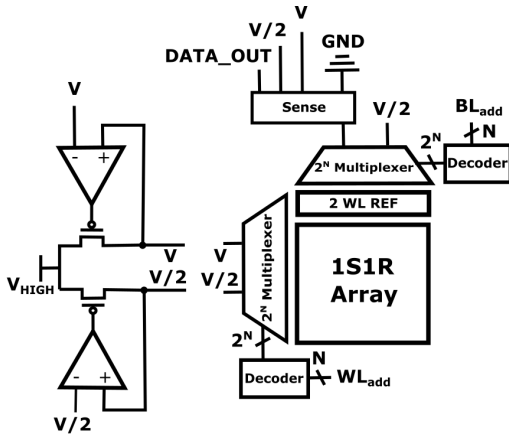


Fig. 1. Global architecture scheme, including LDO to generate V and $V/2$ voltages regulated from our sense amplifier regulation loop

- The row sneak-current uses extra-current than the one needed to read the cell with a risk of drop-out of the read voltage V .
- The column sneak-current adds an extra-current to the one crossing the accessed cell with the risk of blurring the cell read current.

Both sneak-path currents of course depend on OTS selectivity as well as array size, these two parameters are being linked. Consequently, any sensing solution developed for 1S1R array should be able to:

- Regulate the applied read voltage V on the selected lines and $V/2$ on the unselected lines to compensate for large read current due to sneak-path and read current above the OTS selector's hold current [18].
- Compensate the sneak-path current to solely isolate the contribution of the read current crossing the accessed cell.

Our proposition follows these two requirements. First of all, as illustrated in Figure 1, knowing the read voltage to be applied on the array, we use a regulator loop inside the sense amplifier solution to compensate the read voltage drop due to the current sensing, which is dependent on the accessed PCM cell state (HRS or LRS) but also of the sneak-path current amplitude. The principle is to add to the read voltage V and respectively $V/2$, the voltage drop in the sense amplifier in order to have a constant voltage applied on the selected cell.

In a second time, we also introduce two references row as depicted in Figure 2. The two references rows exhibit 1S1R cells with for each column a PCM in HRS and one in LRS. The main idea is to sense, prior to the selected cell of a given column, both reference cells sharing the selected column. Doing so, we preserve the sneak-path current context, and we are able to generate a voltage reference that cancels the sneak-path current. The reference generation is built using the charge sharing principle, in three functional phases. During the first phase, the sense input capacitor is charged using the LRS 1S1R reference cell resulting in a capacitor-voltage given in (1).

$$V_{IN} = \frac{(I_{LRS} + I_{sneak}) * T}{C} \quad (1)$$

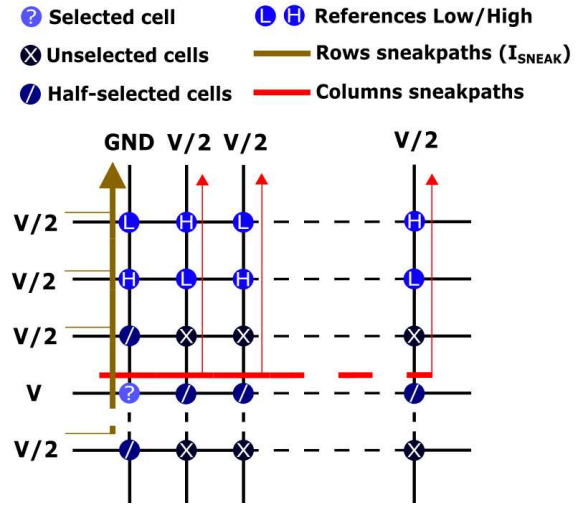


Fig. 2. 1S1R array with 2 references rows, illustrating also row sneak path and column sneak path during bit cell selection.

With T the charging time, C the sense input capacitor, I_{LRS} the current through the LRS 1S1R cell reference, and I_{sneak} the sneak path current of the selected column.

During the second phase, the input capacitor is further charged using the HRS 1S1R reference cell, resulting in a new capacitor-voltage given by:

$$V_{IN} = \frac{(I_{LRS} + I_{sneak} + I_{HRS} + I_{sneak}) * T}{C} \quad (2)$$

With I_{HRS} the current through the HRS 1S1R cell reference.

In the third phase, a charge sharing process occurs, using a reference capacitor equal to the input capacitor C . Doing so, the reference voltage is given by:

$$V_{REF} = \frac{(\frac{I_{LRS} + I_{HRS}}{2} + I_{sneak}) * T}{C} \quad (3)$$

Thus when reading the selected cell, the input capacitor voltage is determined by:

$$V_{IN} = \frac{(I_{CELL} + I_{sneak}) * T}{C} \quad (4)$$

And knowing that C and T are the same in (3) and (4), it is straightforward to see, that the sneak current is compensated and that I_{CELL} (the selected cell current) is compared solely to $\frac{I_{LRS} + I_{HRS}}{2}$.

It is also important to note that any temperature drift in the 1S1R cell might be compensated by this self-reference generation.

III. SENSE AMPLIFIER CIRCUIT DESCRIPTION

A. Circuit description

The full scheme of our new self-referenced sensing solution is illustrated in Fig.3. It is composed mainly of three blocks:

- The regulation block (Fig.3.a), which is mainly composed of two current mirrors generating the reference voltages V and

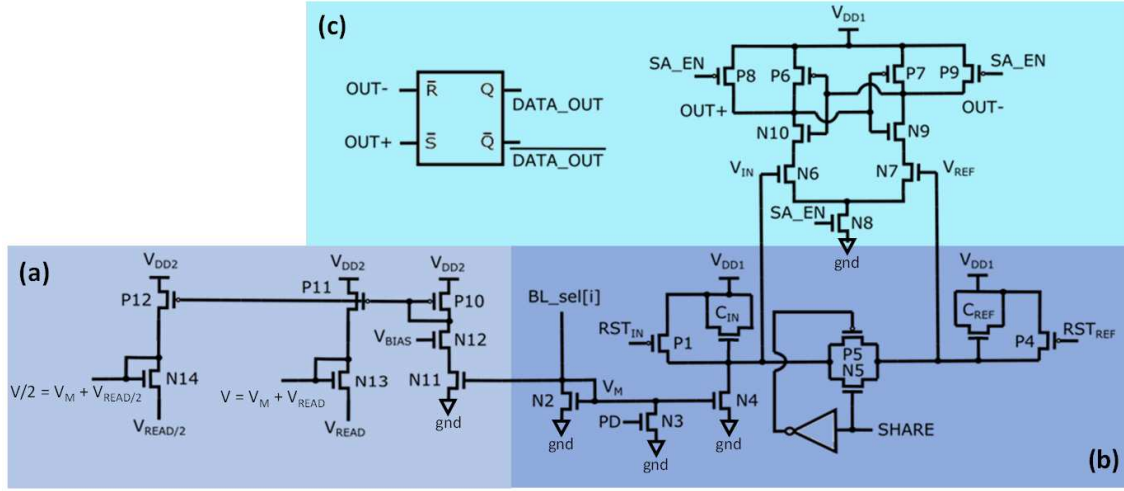


Fig. 3. Schematic of the proposed sense circuit with three main blocks: (a) the regulation block, (b) the capacitor block and (c) the comparator block

$V/2$, used as input for the LDOs biasing the array rows and columns, from respectively the inputs V_{READ} and $V_{READ}/2$

- The capacitor block (Fig.3.b), which exhibits the input capacitor C_{IN} and the reference capacitor C_{REF} both equal to the same value C . They are used for auto-reference generation through charge-sharing.
- The comparator block (Fig.3.c), which is built with a StrongARM comparator [19] followed by an RS latch to produce the sense output $DATA_OUT$.

Regulation block: The regulation block allows to copy voltage V_M and to add its value during the current sensing, including cell current and sneak-path current, on both input voltages V_{READ} and $V_{READ}/2$ to generate $V = V_M + V_{READ}$ and $V/2 = V_M + V_{READ}/2$. Actually, during the current acquisition, since the current might be high, V_M is increasing, thus it is mandatory to regulate the biasing applied on memory array rows and columns to do not collapse the applied voltage on the selected cell. Please note, that N12 safeguards N11 from high swing voltage and needs adequate biasing for quick regulation. P10, P11, and P12 form two current mirrors, and N13, N14 act as an active charge in order to create the set points.

Capacitors block: The principle of current acquisition is based on the voltage discharge of the input capacitor C_{IN} through a current mirror composed of N2 and N4. Thus, prior to any current acquisition, C_{IN} is charged to V_{DD1} through P1 by pooling down signal RST_{IN} . In a similar way, before any reference voltage generation, through sharing activation (signal $SHARE = '1'$), C_{REF} is charged to V_{DD1} through P4 by pooling down signal RST_{REF} . A pull-down transistor N3 is added to ensure that N4 is cut-off during two current acquisition phases in order to do not disturb the voltage stored on C_{IN} . The sharing between C_{IN} and C_{REF} is ensured by an analog switch (N5, P5) controlled by the signal $SHARE$ (active high).

Comparator block: The comparator block is designed with a StrongARM comparator followed by an RS latch. This block compares the two inputs voltages V_{CIN} and V_{CREF} to generate the digital output.

B. Functional validation

The proposed solution has been designed using a 28nm FDSOI technology from STMicroelectronics, using two different supply voltages: low V_{DD1} equal to 1.0V and middle voltage V_{DD2} equal to 5.5V.

Fig.4 illustrates the self-reference generation followed by a read operation on an HRS cell and a read operation on an LRS cell. The self-reference generation takes 3 phases, whereas any successive read operations take 2 phases each. Please note, that to ease the representation all addressing changes, row selection, and column multiplexer activation, have been set here to 1ns as for the sense circuit internal signal change. Of course, addressing timing varies accordingly to the array size and the memory controller feature, when the sense amplifier is embedded in a full memory chip. It is also important to note that; even if the reference generation principle remains similar to the one presented in section II, we proceed with capacitor discharge and not charge to minimize current copy circuitry.

Self-reference generation: During the 1^{st} phase, the sense amplifier is disconnected from the memory array, accordingly the signal PD is activated and the reset signals (RST_{IN} and RST_{REF}) are activated with a low value to charge both capacitors to V_{DD1} , doing so both capacitor voltages are initialized and $V_{IN} = V_{REF} = V_{DD1}$. Please note that the signal PD is activated, whenever the sense circuit is disconnected from the array. After this 1^{st} phase, the self-reference generation process starts with the selection of first the LRS cell reference and after with the selection of the HRS cell reference, during this complete process, the signal $SHARE$ is activated, thus the discharge occurs simultaneously on both C_{IN} and C_{REF} . With this strategy, the charge sharing between both capacitors is realized during the acquisition. Thus, during the 2^{nd} phase, the sense amplifier is connected to the memory array (PD is disabled) and both capacitors are discharged following (5):

$$V_{IN} = V_{REF} = V_{DD1} - \frac{(I_{LRS} + I_{sneak}) * T}{2C} \quad (5)$$

It is also important to notice that since the read current I_{LRS} plus the sneak-path current I_{sneak} are absorbed by the structure, the

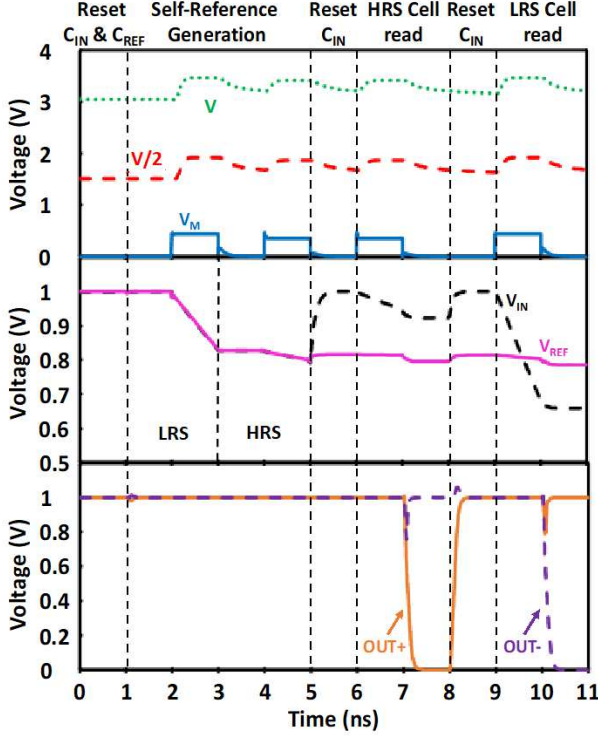


Fig. 4. Simulation of the proposed sense operation, with the self-reference generation (Reset both capacitors & reference generation), followed by the sensing of a cell in a HRS (reset in and read) $V_{IN} > V_{REF}$ and $OUT+ = 0$ and respectively of a LRS cell (reset in and read) $V_{IN} < V_{REF}$ and $OUT+ = 1.0V$. Regulated signal are also represented during all phases.

potential V_M rises and has to be added to the regulated voltages V and $V/2$. After the second phase, the sense is first disconnected from the array, the HRS cell reference is addressed, and when the signals are stabilized in the memory array, the sense amplifier is again connected, here also with the *SHARE* signal activated. During this 3rd phase, here also with regulated loop activated, both capacitors are again discharged, thus the resulting voltages on the capacitors can be expressed following (6):

$$V_{IN} = V_{REF} = V_{DD1} - \frac{(I_{LRS} + I_{HRS} + 2 \cdot I_{sneak}) \cdot T}{2 \cdot C} \quad (6)$$

This process, similarly to the principle described in section II, creates a reference voltage image of the mean of the I_{LRS} and I_{HRS} including the sneak path current of the acceded column I_{sneak} . It is interesting to note that the self-reference generation takes three phases, after that, only the input capacitor will have to be charged to V_{DD1} and discharge accordingly to the state of the cell to be read, in two phases. Another advantage of this self-referencing scheme is that after a reference generation and until the leakage current of the MOS (P4, P5, N7, and N5) degrades the voltage reference V_{REF} , numerous reading phases can be performed on the cells of the same column in burst mode, before refreshing the reference voltage.

Read operation: Before any read operation, it is mandatory to disable the *SHARE* signal and to reset the input capacitor by activating the RST_{IN} signal. Doing so during the 1st phase of a read operation the voltage V_{IN} is again initialized to V_{DD1} . In the

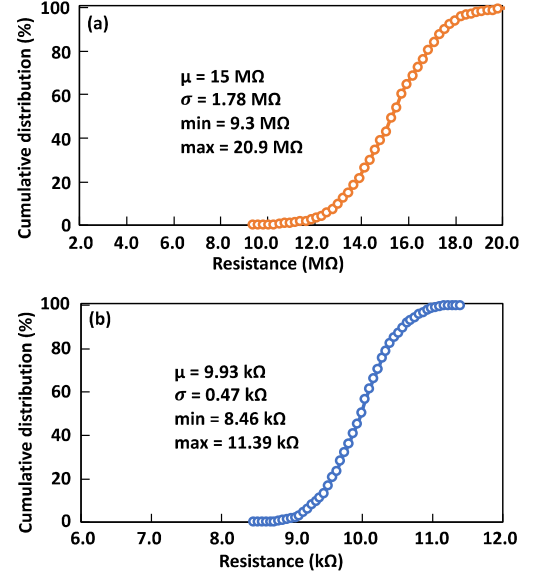


Fig. 5. Equivalent resistance cumulative distribution, used to simulate OTS and PCM variability with (a) OTS in off state during the read operation of a PCM in HRS state and, (b) OTS in on state during the read operation of a PCM in LRS state

2nd phase of the read operation, the sense amplifier is connected to the memory array and the input capacitor is discharged by the read current, accordingly to the state of the addressed cell, while considering the sneak path current I_{sneak} . Depending on the state of the addressed cell, the voltage V_{IN} is above (HRS) or below (LRS) the voltage reference V_{REF} . The comparator is then activated latching the output on the two internal nodes $OUT+$ and $OUT-$. Please note, that the regulation process is also active during the read operation 2nd phase.

IV. SENSE AMPLIFIER VALIDATION

A. Sense robustness versus variability

The sizing of our new sense amplifier is defined to target, 10μA of sneak path current, corresponding to the OTS characteristics reported in [18] and considering a 1Mb array. The simulation timings are the ones presented in Fig.4. First of all, the energy consumption of the sense amplifier has been extracted from simulations in nominal case, per block and per operation (self-reference generation, HRS, and LRS cell read), as shown in Table I. As expected, since a large current is involved during reference generation and LRS read, these operations are the most consuming. The regulation loop is the main contributor, whereas the consumption of the two other blocks remains below the tens of fJ.

TABLE I. SENSE AMPLIFIER ENERGY CONSUMPTION

Blocks	Operations		
	Ref. generation	HRS cell read	LRS cell read
Regulation	1.465 pJ	384 fJ	1.28 pJ
Capacitors	16.6 fJ	1.05 fJ	15.2 fJ
Comparator	0.052 fJ	0.3 fJ	0.68 fJ
Total	1.48 pJ	385.4 fJ	1.3 pJ

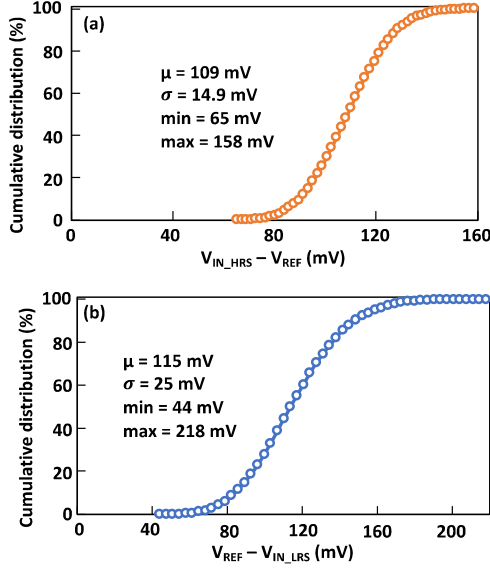


Fig.6. Margin window cumulative distribution with (a) $V_{IN_HRS} - V_{REF}$ for a read operation on a PCM HRS and (b) $V_{REF} - V_{IN_LRS}$ for a read operation on a PCM LRS.

Then, to analyze the robustness of our sense solution, we first run an extensive set of simulations to take into account Process – Voltage – Temperature variations. Voltage variations are classically set to -10%, nominal, and +10% of the V_{DD1} defining 3 corner cases: 0.9V, 1V, and 1.1V. The operating temperature variations are also defined with 3 corner cases: -55°C, 27°C, and 125°C. So, the validation of our sense solution is performed against this set of 9 corner cases. For the process variations, we consider global as well as the local source of variability at $-3\sigma/+3\sigma$, including mismatch on the typical process corner, considering the implementation of common centroid and inter-digitized layout in order to reduce the mismatch between capacitor and StrongArm comparator. For all simulated voltage and temperature corners, 1000 runs are performed to take into account the process variations. Regarding the OTS and PCM variability, we have extracted dispersion reported in [18] for the OTS and in [20] for the PCM respectively. From these extractions and knowing that during a read operation on a PCM in LRS with OTS-on and a PCM in HRS with OTS-off, we have considered a Gaussian distribution whose mean value is 9.93k Ω and standard deviation is equal to 470 Ω and another Gaussian distribution whose mean value is 15M Ω and standard deviation is equal to 1.78M Ω , respectively (Fig.5).

Fig.6.a reports the margin window ($V_{IN} - V_{REF}$) between the input capacitor voltage V_{IN} and the reference capacitor voltage V_{REF} , considering our 9 Voltage-Temperature corners and with 1000 Monte Carlo runs for each corner, in the case of a read operation on a PCM HRS (noted V_{IN_HRS}). Respectively, Fig.6.b reports the margin window ($V_{REF} - V_{IN}$) in the same conditions, but for a read operation on a PCM LRS (noted V_{IN_LRS}). Both margin windows exhibit a positive value of 65 mV and 44 mV, validating the robustness of our sense solution. This robustness

strongly relies on the auto-reference generation, compensating even worst-case variations.

B. Sense robustness versus OTS characteristics and array size

Keeping the same sizing and timing constraints, the proposed sense solution is evaluated versus different levels of sneak-path current to assess the robustness of the design with different OTS selector characteristics and different array sizes. The evaluated conditions are reported in Table II with for each pair of OTS selector characteristic/array size, the corresponding theoretical sneak-path current.

TABLE II. SNEAK PATH CURRENT I_{SNEAK}

$I_{sneak[ij]}$ (A) at $V/2$	$n \times n$ array size			
	10 kb	1 Mb	100 Mb	3.2 Gb
OTS from [13]: 10 pA	10 nA	100 nA	1 μ A	6 μ A
OTS from [18]: 1 nA	1 μ A	10 μ A	100 μ A	600 μ A
OTS from [14]: 50 nA	50 μ A	500 μ A	NA	NA

Please note, that sneak-path currents above 1mA are discarded as non-realistic values in memory chip design-space exploration (noted NA in Table II). The sneak path current is calculated as follow:

$$I_{sneak} = \sum_{row=0}^{n-1} I_{sneak[i]} \quad (7)$$

with $I_{sneak[ij]}$ a single cell sneak-current when the OTS is biased at $V/2$ and n is the number of rows in the array.

The simulation results for a typical case are reported in Fig.7 with the V_{IN} voltage for a read operation on a PCM in HRS (noted V_{IN_HRS}), respectively on a PCM in LRS (noted V_{IN_LRS}), and the V_{REF} voltage versus the sneak-path current given Table II. One can first notice that the auto-reference generation technique is efficient for a broad range of sneak-path current. Actually, for sneak-path current ranging up to 600 μ A, the reference voltage level is well balanced in between the LRS voltage level and the HRS voltage level. However, due to the sizing of the capacitor block (Fig.3.b), when the input current overcomes a given limit (around a few hundreds of μ A), one can observe two effects. The first one is a too large potential capacitor-discharge, with possibly V_{IN} and V_{REF} close to the NMOS threshold voltages (noted as operating limit in Fig.7),

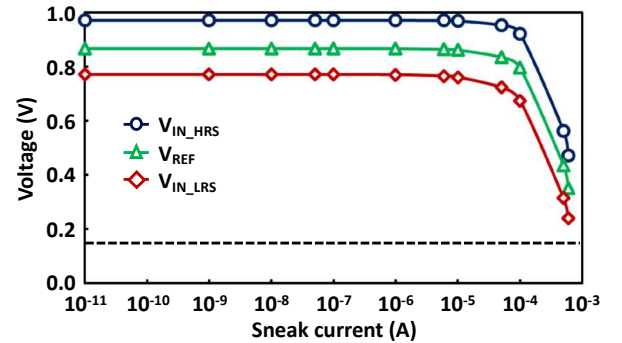


Fig.7. Input voltage V_{IN} (corresponding to the read of a PCM HRS and respectively a PCM LRS) and voltage reference V_{REF} evolution versus the identified conditions given Table II for various OTS selector characteristic and array size.

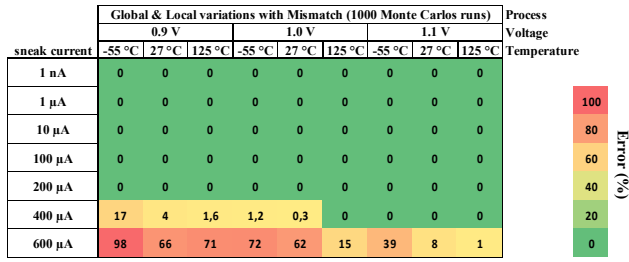


Fig.8. Pass/Fail results (shmooplot) of the PVT simulation of the proposed sensing circuit for various sneak-path currents.

with a direct impact on the comparator response time and an over-sensitivity to mismatch. The second effect is a nonlinear discharge of the capacitor due to the polarization regime change of the transistor N4, however since the reference is auto-generated, this effect remains partially compensated. Thus depending on selector characteristics as well as array size, careful sizing of the capacitors C_{IN} and C_{REF} has to be adopted. Finally, it is worth noting, that using body bias options, the threshold of the MOS at the inputs of the comparator can be trimmed to enhance the sense robustness to large sneak-path current for a given sizing.

C. Overall sense robustness

Finally, our sense amplifier is benchmarked on various sneak-path current for the 9 predefined corners with Monte Carlo simulations (1000 runs) to include process variations. Fig.8 presents a shmoo plot of the pass/fail sensing results considering the corners cases and the process variation versus different sneak path current values. The first errors occur for a sneak-path current of 400 μ A for the most severe voltage corner case. The errors are mainly due to the low voltage corner (0.9V) since this corner reduces the dynamic across the capacitor, leading to 17% of reading errors. For extreme sneak-path current the solution exhibits errors, whatever the corner, meaning that the C_{IN} and C_{REF} sizing is not sufficient to deal with the extreme amount of sneak-path current. Besides, for this high sneak path, the errors are mainly due to voltage corner (0.9V) together with low temperature corner. For all other cases representing a large range of sneak-currents including the targeted one (10 μ A), due to the auto-reference generation, our new sensing solution has clearly demonstrated its robustness.

V. CONCLUSION

In this work, we propose for the first time a sense amplifier suitable for OTS selector and PCM memory. The main advantage of our sensing solution, is to generate, just when necessary, a self-reference that takes into account the sneak-path current. Thanks to this self-reference generation, the leakage current during the read operation of a 1S1R cell is fully compensated. Moreover, we also introduce a regulation loop to apply a constant reading voltage on the selected cell whatever the sensing current. Finally, we have demonstrated the exceptional robustness of our approach through extensive corner cases and Monte-Carlo simulations, and thus for a broad range of sneak path current, corresponding to various OTS features and/or memory array size. This new sensing solution opens the way to a robust OTS selector and PCM memory reading operation in high-end microcontroller products.

REFERENCES

- [1] Hang-Ting Lue et al, "3D AND: A 3D Stackable Flash Memory Architecture to Realize High-Density and Fast-Read 3D NOR Flash and Storage-Class Memory", IEEE International Electron Devices Meeting (IEDM), 2020
- [2] Hang-Ting Lue et al, "A Vertical 2T NOR (V2T) Architecture to Enable Scaling and Low-Power Solutions for NOR Flash Technology", IEEE Symposium on VLSI Technology, 2020
- [3] F. La Rosa et al, "40nm embedded Select in Trench Memory (eSTM) Technology Overview", IEEE 11th International Memory Workshop (IMW), 2019
- [4] M. Carissimi et al, "2-Mb Embedded Phase Change Memory With 16-ns Read Access Time and 5-Mb/s Write Throughput in 90-nm BCD Technology for Automotive Applications", IEEE Solid-State Circuits Letters, vol. 2, no. 9, sep. 2019
- [5] G. Navarro et al, "Highly Sb-Rich Ge-Sb-Te Engineering in 4Kb Phase-Change Memory for High Speed and High Material Stability Under Cycling" IEEE 11th International Memory Workshop (IMW), 2019
- [6] E. Nolot et al, "Germanium, antimony, tellurium, their binary and ternary alloys and the impact of nitrogen: An X-ray photoelectron study", Applied Surface Science, vol. 536, Jan. 2021
- [7] F. Disegni et al, "Embedded PCM macro for automotive-grade microcontroller in 28nm FD-SOI", Symposium on VLSI Circuits, 2019
- [8] M. Laudato et al, "ALD GeAsSeTe Ovonic Threshold Switch for 3D Stackable Crosspoint Memory" IEEE International Memory Workshop (IMW), 2020
- [9] Anthonin Verdy et al, "Improved Electrical Performance Thanks to Sb and N Doping in Se-Rich GeSe-Based OTS Selector Devices", IEEE International Memory Workshop (IMW), 2017
- [10] C. Laguna et al, "Innovative Multilayer OTS Selectors for Performance Tuning and Improved Reliability", IEEE International Memory Workshop (IMW), 2020
- [11] Solomon Amsalu Chekol et al, "Thermally Stable Te-based Binary OTS Device for Selector Application", Non-Volatile Memory Technology Symposium (NVMTS), 2018
- [12] S.R. Ovshinsky, H. Fritzsche, "Amorphous semiconductors for switching, memory, and imaging applications", Transactions on Electron Devices, 1973, vol. 20, issue 2
- [13] A. Verdy et al, "Optimized Reading Window for Crossbar Arrays Thanks to Ge-Se-Sb-N-based OTS Selectors", IEEE International Electron Devices Meeting (IEDM), 2018
- [14] W.C. Chien et al, "Comprehensive Scaling Study on 3D Cross-Point PCM toward 1Znm Node for SCM Applications", Symposium on VLSI Technology, 2019
- [15] Jiwei Li et al, "New write operation scheme for alleviating effect of line resistance on RRAM crossbar array", IEEE Advanced Information Management, Communicates, Electronic and Automation Control Conference (IMCEC), 2016
- [16] A. Levisse et al, "SneakPath compensation circuit for programming and read operations in RRAM-based CrossPoint architectures", 15th Non-Volatile Memory Technology Symposium (NVMTS), 2015
- [17] Woorham Bae et al, "A Variation-Tolerant, Sneak-Current-Compensated Readout Scheme for Cross-Point Memory Based", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 12, 2018
- [18] J. Minguet Lopez et al, "Optimization of RRAM and OTS selector for advanced low voltage CMOS compatibility", IEEE International Memory Workshop (IMW), May 2020, Dresden, Germany. pp.1-4
- [19] Behzad Razavi, "The StrongARM Latch [A Circuit for All Seasons]", IEEE Solid-State Circuits Magazine, vol. 7, no.2, 2015
- [20] G.Lama et al, "Reliability analysis in GeTe and GeSbTe based phase-change memory 4 kb arrays targeting storage class memory applications", Microelectronics Reliability, vol.114, Nov. 2020