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ABSTRACT Nowadays, many electronic systems store valuable Intellectual Property (IP) information inside Non-Volatile Memories (NVMs). Encryption mechanisms are widely used by designers in order to enhance the integrity of such IPs and protect them from any kind of unauthorized access or modification. At the same time, often such IPs are critical from a reliability standpoint. Thus, dedicated techniques are employed to detect possible reliability threats (e.g., transient faults affecting the NVM content). The weights of a neural network (NN) model (e.g., integrated into an object detection system for autonomous driving or robotics) are a typical example of precious IP from both security and reliability standpoints. Indeed, NN weights often constitute proprietary data, stemming from an extensive and costly training process; moreover, their correctness is key for the NN to work reliably. In this article, we explore the capability of encryption mechanisms to ensure protection from both security and reliability threats. In particular, we applied several encryption mechanisms to two neural network applications to secure their weights and we assessed, via extensive fault injection campaigns, the fault detection that they provide. Experimental results show that by cleverly choosing the proper encryption scheme it is possible to achieve very high fault detection rates (greater than 99%) with respect to Multiple Bit Upsets. The gathered results pave the way to the integration of reliability and security mechanisms to achieve better results with lower costs.

INDEX TERMS Artificial Neural Network, Convolutional Neural Network, Encryption, Fault Detection, Fault Injection Campaign, Non-Volatile Memories, Reliability, Security

I. INTRODUCTION

INFORMATION technology is a major aspect of the modern society. Digital systems have become widespread, considerably changing the way people interact with computing machines. The design process and the architectures of electronic systems have evolved considerably since their emergence several decades ago. Nowadays, designers must take into consideration several constraints, including those related to reliability, and follow standards such as DO-254 for avionics and ISO-26262 for automotive in order to meet certain criteria and thresholds. These constraints derive from the needs of safety-critical systems. Indeed, these systems must be able to detect a sufficiently high percentage of faulty conditions that could compromise their correct operation, thus avoiding incurring critical failures, which in turn could endanger human lives or cause large economical losses.

In the last years, also the interest towards security-oriented techniques to prevent possible attacks to such systems has been exponentially growing. These attacks aim to either change the behavior of the systems or extract private and/or precious information (*Intellectual Property* or *IP*) from them [1]. Some of these IP data items are stored into Non-Volatile

Memories (NVMs) that are an attractive target for malicious users due to the persistence of the data [2]. Studies has been conducted to evaluate and mitigate the security threats for NVMs [3]. NVMs are also prone to faults, caused by, for example, radiation effects. In order to harden the memories with respect to faults, designers typically adopt redundancy solutions (e.g., Error Correction Codes, or ECCs) able to detect the occurrence of single- and multiple-bit errors and to possibly correct some of them [4], [5], [6]. On the other side, when the content of a memory represents a valuable IP, designers protect it against possible attacks via encryption [7].

A prime example of a system where both safety and security play a crucial role is an autonomous system [8] that employs Machine Learning (ML) technology [9], [10]. Machine learning is a widely adopted technology in various sectors such as healthcare [11], automotive [12], [13], [14] and aerospace [15]. In these scenarios, the weights of the ML model represent a valuable asset [16] for the system since they are strongly linked to the application's overall functionality. Furthermore, the weights are the result of a typically long (hence, expensive), non-intuitive training process of the model. As a result, the weights of a ML model represent a valuable IP for the system and are typically stored into NVMs that shall not be compromised or tampered with.

At the moment, existing solutions to protect the NVM content are not designed to provide protection from faults and from malicious attacks at once. In fact, reliability experts decide about the former ones, while security experts deal with the latter, often with limited interactions between the two groups. This work originates from the observation that encryption mechanisms may also offer some interesting fault detection capabilities, since in some cases they tend to amplify the effect of faults, making them more manifest, and thus detectable. Hence, studying the reliability features of different encryption solutions becomes attractive. This enables taking also reliability into account when selecting the most suitable encryption mechanism for a given system. Indeed, we believe that designers needing to adopt encryption mechanisms in their systems may benefit from the intrinsic fault-detection capability of such mechanisms. This, in turn, facilitates the achievement of the target reliability goals for the system.

In this work, we experimentally evaluate the positive effects that data encryption may have in terms of reliability enhancements with respect to the effects of possible transient faults. In particular, we focus on systems having NVMs already provided with the encryption/decryption mechanisms to protect the stored data from malicious attacks. As case studies, we resort to an Artificial Neural Network (ANN) and a Convolutional Neural Network (CNN), whose weights represent the IP, encrypted and stored in the NVM. In our experiments, we inject faults in the encrypted weights and analyze their effects on the Neural Network behavior and the system fault detection capabilities with and without encryption. We perform various experiments with different ciphers and extensive fault injection campaigns to evaluate the effect of the encryption on the system fault detection capabilities. The gathered experimental results show that by carefully selecting a cryptographic algorithm, we can achieve a very high rate of fault detection, in particular with respect to Multiple Bit Upsets (MBUs). Hence, this work paves the way to a more clever selection of an encryption mechanism not only protecting the stored memory content with respect to malicious attacks, but also providing a sufficiently high reliability degree.

In this article, we integrate and extend the results of the work presented in [17]. In particular, the major contributions of this work are the following.

1) A thorough analysis of the fault tolerance capabilities of different operational modes of the *Advanced Encryption Standard (AES)*, widely employed for memory encryption.
2) Extensive experimental validation of AES fault tolerance capabilities on a new case study, a Convolution Neural Network (CNN). To the best of our knowledge, this is the first work studying the AES fault tolerance capabilities in the context of a CNN.

Experimental results show that a particular AES mode – the Propagating Cipher FeedBack (PCBC) encryption mechanism with padding – allows achieving nearly 100% fault detection for both considered Neural Networks with respect to the Single Event Upset (SEU) faults model and the Multiple Bit Upset (MBU) faults model with multiplicity varying from 10 to 500.

The remainder of the article is organized as follows. Section II reports an overview on the state-of-the-art work on NVM reliability and provides a preliminary background on memory encryption. Section III illustrates the study that we conducted. Section IV details both case studies along with the experimental setup. Section V illustrates the obtained experimental results and, finally, Section VI draws the conclusions.

II. STATE-OF-THE-ART AND BACKGROUND

NVMs (e.g., flash memories) are being widely used as a storage medium for numerous devices since they are characterised by high performances with low power consumption and large storage density. They are used by designers in various business sectors e.g., the mobile-phone industry and the automotive industry. However, there is a notable difference between the two aforementioned domains. In the latter, the memory design criteria are strongly influenced by safety standards (e.g., ISO-26262), since the memory is meant to be used in safety-critical systems on board of the vehicle. Conversely, when realizing systems which can hardly endanger human lives (such as a mobile-phone), the design constraints tend to be more relaxed. For example, the data retention rate in an embedded flash memory that is planned to be used in a car spans from 10 to 20 years; in the case of a mobile phone, the stored data last for a maximum of 5 years. Moreover, devices expected to be in the field for a long period of time are prone to error accumulation primarily due to aging of the hardware components. Furthermore, designers have to consider that NVMs are prone to errors due to radiation effects

[18], [19] and to error accumulation. A recent study [20] reports an unexpected error explosion phenomenon in flash memories, where multiple errors occur in flash blocks over several operation cycles that exceed the ECCs detection and correction capabilities.

The reliability of NVMs has been extensively studied [21]. Also, numerous design methodologies, based on ECCs, have emerged over the years in order to enhance the resilience of NVMs to (soft and hard [22]) errors. As prominent examples, we can mention the IBM's Chipkill used in combination with dynamic bit-steering [23] and the Intel's Lockstep [24]. The security of NVMs has been also thoroughly studied [25], [26].

Typically, reliability and security are two aspects that are accounted for separately and independently. The main objective of our work is to pave the way to new approaches combining the two aspects. To do so, we analyze the inherent fault-tolerance features of a prominent and widely-used security mechanism, i.e. the encryption.

In the next subsection, we report an extensive background on memory encryption.

A. MEMORY ENCRYPTION

NVMs are particularly sensitive in terms of security. Their ability to permanently retain the stored information makes them easily exploitable by invasive attacks. Through chip decapsulation an attacker can obtain direct access to the NVM surface and perform several kinds of attacks. One common threat is IP stealing. This is achieved by reading out the content of the NVM, which normally contains application code and data that represent a valuable IP for the company producing the target system. Another threat stems from the possibility for the attacker to tamper with the NVM content and provoke malfunctions in the processing elements that could ultimately result in privilege escalation on the system. A famous example is the code reuse attack and its variants, such as Return-oriented Programming (ROP) [27], [28] and Jump-oriented Programming (JOP) [29].

In this article, we focus on machine learning applications based on neural networks for safety-critical systems. In this context, the weights of the neural network stem from a long and expensive training process making them a valuable asset. Moreover, in many safety-critical applications the computing systems are deployed in close proximity to the user, making them easily accessible for the purpose of the aforementioned physical attacks.

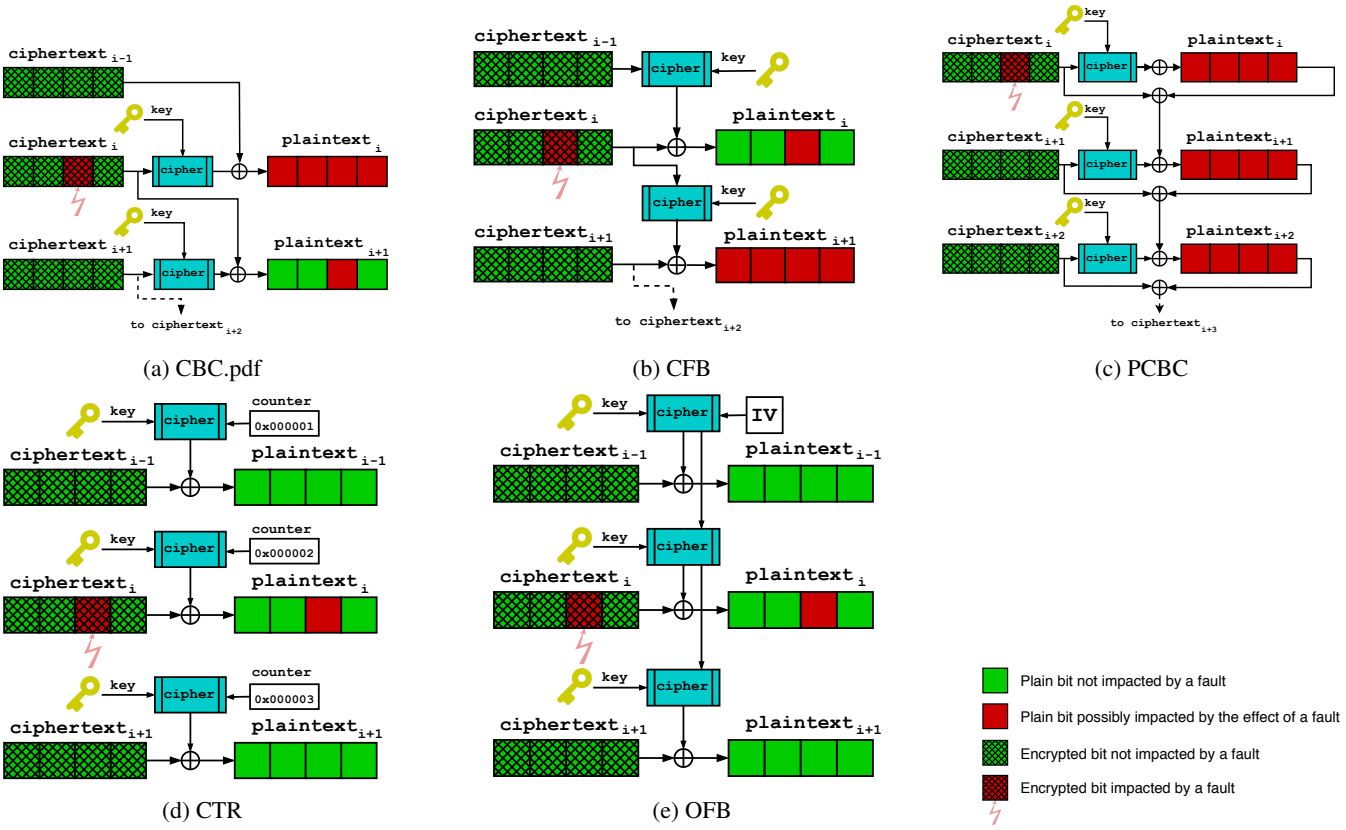
Memory encryption is a powerful mechanism for counteracting such threats. If the NVM content is fully encrypted, an attacker that obtains the physical access to the memory is not able to perform the aforementioned attacks. In fact, even if the attacker is able to read out the memory, the encryption makes the understanding of its content impossible. Moreover, encryption makes tampering-based attacks much more complex: an attacker would have to modify the encrypted data so that the decryption mechanism transforms them into data causing the desired corrupt behavior.

However, encryption alone is not capable of exhaustively detecting memory corruptions. More powerful techniques based on integrity primitives (e.g., authenticated encryption) are capable of protecting computing systems against most kinds of perturbations (i.e., fault attacks) that involve the memory content [30] [31]. In this article, we do not deal with artificial faults induced by an attacker, but we focus on natural faults coming from environmental sources instead. Although many similarities exist between artificial and natural faults, these are two problems that are traditionally dealt with very different technologies. In fact, protection mechanisms against fault attacks are based on security techniques possibly based on cryptographic primitives (e.g., the already mentioned authenticated encryption), while natural faults are dealt with memory hardening techniques (e.g., error correcting codes). In this article, we introduce the possibility of dealing with natural faults relying on techniques belonging to the security domain. We consider very simple memory encryption techniques, without the additional cost of the data integrity primitives, and we evaluate their properties in aiding the processing system at detecting natural faults that can possibly affect the data stored into the NVM.

We consider a memory encryption implementation where data are loaded into the NVM already encrypted. When data are read by the processing element (in our case, a general-purpose CPU) they are streamed through a hardware decryption module that is interposed between the NVM and the CPU. The encryption algorithm is based on a symmetric cryptography primitive, where the same secret key is used for both encryption and decryption. In the memory decryption scenario, the secret key must be stored inside the decryption module, possibly hardwired inside the module logic in order to avoid easy access through invasive attacks.

On the same architecture, we evaluate several encryption algorithms, all based on the Advanced Encryption Standard (AES), which can be implemented according to different *modes of operation*. The common element is a pseudo-random permutation (PRP) that processes a 128-bit block of plaintext in order to generate a 128-bit block of ciphertext. The PRP is conceived in order to have the following characteristics:

1) The permutation is dependent on the secret key. This implies that if the key is not known, the permutation looks like a random transformation, hence it is unfeasible to derive the corresponding plaintext only by knowing a ciphertext.
2) The permutation is invertible. This allows to build the decryption function using the same key.
3) The permutation has *confusion* and *diffusion* properties. This means that each bit of the output is dependent on all the 128 bits of the input. For the fault detection purpose, this is a very important property because the corruption of one bit on the input block results in the corruption of the whole output block. In the following, we will refer to this property as *fault spreading*, that is related to the multiplicity and to the location of the errors stemming from a single bit error on the input message.



(a) CBC.pdf (b) CFB (c) PCBC

(d) CTR (e) OFB

FIGURE 1: Decryption process of different AES modes of operations and their related fault spreading property

The AES basic PRP, also called *block cipher*, allows to build several types of ciphers with different characteristics (i.e., different modes of operation).

III. ANALYSIS OF THE AES FAULT DETECTION CAPABILITY

In this section, we detail the thorough analysis that we performed on the fault detection capabilities of different encryption mechanisms. In particular, we provide a definition of the different AES modes highlighting their capability to spread the fault effects.

A. AES MODES OF OPERATION AND THEIR FAULT PROPAGATION PROPERTY

In the following, we detail the modes of operation that we analyze in this article, highlighting their fault propagation properties:

- **Cipher Block Chaining (CBC) mode**: in this mode of operation, each block of plaintext is added to the previous ciphertext block before being encrypted. This way, each ciphertext block depends on all plaintext blocks processed up to that point. In the decryption function, each plaintext block is added to the previous ciphertext after decryption. This implies that a 1-bit corruption on the ciphertext block i is propagated to the whole 128-bit plaintext block i, plus to 1 bit of the plaintext block $i+1$. This is due to the fact that the addition operation (i.e., a bit-wise XOR) does not spread the fault, but it simply transmits it to the corresponding bit of the result (Figure 1a). Thus the fault spreading of the CBC mode is equal to 1 block plus 1 bit of the next block.
- **Cipher Feedback (CFB) mode**: in this mode of operation, each ciphertext block is computed as the sum of the corresponding plaintext block plus the encryption of the previous ciphertext block. In the decryption function, each plaintext block is computed as the sum of the corresponding ciphertext block and the encryption of the previous ciphertext block. Here, the encryption of the ciphertext block i is used as a keystream for both the encryption and the decryption of the block $i+1$. This implies that a 1-bit corruption on the ciphertext block i is transmitted to the corresponding bit of the plaintext block i, and it is also spread over the entire block $i+1$ (Figure 1b). Thus the fault spreading of the CFB mode is equal to 1 bit in the present block plus the entire next block.
- **Propagating CBC (PCBC) mode**: in this mode of operation, each block of plaintext is added to both the previous plaintext block and the previous ciphertext block before being encrypted. This leads to a similar decryption behavior, i.e., each block of plaintext is added

to both the previous plaintext block and the previous ciphertext block after the decryption function. This implies that a 1-bit corruption on the ciphertext block i is spread over the plaintext block i, plus all the following blocks up to the last one (Figure 1c). Thus the fault spreading of the PCBC mode is equal to the number of blocks that are present between the block where the fault has happened and the last block of the encrypted data.

- **Counter (CTR) mode**: in this mode of operation, the encryption function is applied to a sequence of values that are generated by a counter initialized by a seed. The resulting output blocks (i.e., the keystream) are added to the plaintext blocks in order to obtain the ciphertext blocks as result. The decryption operation is performed generating the same keystream and adding it to the ciphertext blocks in order to obtain the plaintext blocks. This implies that a 1-bit corruption on a ciphertext block is propagated to the same bit on the resulting plaintext block (Figure 1d). Thus, the fault spreading of the CTR mode is equal to 1 bit in the same encrypted block.
- **Output Feedback (OFB) mode**: in this mode of operation, a keystream is generated starting from an initialization value that is passed through the encryption function multiple times. The ciphertext block is obtained as the sum between the plaintext block and the corresponding keystream block. In the decryption operation, the same keystream is generated (i.e., starting from the same initialization value) and this is added to the ciphertext blocks to compute the corresponding plaintext blocks. This implies that a 1-bit corruption on a ciphertext block is propagated to the same bit on the resulting plaintext block (Figure 1e). Thus the fault spreading of the OFB mode is equal to 1 bit in the same encrypted block.

From this point forward, we separate the AES modes of operation into two different categories, according to their fault spreading property.

- **Non-spreading category** including the CTR and the OFB modes of operation.
- **Spreading category** including the CBC, CFB and PCBC modes of operation.

In the *non-spreading* category, the faults on the ciphertext are not spread over the plaintext during decrpytion, but they are simply trasmitted to the corresponding bit. Conversely, modes of operation in the *spreading* category are able to spread the effect of one-bit corruption on the ciphertext over at least an entire block of plaintext.

B. THE ROLE OF PADDING IN AES

Block-based encryption needs *padding* to work properly. Indeed, since the encryption is performed on 128-bit blocks, it is necessary to conceive a way to deal with plaintexts whose size is not multiple of 128 bits. The *padding* standards are conceived in order to add to the plaintext the number of bytes required to reach a multiple of 16 bytes (i.e., 128 bits). Thus, the size of the resulting ciphertext is always a multiple of 16 bytes. After decryption, the extra padding bytes are removed to obtain the original plaintext. The procedure used by the decryption module to determine the number of bytes that must be removed is mandated by the standard. One of the most popular padding technique for block ciphers relies on the PKCS #7 - RFC 2315 standard [32]. According to this standard, if n bytes are added to pad the last block, then each of these bytes will encode the value n. After decryption, the last byte of the resulting plaintext is read, and its value determines the number of bytes that must be discarded. To provide an example, let us imagine a plaintext message of 100 bytes, which corresponds to 6 128-bit blocks plus 4 bytes. In order to complete the seventh block, 12 bytes are added as padding. Therefore, each padding byte will contain the value `0x0C` (12 in decimal). After decryption, the presence of the value `0x0C` on the last byte of the plaintext implies two things:

(i) the last 12 bytes of the resulting plaintext must all encode the value `0x0C`;
(ii) the last 12 bytes of the resulting plaintext must be removed after decryption.

C. FAULT TOLERANCE ANALYSIS

The phenomena described in Subsection III-A entail different consequences for the system.

The *non-spreading* modes of operation do not exacerbate the fault effect, leaving it confined to a specific bit of the plaintext. From a fault tolerance standpoint, a fault has the same probability to be masked or detected by the system or by the running application as if no encryption was applied. Conversely, the *spreading* modes of operation aggravate the fault effect by extending it to multiple bits of the plaintext. From a fault tolerance standpoint, this could potentially entail worse consequences if no extra detection mechanism is available in the hardware platform or in the running application.

Therefore, using the spreading AES modes of operation may seem extremely counterproductive, as it aggravates the fault effects and does not help detecting their presence. However, as mentioned in Subsection III-B, the padding standard introduces some redundancy that may improve the fault-tolerance. Indeed, storing the information about the number of added padding bytes into the padding bytes themselves (`0x0C` in the example in Subsection III-B) is not strictly necessary for the correct operation of the encryption. Nonetheless, the redundancy turns out being a powerful property for the purpose of fault detection. In fact, considering the above example, if the value `0x0C` appears on the last byte, but not all the 12 last bytes contain the same value, the decryption operation can detect and signal a decryption error.

Concerning the AES operation modes described in Section III-A, for the padding check to be used for fault-detection, the effect of a fault must reflect on the padding bits. In general, the event of having a fault impacting a padding bit is as probable as for the other bits. Thus, for non-spreading operation modes, the presence of padding check is not likely

to have a significant impact on fault-tolerance. Conversely, when the fault effect is extended to other bits (as in spreading operation modes), the probability of obtaining a corrupted padding increases, and so does the detection capability. In details, CBC and CFB (Figures 1a and 1b) operation modes propagate the effect of a fault occurring on a single ciphertext bit only to the corresponding plaintext block and to the next one. Therefore, also these two operation modes are not much likely to benefit from the padding check. Nevertheless, the PCBC mode (Figure 1c) has the interesting property to propagate a fault in a given block to all the successive blocks, all the way to the padding blocks. As a result, the probability to spread the effect of a fault to the padding and detect it is much higher in the PCBC mode of operation.

In the next sections, we report the experimental validation of this analysis.

IV. EXPERIMENTAL VALIDATION OF ENCRYPTION FAULT DETECTION CAPABILITY

In this section, we describe the experimental setup that we adopted to validate the encryption fault detection capabilities discussed in Section III. Firstly, we describe the adopted fault models, as well as the classification that we use to categorize faults depending on their effects on the application under study. Then, we present the two ML applications used as case studies, the adopted fault injection setup and the flow of our experiments.

A. FAULT MODELS, FAULT CLASSIFICATION, AND FAULT EFFECTS

For the purpose of our analysis, in order to model the transient faults affecting the NVM that stores the IP of our system, we consider the *Single Event Upset (SEU)* (error multiplicity equal to 1) and the *Multiple Bit Upset (MBU)* (error multiplicity > 1). We perform fault injection campaigns only on the ML application weights and not on other ML data or application code. Concerning the application code, in a previous work [33] we have shown that encryption enables high fault detection rates. For the purpose of our analysis we classify faults as follows:

- *Silent*: the fault does not affect the classification results of the ML application and is not detected. The results match the expected ones, i.e. the fault-free (golden) classification results. The top-1 classification, namely the result predicted with the highest probability, is not modified.
- *Silent Data Corruption (SDC)*: the fault affects the classification results of the ML application and is not detected. The results do not match the golden classification results. The top-1 classification is modified.
- *Detected*: we consider 2 fault detection mechanisms:
  1) *Exception*: the fault effect generates an 'illegal' condition and either the software or the hardware triggers an exception revealing the fault occurrence.
  2) *Decryption Detection*: the fault is detected by the decryption mechanism. In particular, the fault affects one (or more) of the padding bytes appended to the plain-text (weights) for the encryption; the decryption mechanism detects the padding incorrectness and triggers an error, allowing the detection of the fault occurrence.

It has been shown that ML-based systems are rather resilient to errors [34], [35], [36]. Obviously, we want to avoid *SDC* cases, that may be catastrophic for the system and its environment. For example, in a self-driving vehicle, an object detection ML application impacted by a fault could lead to an incorrect detection of, for instance, pedestrians. This could put human lives in harmful situations [37].

In most ML applications, the weights are represented by floating point numbers. The IEEE-754 standard [38] specifies a special value, 'Not a Number' (NaN), that is the result of invalid operations. The presence of a NaN value reveals an incorrect behavior and, in our scenario, triggers an exception. According to the IEEE-754 standard, a sequence of bits interpreted as NaN satisfies the following conditions:

1) the exponent bits are all set to 1,
2) at least one bit of the mantissa is set to 1.

NaN values may be detected at hardware level by the CPU or at software level by the application code. In both cases, an exception is typically triggered. In our context, a fault affecting an encrypted weight is detected if its effect generates either a NaN value – thus a software exception – or a corrupted padding, caught by the decryption mechanism. Otherwise, it will be either a silent fault or an SDC. This depends on the fault criticality, which is connected to the fault location. In Figure 2 we report the binary representation of a 64-bit floating-point number. If the effect of an undetected fault

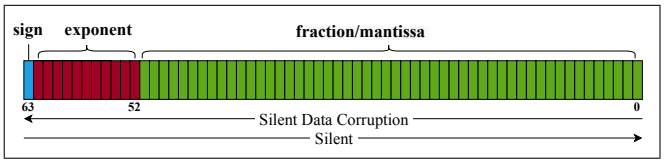


FIGURE 2: IEEE-754: Binary64 Floating Point number representation.

happens to corrupt one (or more) of the Least Significant Bits (LSBs) of the floating point number, then it will most probably be silent since the change of the weight's value will not be significant. Conversely, as the fault location moves towards the Most Significant Bits (MSBs) then the effects will be more severe and can lead to SDC [39], [40]. More in detail, as observed in [39], faults impacting the sign and the mantissa bits have a weaker impact on the network behavior than faults impacting the exponent bits.

B. CASE STUDY A: SIMPLE ANN

The first case study used for our experiments is an ANN. It is a classifier, which was developed using an ANSI C library [41]. Given as input a point in the (x, y) Cartesian plane, the ANN assigns it to one of the three following classes:

- C1: The point belongs to either one of the circles: $(x \pm 1)^2 + (y \pm 1)^2 \geq 0.16$
- C2: The point belongs to either one of the disks: $0.16 < (x \pm 1)^2 + (y \pm 1)^2 < 0.64$
- C3: The point belongs to neither circle nor disk: $(x \pm 1)^2 + (y \pm 1)^2 \geq 0.64$

The aforementioned loci are depicted in Figure 3. The training

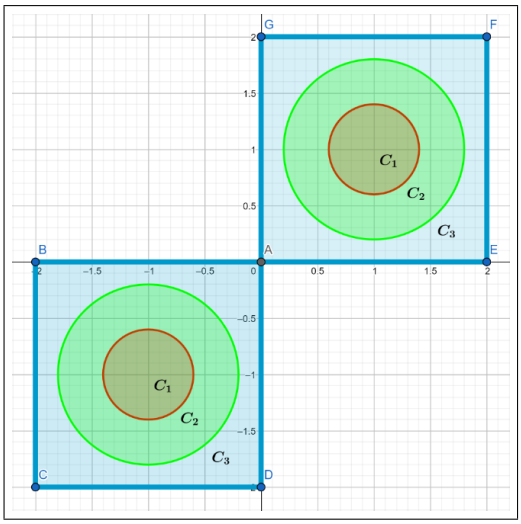


FIGURE 3: Graphical visualisation of the loci determined by the classification boundaries of the target ANN.

and the testing set of the network contain $3,000$ points each ($6,000$ in total). In each set $1,500$ randomly generated points are located inside the $[0, 2] \times [0, 2]$ rectangle and $1,500$ points are located inside the $[0, -2] \times [0, -2]$ rectangle.

The network is composed of 1 input layer, 3 hidden layers and 1 output layer. The input layer has 2 neurons, one for each of the points coordinates (x, y). The hidden layers have 10 neurons each and the output layer has 3 neurons, one for each of the classes (C1, C2, C3). In total, the network contains 283 weights (including each neuron's BIAS input weight), each corresponding to a 64-bit floating point number. In order to train the network we used the supervised learning technique. Every point in our training and test dataset was encoded using one-hot encoding. The adopted training algorithm was *gradient descent*.

The generalization error of the network was found to be 1.33%. This is the probability for the classifier to misclassify a given point of the test-set (e.g., to classify a point of the class C1 as a point of the class C2 or C3). The activation function selected for this network is the *sigmoid function*.

C. CASE STUDY B: CNN

The CNN that we used for our experiments is the LeNet-5 network [44]. It was first introduced in [43], where it was used to detect handwritten zip codes digits [45].

We resort to a LeNet-5 variant [42] trained on the MNIST dataset of handwritten digits [46] using the darknet framework [47]. The CNN takes as input 28x28 pixel images and its architecture, depicted in Figure 4, consists of the following layers:

C1: A convolutional layer that produces as output 32 feature maps of size 28x28. C1 has 2,400 trainable weights.

S2: A sub-sampling layer that reduces the dimension of the feature maps from 28x28 to 14x14. To generate a single value of a given output feature map, S2 takes the maximum value among a subset of four (2x2) input values.

C3: A convolutional layer that produces 64 feature maps of size 14x14. C3 has 51,200 trainable weights.

S4: A sub-sampling layer producing 64 feature maps of size 7x7, similarly to S2. Also S4 takes the maximum value among a subset of four (2x2) input values to generate an output value.

FC5: A fully connected layer with 1024 neurons. FC5 has 3,211,264 trainable weights.

FC6: A fully connected layer with 10 neurons. FC6 has 10,240 trainable weights.

OUT At the output of the network, a *Softmax* operation is performed. This maps the output values to the range [0,1], to treat them as probabilities. Finally, the sum of squared error (SSE) is calculated to compute the distance between the values from FC6 and some parameter vectors that correspond to the ten classes of digits. The parameter

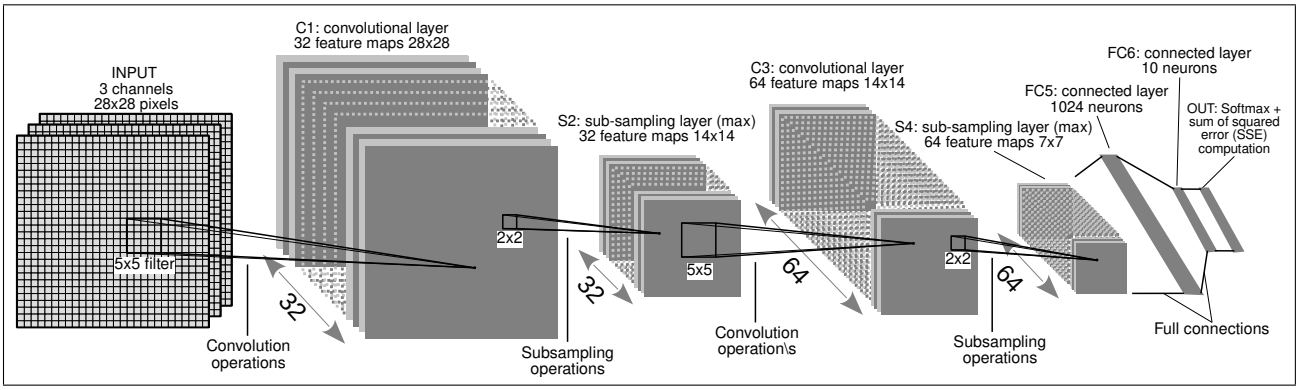


FIGURE 4: LeNet-5 variant architecture [42] (inspired from [43])

vectors were determined manually and kept fixed.

Neurons in layers C1, C3, FC5, and FC6 compute a dot product between their input vector and their weight vector and add a bias. For C1, C3, and FC5, the result is then passed through a *Rectified Linear Unit (ReLU)* activation function. For FC6 a linear activation function is used. Table 1 reports the percentage of images classified correctly per-digit after training the network along with the number of images that were used for the training and testing purposes of the network. In total, 70,000 images were used.

MT: Nick, please, add the number of images used in the test set. The total number of weights of the whole network, including neurons of both the convolutional and fully connected layers, is $3,275,104$. For more details on the LeNet-5 structure and functionality, please refer to [43].

TABLE 1: LeNet-5 classification accuracy, training and testing data for the MNIST dataset

Digit	Accuracy	Number of Images	
		Training	Testing
0	95,87%	5,923	980
1	97,41%	6,742	1,135
2	87,39%	5,958	1,032
3	81.76%	6,131	1,010
4	94,42%	5,842	982
5	78,06%	5,421	892
6	91,45%	5,918	958
7	90,45%	6,265	1,028
8	89,07%	5,851	974
9	88,33%	5,949	1,009
		60,000	10,000

D. FAULT INJECTIONS

As already mentioned, in this study we focus on transient faults affecting the NVM that stores the ML application's weights. To correctly model this scenario, we performed fault injection campaigns on the encrypted version of the ML applications' weights, before decrypting and using them to execute the ML application. Table 2 presents the size (in terms of total number of bits used to represent the weights) of the two ML applications, along with the total amount of experiments performed.

TABLE 2: Network Sizes and Total Experiments

Network	Total bits (net's weights)	Experiments	
		SEU	MBU
ANN	18,112	6	36
CNN	209,606,656		

For the experiments executed under the SEU fault model, we performed one fault injection campaign for each of the six considered cryptographic configurations. For the experiments executed under the MBU fault model, we performed six fault injection campaigns for every cryptographic configuration. Specifically, we injected faults of six different multiplicities, namely $10, 20, 50, 100, 200$ and 500. Thus, the total amount of experiments (i.e., fault injection campaigns) related to MBU model was $6 \times 6 = 36$.

Fault Injections per ML application

In order to obtain statistically meaningful results with an error margin of $\approx$1.5% and a confidence level of 95% we had to perform $3,454$ fault injections for every experiment on the ANN and $4,145$ fault injections for every experiment on the CNN application. The number of injected faults per experiment was calculated according to [48] as:

$$fault\_injections = \frac{N}{1 + e^2 \times \frac{N-1}{t^2 \times 0.25}}$$

where:

- N is the population, size i.e., column 2 of table 2.
- e is the desired error margin.
- t depends on the desired confidence level (t=1.96 corresponds to 95% confidence level)

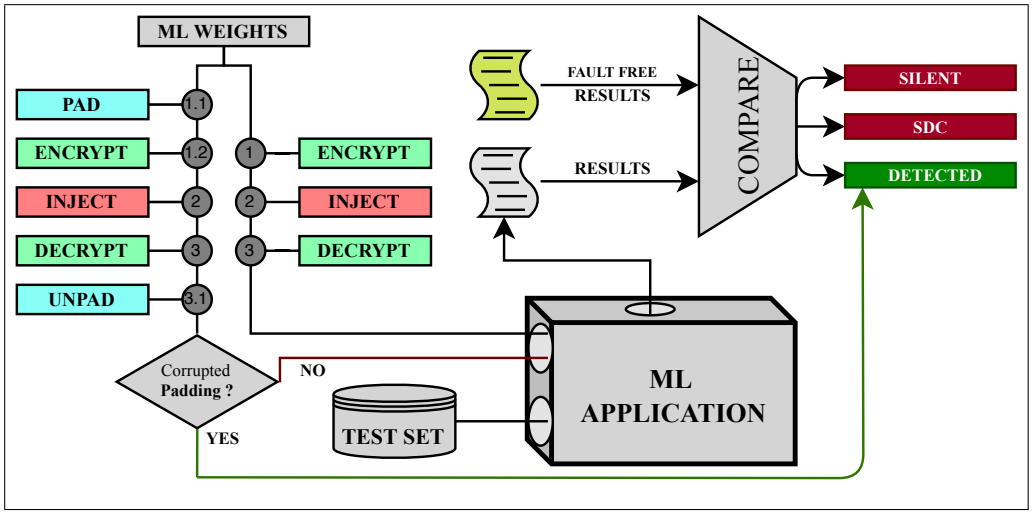


FIGURE 5: Experimental Setup

Furthermore, a uniform distribution was used for each fault injection campaign. Thence, each memory bit had the same probability of being selected.

E. EXPERIMENT FLOW

Figure 5 depicts the flow of our experiments. To study the effect of the padding check on fault detection capabilities, we organized the flow as follows. Firstly, the weights are either padded or not and then encrypted; then, a fault is injected in one of the weights, and finally they are decrypted and then either un-padded or not. When the padding is used, the effect of a fault on the encrypted memory content may propagate to the padding, thanks to the decryption. In this case, the padding check mechanism detects that the padding bytes have been altered, thus leading to the fault detection. On the other hand, if a padding byte has not been altered (or if the target system does not perform the padding integrity check), then it is up to the application to possibly detect the fault. As already mentioned, in our scenario this happens only if a NaN is generated and an exception is triggered. Finally, the classification results are compared with the golden classification results. Classification is performed as follows:

- If the results match i.e., exactly the same classification was performed with respect to the fault-free scenario, then the fault is classified as silent.
- If the results do not match i.e., items have been miss-classified, then the fault is classified as SDC.
- If the decryption mechanism detects a discrepancy in the padding segment or the application detects a NaN value while loading the weights, an exception is triggered and the fault is classified as detected.

In order to support the fault injection experiments we developed a tool using Python. This tool is responsible of (i) encrypting the weights of the respective ML application using a given cipher configuration, (ii) injecting a fault of a given multiplicity in the form of bit-flips and finally (iii) decrypting the memory data segment.

First of all, the tool executes the fault-free (golden) ML application with the given test set and obtains the fault-free NN results. Then, in order to have a point of reference and comparison, we perform fault injections on the networks' weights without using encryption. The criticality of the fault strongly depends on the fault location, as explained in Section IV-A. In this scenario, the only case where a fault is detected is when it causes a NaN value, which in turn triggers a software exception.

V. RESULTS

In this section, we present the experimental results that we obtained for our case studies. SEU results are summarized in Table 3, while MBU results are presented in the plots of Figure 6 and Figure 7. In both cases, two scenarios are considered. In the first scenario, checks on the padding segment of the ciphertext are not performed (NO PAD), while in the second scenario, checks are performed during the decryption process (PAD).

A. SEU EXPERIMENTS

ANN

Regarding the SEU experiments on the ANN, in the upper part of Table 3 we show that the differences between the results of the experiments performed with no encryption (our reference baseline) and those performed with non-spreading encryption ciphers are not significant, regardless of the padding utilization. Thus, non-spreading encryption ciphers do not provide any enhanced fault-detection capabilities. The majority of the injected faults are classified as silent.

As for the spreading encryption ciphers, we observe that almost always they produce more SDCs than the reference scenario, regardless of the padding utilization. The reason behind this behavior is the propagation of the fault during decryption. As explained in Section II-A, these modes of operation tend to amplify the fault effect by propagating it to neighbouring blocks of information. This attribute of the ciphers increases the probability of corrupting significant information bits that will eventually lead to a SDC case. However, the PCBC cipher configuration with padding utilization (PAD scenario) stands

TABLE 3: SEU Results

Fault Classification		**ANN**									
		NO PAD					PAD				
		non-spreading		*spreading*			*non-spreading*		*spreading*		
	NO ENC	CTR	OFB	CBC	CFB	PCBC	CTR	OFB	CBC	CFB	PCBC
Silent	75,5%	78,8%	77,4%	1,6%	2,6%	6,4%	76,6%	76,6%	0,6%	1,8%	0%
SDC	24%	21,8%	22%	98%	97,4%	92,8%	22,8%	22%	98,2%	96,4	0,6%
Detected	0,3%	0%	0,6%	0,4%	0%	0,8%	0,6%	1,4%	1,2%	1,8%	**99,4%**
Fault Classification		**CNN**									
		NO PAD					PAD				
		non-spreading		*spreading*			*non-spreading*		*spreading*		
	NO ENC	CTR	OFB	CBC	CFB	PCBC	CTR	OFB	CBC	CFB	PCBC
Silent	97,3%	96,8%	96,9%	20,3%	20,4%	0,0%	96,8%	96,9%	20,3%	20,4%	0,0%
SDC	2,7%	3,2%	3,1%	79,0%	78,6%	24,5%	3,2%	3,1%	79,0%	78 ,6%	0,1%
Detected	0,0%	0,0%	0,0%	0,7%	1,0%	75,5%	0,0%	0,0%	0,7%	1,0%	**99,9%**

NO PAD: Experiments that do not consider padding checking during decryption
PAD: Experiments that consider padding checking during decryption

out for achieving a fault detection rate of 99,4%. This result is due to the nature of the PCBC decryption process: when a fault is injected in the ciphertext, the PCBC decryption mechanism propagates the fault effects to all of the following blocks, resulting in the corruption of the padding segment. Hence, the corruption is detected by the padding check and an exception is raised.

CNN

The SEU results of the CNN case study are reported in the lower half of Table 3. Encryption with non-spreading ciphers does not provide any notable fault detection capabilities, similarly to the ANN scenario. Indeed, the results do not substantially deviate from the *no encryption* scenario and the vast majority of the faults fall into the silent category. Similarly to the ANN results, CBC and CFB block ciphers produce a high number of SDCs, regardless of the padding utilization. On the other hand, the PCBC configuration shows improved detection capabilities. In fact, when the padding check is not used, the PCBC is able to detect 75,5% of the faults. Moreover, when the padding check is performed, the PCBC achieves a detection rate of 99,9%.

One notable difference between the two case studies can be observed for the PCBC case in the NO PAD scenario. Without padding checks, PCBC achieves a higher fault detection rate when applied to the CNN, compared to the ANN. Note that the only way for a fault to be detected in this case is for the fault to generate a NaN value that will trigger an exception. We think that the reason behind this peculiarity may be the difference in size and number of operations between the two networks in combination with the PCBC's fault spreading property to all the following blocks. Indeed, the CNN's weights, as shown in column 2 of table 2, are 10^4 times as many as the weights of the ANN network. In order to be encrypted with a spreading cipher configuration, the weights are split into 128-bit blocks. In the ANN there are 142 blocks whilst in the CNN there are 6,550,208 blocks. Thus, during the decryption process, the effect of a fault impacting a random encrypted block in the CNN will be propagated to much more subsequent blocks than in the ANN, thus impacting more weights. Moreover, much more operations are carried out in the CNN than in the ANN. This surely contributes to error accumulation and propagation and increases the probability of getting a NaN. To give an example, we think that when a fault impacts a lot of weights (thanks to PCBC spreading property), it is likely that one or more of them assume a large value. The large values would grow even bigger thanks to the convolution operations, which involve basically multiplications and additions, and eventually could turn into the infinity value. Ultimately, operations with infinity values (e.g. multiplication with zero or the $\infty - \infty$ operation) could likely generate a NaN.

B. MBU EXPERIMENTS

ANN

Figure 6 reports the results of the MBU experiments for the ANN application. Regarding the NO PAD scenario (Figure 6-a), we observe that non-spreading ciphers behave similarly to the no encryption scenario. As the fault multiplicity rises, the fault detection rates rise as well. This means that, as the number of injected faults rises, the probability to induce a NaN increases. On the other hand, spreading cipher configurations tend not to provide any significant fault detection rate. Specifically, we can see that their fault detection rate drops for fault multiplicity higher than 200.

Concerning the PAD scenario where the padding integrity checks are performed (Figure 6-b), we observe PCBC dominating over the rest of the ciphers. Indeed, the PCBC achieved high fault detection capabilities, very close to 100%, regardless of the injected fault multiplicity. In general, the performance of all the ciphers in terms of their fault-detection capabilities was also enhanced since in this scenario a fault may corrupt bytes of the padding segment, generating an

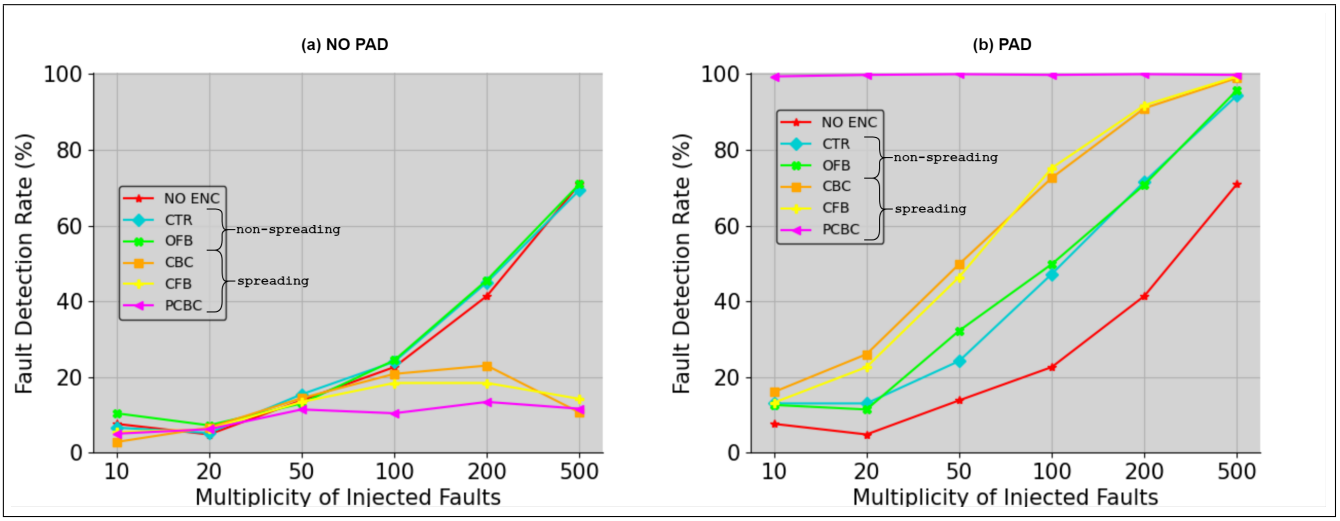


FIGURE 6: ANN MBU results for the (a) NO PAD and (b) PAD scenarios

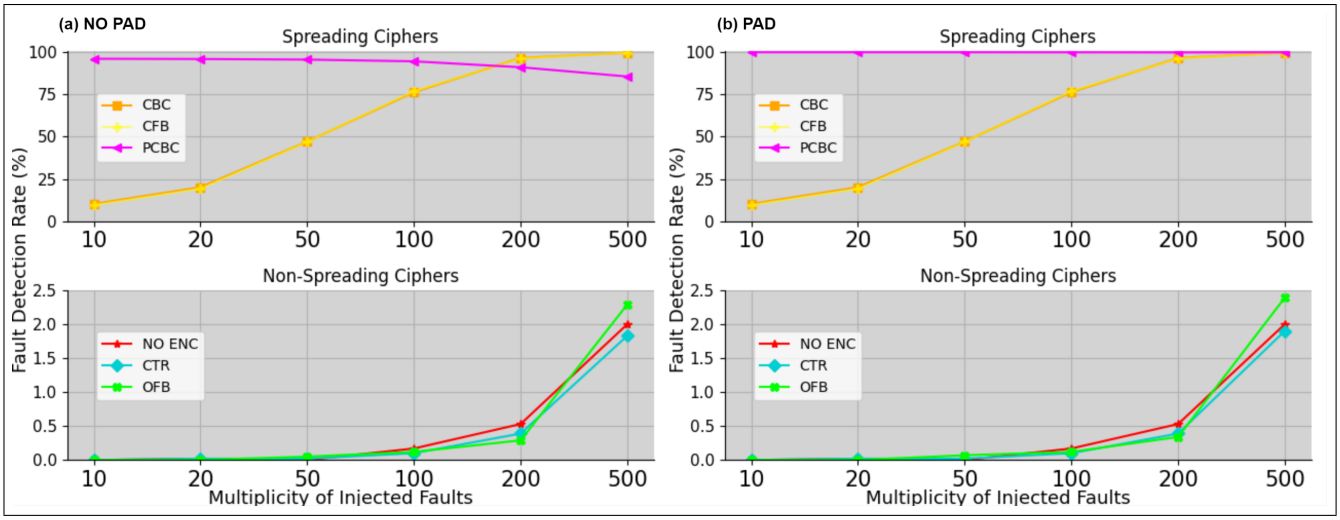


FIGURE 7: CNN MBU results for the (a) NO PAD and (b) PAD scenarios

immediate detection.

CNN

The results of the CNN case study are depicted in Figure 7. Similarly to what happens in the SEU experiments, we can see that the plots deviate from the ANN case. Regarding the NO PAD scenario (Figure 7-a), non-spreading ciphers do not provide significant fault detection. In fact, they achieve a detection rate close to the no encryption scenario. On the other hand, the fault detection rates obtained for spreading ciphers are higher for the CNN compared to the ANN. In particular, the PCBC configuration showed also in this case high detection capabilities, very close to 100%. We think that this phenomenon is related to what previously stated in Section V-A for the SEU experiment for the NO PAD scenario: the number of weights and operations in the CNN is much larger than in the ANN. Therefore, we think that, when multiple faults impact the CNN weights and the effect is spread to other weights thanks to spreading AES configurations, it is highly likely to generate high values that could eventually turn into infinity. Operations with infinity values could likely generate a NaN.

In the PAD scenario (Figure 7-b), where padding checks are performed, we observe again PCBC dominating over the rest of the ciphers by achieving very high fault detection rates, close to 100%.

Silent Faults and SDCs

As already discussed, the faults that remain undetected can be classified either as Silent or SDC. In both the analyzed ML applications, the percentage of undetected faults that are classified as SDCs is directly proportional to the injected fault multiplicity. Consequently, the percentage of undetected faults that are classified as silent is inversely proportional to the fault multiplicity. Indeed, as the multiplicity of faults increases, the likeliness of an undetected fault impacting significant memory bits increases as well; thus, the probability of a fault being silent and not causing data corruptions decreases. We observed the same trend for both spreading and non-spreading cipher configurations.

While the trend is the same, for low fault multiplicities the non-spreading configurations tend to produce higher percentages of silent faults (thus lower percentages of SDCs) than the spreading configurations. This is due to the intrinsic property of these latter configurations to spread the fault effects to multiple bits in the decryption process.

VI. CONCLUSIONS

The modern society is permeated with digital computing systems, which are increasingly vital to our everyday life. The design process of these systems has become incredibly complex, as many requirements have to be taken into account. In particular, reliability constraints have profoundly impacted the way designers implement these systems. Furthermore, in the last years, the growing interest in avoiding malicious attacks on intellectual properties within these systems led designers to integrate security-oriented techniques, such as memory encryption.

Autonomous systems employing Machine Learning (ML) technology are a prominent example where both reliability and security constraints are crucial. In particular, the correctness of the ML model weights determines the proper behavior of the system; at the same time, the weights are also considered a precious Intellectual Property (IP) item, since they are the result of an expensive and not trivial training process. Thus, companies need to protect them at once from faults and from malicious attacks. Unfortunately, these two aspects are studied and handled separately, with little interaction between the respective experts.

In this work, we analyzed and highlighted the fault-detection capabilities offered by memory encryption mechanisms. This enables designers to single out the most suitable

memory encryption mechanism for a system, while taking into account not only its safety, but also its reliability. We experimentally evaluated the positive impact that data encryption has in terms of reliability enhancements with respect to the effects of transient faults. To do so, we performed extensive fault injection campaigns on the encrypted weights of an Artifical Neural Network (ANN) and of a Convolutional Neural Network (CNN) and evaluated the fault-detection capabilities provided by the decryption mechanism. The underlying idea is that the effect of a fault affecting an encrypted data will spread to adjacent data in the decryption process, thus increasing the probability of detecting the fault occurrence. The obtained results showed that selecting a particular Advanced Encryption Standard (AES) configuration, i.e., the Propagating Cipher Block Chaining (PCBC), in combination with padding check mechanisms allowed us to achieve significantly high fault detection rates ($> 99\%$), with respect to the Single Event Upset (SEU) and the Multiple Bit Upset (MBU) faults models.

This work encourages and paves the way to the development of new integrated design techniques that take into account at once multiple crucial requirements of the new-generation advanced computing systems.

REFERENCES

[1] K. F. Li and N. Attarmoghaddam, "Challenges and methodologies of hardware security," in *International Conference on Advanced Information Networking and Applications*. IEEE, 2018.

[2] S. Ghosh, M. N. I. Khan, A. De, and J. Jang, "Security and privacy threats to on-chip non-volatile memories and countermeasures," in *2016 IEEE/ACM International Conference on Computer-Aided Design*, 2016, pp. 1–6.

[3] Mohammad Nasim Imtiaz Khan and Swaroop Ghosh, "Assuring Security and Reliability of Emerging Non-Volatile Memories," in *2020 International Test Conference*. IEEE, 2020.

[4] D. Rossi and C. Metra, "Error correcting strategy for high speed and high density reliable flash memories," *Journal of Electronic Testing*, vol. 19, pp. 511–521, 2003.

[5] W. Liu and J. Rho and W. Sung, "Low-Power High-Throughput BCH Error Correction VLSI Design for Multi-Level Cell NAND Flash Memories," in *2006 IEEE Workshop on Signal Processing Systems Design and Implementation*, 2006, pp. 303–308.

[6] J. Xiao-bo and T. Xue-qing and H. Wei-pei, "Novel ecc structure and evaluation method for nand flash memory," in *2015 28th IEEE International System-on-Chip Conference (SOCC)*, 2015, pp. 100–104.

[7] M. Ye, K. Zubair, A. Mohaisen, and A. Awad, "Towards low-cost mechanisms to enable restoration of encrypted non-volatile memories," *IEEE Transactions on Dependable and Secure Computing*, pp. 1–1, 2019.

[8] S. Katzenbeisser and I. Polian and F. Regazzoni and M. Stöttinger, "Security in Autonomous Systems," in *2019 IEEE European Test Symposium (ETS)*, 2019, pp. 1–8.

[9] Tom Michel, *Machine Learning*. McGraw Hill, 1997.

[10] Yann LeCun and Yoshua Bengio and Geoffrey Hinton, "Deep learning," *Nature*, vol. 521, pp. 436–444, 2015.

[11] Michael K. K. Leung and Hui Yuan Xiong and Leo J. Lee. and Brendan J. Frey, "Deep learning of the tissue-regulated splicing code," *Bioinformatics*, vol. 30, no. 12, pp. 121–129, 2014.

[12] Pierre Sermanet, Koray Kavukcuoglu, Soumith Chintala, and Yann LeCun, "Pedestrian Detection with Unsupervised Multi-Stage Feature Learning," *CoRR*, vol. abs/1212.0142, 2012.

[13] C. Farabet, C. Couprie, L. Najman, and Y. LeCun, "Learning Hierarchical Features for Scene Labeling," *IEEE Transactions on Pattern Analysis and Machine Intelligence*, vol. 35, no. 8, pp. 1915–1929, 2013.

[14] C. Garcia and M. Delakis, "Convolutional face finder: a neural architecture for fast and robust face detection," *IEEE Transactions on Pattern Analysis and Machine Intelligence*, vol. 26, no. 11, pp. 1408–1423, 2004.

[15] Daniel R. Wade and Andrew William Wilson, "Applying machine learning-based diagnostic functions to rotorcraft safety," in *17th Australian Aerospace Congress*, 2017.

[16] Tramèr Florian and Zhang Fan and Juels Ari and Reiter Michael K. and Ristenpart, Thomas, "Stealing Machine Learning Models via Prediction APIs," in *25th USENIX Conference on Security Symposium*, ser. SEC'16. USA: USENIX Association, 2016, p. 601–618.

[17] R. Cantoro, N. I. Deligiannis, M. S. Reorda, M. Traiola, and E. Valea, "Evaluating data encryption effects on the resilience of an artificial neural network," in *2020 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, 2020, pp. 1–4.

[18] Andreani,C. and Senesi,R. and Paccagnella,A. and Bagatin,M. and Gerardin,S. and Cazzaniga,C. and Frost,C. D. and Picozza,P. and Gorini,G. and Mancini,R. and Sarno,M. , "Fast neutron irradiation tests of flash memories used in space environment at the ISIS spallation neutron source," *AIP Advances*, vol. 8, no. 2, p. 025013, 2018.

[19] M. Bagatin and S. Gerardin and A. Paccagnella and A. Visconti and L. Chiavarone and M. Calabrese and C. D. Frost, "Sensitivity of NOR Flash memories to wide-energy spectrum neutrons during accelerated tests," in *2014 IEEE International Reliability Physics Symposium*, 2014, pp. 5F.3.1–5F.3.6.

[20] Yuqian Pan and Haichun Zhang and Mingyang Gong and Zhenglin Liu, "Unexpected Error Explosion in NAND Flash Memory: Observations and Prediction Scheme," in *2020 IEEE 29th Asian Test Symposium*, 2020.

[21] D. Ielmini and A.S. Spinelli and A.L. Lacaita, "Recent developments on Flash memory reliability," *Microelectronic Engineering*, vol. 80, pp. 321–328, 2005, 14th biennial Conference on Insulating Films on Semiconductors.

[22] D. H. Yoon and N. Muralimanohar and J. Chang and P. Ranganathan and N. P. Jouppi and M. Erez, "FREE-p: Protecting non-volatile memory against both hard and soft errors," in *2011 IEEE 17th International Symposium on High Performance Computer Architecture*, 2011, pp. 466–477.

[23] Timothy J. Dell, "A White Paper on the Benefits of Chipkill-Correct ECC for PC Server Main Memory," IBM Microelectronics Division, Tech. Rep., 1997.

[24] Intel, "Independent Channel vs. Lockstep Mode - Drive your Memory Faster or Safer," https://software.intel.com/content/www/us/en/develop/blogs/independent-channel-vs-lockstep-mode-drive-you-memory-faster-or-safer.html, [Online; accessed 05-November-2020].

[25] Amro Awad and Laurent Njilla and Mao Ye, "Triad-NVM: Persistent-Security for Integrity-Protected and Encrypted Non-Volatile Memories (NVMs)," 2018.

[26] S. Liu and A. Kolli and J. Ren and S. Khan, "Crash Consistency in Encrypted Non-volatile Main Memory Systems," in *2018 IEEE International Symposium on High Performance Computer Architecture (HPCA)*, 2018, pp. 310–323.

[27] H. Shacham, "Return-oriented programming: Exploits without code injection," in *Black Hat USA*, 2008. [Online]. Available: https://www.blackhat.com/html/bh-usa-08/bh-usa-08-archive.html

[28] R. Roemer, E. Buchanan, H. Shacham, and S. Savage, "Return-oriented programming: Systems, languages, and applications," *ACM Trans. Inf. Syst. Secur.*, vol. 15, no. 1, Mar. 2012. [Online]. Available: https://doi.org/10.1145/2133375.2133377

[29] T. Bletsch, X. Jiang, V. W. Freeh, and Z. Liang, "Jump-oriented programming: A new class of code-reuse attack," in *Proceedings of the 6th ACM Symposium on Information, Computer and Communications Security*, ser. ASIACCS '11. New York, NY, USA: Association for Computing Machinery, 2011, p. 30–40. [Online]. Available: https://doi.org/10.1145/1966913.1966919

[30] O. Savry, M. El-Majihi, and T. Hiscock, "Confidaent: Control flow protection with instruction and data authenticated encryption," in *2020 23rd Euromicro Conference on Digital System Design (DSD)*, 2020, pp. 246–253.

[31] Mario Werner and Thomas Unterluggauer and David Schaffenrath and Stefan Mangard, "Sponge-Based Control-Flow Protection for IoT Devices," 2018.

[32] B. Kaliski, "RFC2315: PKCS #7: Cryptographic Message Syntax Version 1.5," USA, 1998.

[33] R. Cantoro and N. I. Deligiannis and M. S. Reorda and M. Traiola and E. Valea, "Evaluating the Code Encryption Effects on Memory Fault Resilience," in *2020 IEEE Latin-American Test Symposium (LATS)*, 2020, pp. 1–6.

[34] S. Mittal, "A survey of FPGA-based accelerators for convolutional neural networks," *Neural Computing and Applications*, 10 2018.

[35] C. Torres-Huitzil and B. Girau, "Fault and Error Tolerance in Neural Networks: A Review," *IEEE Access*, vol. 5, pp. 17 322–17 341, 2017.

[36] W. Sung, S. Shin, and K. Hwang, "Resiliency of Deep Neural Networks under Quantization," *CoRR*, vol. abs/1511.06488, 2015.

[37] Gunnar D Jenssen and Terje Moen and S. Johnsen, "Accidents with Automated Vehicles -Do self-driving cars need a better sense of self?" in *26th ITS World Congress*, 10 2019.

[38] *754-2019 - IEEE Standard for Floating-Point Arithmetic*, IEEE, July 2019, Revision of IEEE Std 754-2008.

[39] A. Bosio and P. Bernardi and A. Ruospo and E. Sanchez, "A Reliability Analysis of a Deep Neural Network," in *2019 IEEE Latin American Test Symposium (LATS)*, 2019, pp. 1–6.

[40] Li, Guanpeng and Hari, Siva Kumar Sastry and Sullivan, Michael and Tsai, Timothy and Pattabiraman, Karthik and Emer, Joel and Keckler, Stephen W., "Understanding Error Propagation in Deep Learning Neural Network (DNN) Accelerators and Applications," in *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis*. Association for Computing Machinery, 2017.

[41] Lewis Van Winkle, "C Neural Network Library: Genann," https://codeplea.com/genann, [Online; accessed 05-November-2020].

[42] Gokul NC, "DarkNet Classifier LeNet MNIST," https://github.com/ashitani/darknet_mnist, [Online; accessed 21-December-2020].

[43] Y. LeCun and L. Bottou and Y. Bengio and P. Haffner, "Gradient-based learning applied to document recognition," *Proceedings of the IEEE*, vol. 86, no. 11, pp. 2278–2324, 1998.

[44] Yann Lecun, "LeNet-5," http://yann.lecun.com/exdb/lenet/, [Online; accessed 06-November-2020].

[45] LeCun Y. and Boser B. and Denker J. S. and Henderson D. and Howard R. E. and Hubbard W. and Jackel L. D., "Backpropagation Applied to Handwritten Zip Code Recognition," *Neural Computation*, vol. 1, no. 4, pp. 541–551, 1989.

[46] Yann LeCun and Corinna Cortes and Christopher J.C. Burges, "The MNIST Database," http://yann.lecun.com/exdb/mnist/, [Online; accessed 06-November-2020].

[47] Joseph Redmon, "Darknet: Open Source Neural Networks in C," http://pjreddie.com/darknet/, [Online; accessed 06-November-2020].

[48] R. Leveugle and A. Calvez and P. Maistri and P. Vanhauwaert, "Statistical fault injection: Quantified error and confidence," in *2009 Design, Automation Test in Europe Conference Exhibition*, 2009, pp. 502–506.

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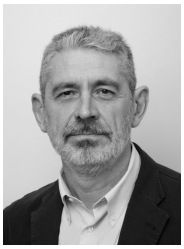

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