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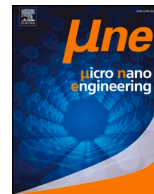
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Research paper

## Sub-20 nm multilayer nanopillar patterning for hybrid SET/CMOS integration

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## ABSTRACT

SETs (Single-Electron-Transistors) arouse growing interest for their very low energy consumption. For future industrialization, it is crucial to show a CMOS-compatible fabrication of SETs, and a key prerequisite is the patterning of sub-20 nm Si Nano-Pillars (NP) with an embedded thin SiO<sub>2</sub> layer. In this work, we report the patterning of such multi-layer isolated NP with e-beam lithography combined with a Reactive Ion Etching (RIE) process. The Critical Dimension (CD) uniformity and the robustness of the Process of Reference are evaluated. Characterization methods, either by CD-SEM for the CD, or by TEM cross-section for the NP profile, are compared and discussed.

## 1. Introduction

The Internet of Things (IoT) is a very rapidly growing market, with 20 billion of connected devices expected by 2020. A critical constraint for those devices is to offer low power consumption [1]. In this context, single-electron-transistors (SETs), consisting of a quantum dot lying between two tunneling junctions to neighbor drain and source Si regions, arise growing interest [2]. In particular, vertical nanopillar based SETs in gate-all-around configuration, where the quantum dot is a Si nanodot embedded in a SiO<sub>2</sub> layer, are promising candidates to offer both low power consumption and an enhanced gate control [3,4]. For future industrialization, it is crucial to show a CMOS-compatible fabrication of SETs working at room temperature. In that purpose, the Horizon 2020 project IONS4SET develops a technology to realize SETs by ion-irradiation-assisted self-assembly of single Si nanodot (ND) in a thin SiO<sub>2</sub> layer sandwiched between silicon of a nanopillar (NP) of ~70 nm height and 15 nm diameter. [5,6]. NPs of such dimensions have already been patterned, but either the processes and materials do not meet the CMOS industry standards, or the NPs are single-layer structures [7,8]. In this work, we report the patterning development of such multi-layer isolated NPs with a Critical Dimension (CD) below 20 nm. Morphological specifications of the NPs have been predicted by simulation [9] and define NPs as a stack, from top to bottom, of a

30 nm-thick Si drain layer, a 6 to 10 nm-thick SiO<sub>2</sub> gate oxide layer, and a 35 nm-thick Si source layer which is patterned in the top silicon of an SOI substrate. The NPs sidewall angle is not a critical parameter for SET electrical behavior and cylindrical NPs are assumed. However, a straight profile is targeted to enhance the SET contacting process capabilities. The selected integration combines e-beam lithography with dry Reactive Ion Etching. We first present the CMOS industrial-compliant, 200 mm equipments and materials used in this work as well as the characterization methodology implemented. We then detail process definition and optimization leading to a Process of Reference (PoR), which we evaluate in terms of CD uniformity and reproducibility.

## 2. Process equipments and materials

## 2.1. Electron-beam lithography (EBL)

We start defining the NPs by an EBL step that should meet two constraints: high resolution and CMOS production line compatibility. The Variable Shaped Beam SB3054 Model from VISTEC, with an acceleration voltage of 50 kV and a bridge 200–300 mm wafer handling platform, meets both requirements. The exposure time of extensive functional and process monitoring features for > 100 chips on a 200 mm wafer is 1 h45 per wafer. Even though our 100 kV Gaussian-

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beam tool would have slightly increased the resolution, this benefit would be limited with the chemically amplified resist that we used. Moreover, it is designed for advanced research patterning with a lower throughput and stability, and thus does not comply with the objective of demonstrating SET/FETs with a CMOS-compatible process.

The electron-sensitive thin layer is a chemically amplified, 70 nm-thick negative tone resist, to limit the EBL writing time. It was either used alone, on a SiN hard-mask, or on Spin-On-Carbon (SOC) and Silicon-Anti-Reflective Coating (SiARC) forming a trilayer stack that meets the industry standards. Resist, SiARC and SOC layers are all spin-coated on a MK8C track from TEL, while the SiN layer is deposited in a PECVD CENT5200E chamber from AMAT.

A specific layout was designed for process and device development purpose, including not only the isolated NPs that will form the core of SETs devices, but also pillar arrays of variable dimensions and densities to support process development.

## 2.2. Reactive ion etching (RIE)

The nano-pillar etching was performed in a single Inductively Coupled Plasma (ICP) chamber from the AMAT CenturaAP DPS-II 200 mm platform. ICP chambers allow both isotropic etch for trimming steps, and anisotropic etch for pattern transfer, all included in an “all in-situ” single recipe. Thanks to the large opening ratio of the layout, we are able to use the end-point detection to precisely control the etch time of every step. Each layer is etched with a dedicated chemistry that we list in Table 1, including the different hard-mask options.

## 3. Characterization

### 3.1. Structural characterization

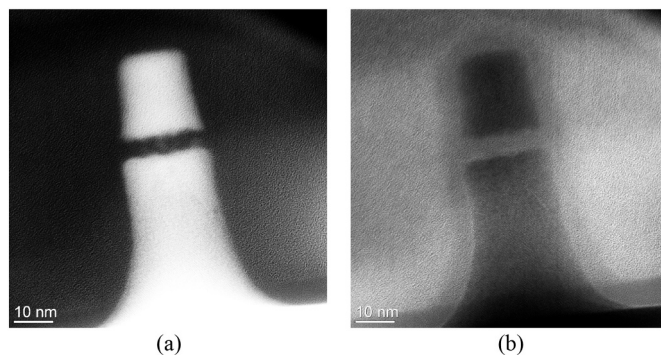
To characterize the NPs' structure, we employed two techniques. First, a simple, non-destructive observation with a high resolution tilted Scanning Electron Microscope (SEM) gives a good information on the pillar's profile. Depending on the magnification, one can observe a single NP, or a large number of them. The SEM Helios NanoLab 1200HP from FEI, installed at LETI, allows dense pillar array as well as isolated pillar imaging.

However, tilted SEM observation becomes limited to observe the multi-layer structure and to separate SiO<sub>2</sub> and Si precisely. Thus, the second technique we implemented is the Energy-Filtered Transmission Electron Microscopy (EFTEM) using Focused Ion Beam (FIB) prepared cross-sectional lamellae. EFTEM allows to depict both the Si and the Si oxide part of the NPs by energy filtered imaging using the Si plasmon loss (17 eV) and the Si oxide plasmon loss (26 eV), respectively. Thus, one can make visible the SiO<sub>2</sub> gate oxide layer and the thickness of the Si oxide layer that covers the whole pillar can be measured as well. The FIB NVision 40 from Zeiss Microscopy, and the EFTEM Titan 80–300 from FEI equipped with the “Gatan Tridium 863” energy filter, are both installed at HZDR. An example of an oxide covered, stacked NP using both filtering is displayed in Fig. 1.

**Table 1**

Etching type (isotropic or anisotropic) and chemistries used for NPs etching.

Layer/step	Type	Chemistry
Resist trimming	Isotropic	HBr-O <sub>2</sub>
SiN	Anisotropic	CH <sub>2</sub> F <sub>2</sub> -O <sub>2</sub>
SiARC	Anisotropic	CF <sub>4</sub>
SOC	Anisotropic	HBr-O <sub>2</sub>
Break-Through	Anisotropic	CF <sub>4</sub>
a-Si	Anisotropic	Cl <sub>2</sub> -HBr
SiO <sub>2</sub>	Anisotropic	CF <sub>4</sub>
Si	Anisotropic	Cl <sub>2</sub> -HBr



**Fig. 1.** EFTEM pictures of the same NP taken with (a) 17 eV plasmon loss filtering with enhanced sensitivity for Si, and (b) 26 eV plasmon loss filtering with enhanced sensitivity for SiO<sub>2</sub>. The grey layer in (b) is the oxide layer that covers the whole pillar: it was generated in a post-patterning process step and is not treated in this paper.

### 3.2. CD measurement

Beyond NPs profile, CD measurement of the pillar diameter is a key characterization for process control. It is well accepted within the metrology community that CD-SEM is not an accurate metrology method for quantification, as parameters setup such as acceleration voltage, threshold level [10], or charging effects [11], can modify the measurement value. Also, CD-SEM images are always taken from the top so that additional oxide layers, oxide bulges and pillar broadening in the lower part result in larger CD values compared to TEM measurements, always done very close to the Si/SiO<sub>2</sub> interface. However, its high reproducibility < 1 nm for similar patterns, is very valuable for process control as we can compare values at various process steps and for various process options.

Thus, we implemented extensive CD measurement after lithography and etching, using the HITACHI CG4000 CD-SEM. The same measurement parameters apply after lithography and etching steps.

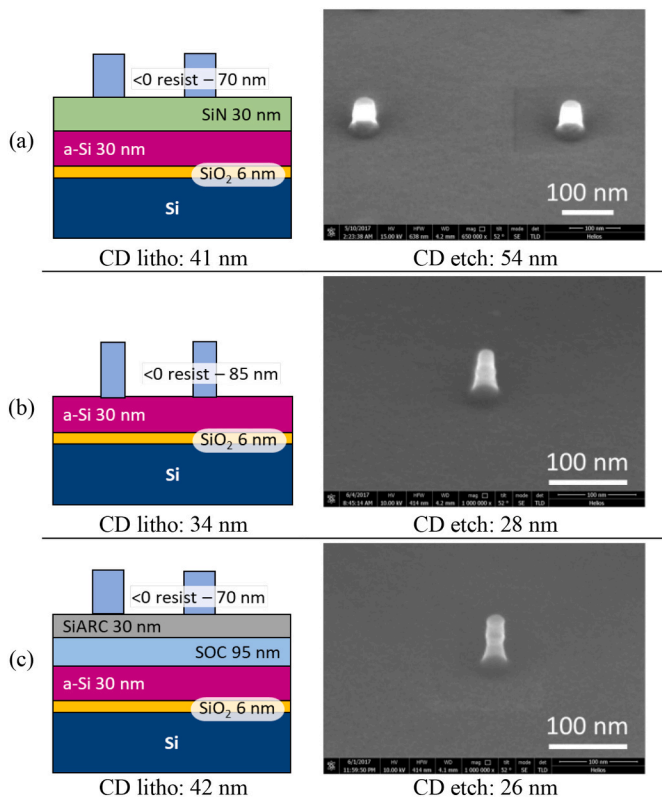
## 4. Process optimization

### 4.1. Patterning stack definition

The main challenge for the patterning of sub-20 nm NPs with standard industrial CMOS equipments was to reach an aggressive CD in a multilayer stack while keeping a straight profile. The hard-mask stack definition is a key contributor to this achievement. We have benchmarked three different approaches: (a) resist coated onto a 30 nm-thick SiN layer; (b) resist directly coated on the substrate (a-Si/SiO<sub>2</sub>/Si); and (c) resist coated onto a Spin-On-Carbon (SOC) and Silicon-Anti-Reflective Coating (SiARC) layers, with a thickness of 95 nm and 30 nm respectively. Fulfilling the objective of being compatible to CMOS-industry typical process, we fine-tuned already existing processes with respect to qualified resist types and thicknesses. A CD reduction of the resist pattern was implemented for SiN and trilayer hard-mask cases only: this so-called “trimming” step is isotropic and consumes the resist thickness. Without a hard-mask, the remaining resist is too thin to etch the entire NP stack.

The minimal achievable CD is determined by CD-SEM measurement after both lithography and etching, and the NPs profile is observed by tilted SEM after etching. In Fig. 2 (a) one can see that the SiN hard-mask is not satisfactory in terms of post-etch CD even though the profile is acceptable. The SiN etching induces a sidewall angle in this layer, leading to a post-etch CD of 54 nm despite a resist trim. This is larger than the post-litho CD, and well above the target. Moreover, the SiN hard-mask is stripped using wet HF process which could impact the thin SiO<sub>2</sub> layer.

Using only resist, as in Fig. 2 (b), we are able to reduce strongly the



**Fig. 2.** Integration scheme and NP profile imaged by tilted SEM, with a magnification of (a) x650k for SiN hard-mask, (b) x1000k for resist only, and (c) x1000k for trilayer SOC/SiARC/resist patterning stacks. Minimum achievable CDs are displayed under the drawing after lithography and under the SEM image after etching.

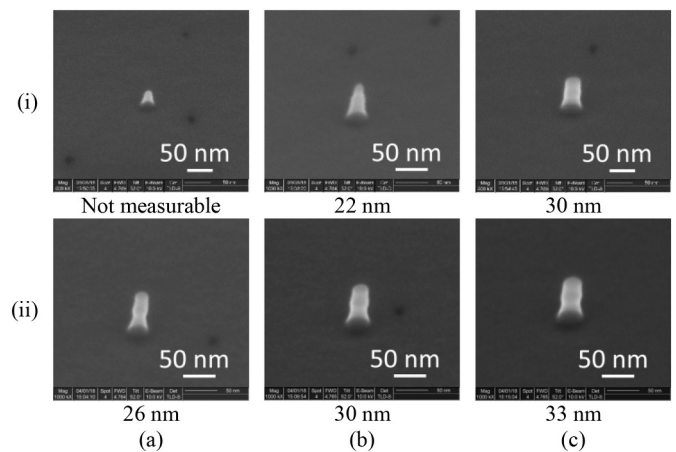
CD post-lithography to 34 nm. The post-etch CD of 28 nm is in the target with an acceptable profile, similar to the SiN approach.

The trilayer stack options appears much more complex, but all hard-mask layers (SOC, SiARC and resist) are spin-coatable in a single step and can be removed without HF wet chemistry. Despite a relatively high post-lithography CD of 42 nm, the etching selectivity offered by the SiARC and SOC allows a significant isotropic trimming of the resist and thus an important negative litho-etch CD bias of  $-16$  nm. In the end, the post-etch minimal CD is 26 nm, which is similar to the resist-only approach. However, the trilayer stack enables a more vertical profile and thus appears to be the best candidate.

#### 4.2. Resist thickness and coating delay

It is well known that the resolution limit of a lithographic process depends on the resist thickness: the thinner the resist, the better the resolution [12]. On the other hand, the resist thickness should be sufficient for the etching of the underlying layers. In other words, one will need to find a compromise between resolution and resist consumption during etching. We have benchmarked two different thicknesses available in-line in the coating track: 40 nm and 70 nm. To determine the resolution, or the minimal CD, we have exposed the smallest isolated feature with the EBL tool at several doses, and etched them with the PoR. The resolution is the smallest CD obtained with a resolved pattern. It is measured by CD-SEM after both lithography and etch steps, while the NPs profile is controlled by tilted SEM after etching only.

The lithography resolution limit is 43 nm for a film thickness (FTH) of 70 nm, and 35 nm for a FTH of 40 nm, thus fulfilling our expectation. However, it is shown in Fig. 3 that 40 nm appears to be too thin for etching consumption, since pillars with the same post-litho CD of 42 nm



**Fig. 3.** NPs profile imaged by tilted SEM and CD value after etching with a resist thickness of (i) 40 nm and (ii) 70 nm. In both cases, the etching was applied on NPs with the same initial post-litho CD of (a) 42 nm, (b) 46 nm, and (c) 50 nm.

are well patterned with the 70 nm-FTH resist, but damaged with the 40 nm-FTH resist. The PoR thickness is thus set up to 70 nm.

To improve furthermore the lithography process, we optimized the delay times between different lithography steps. For the delay between exposure and development, which is a well-known instability cause [13], our standard process already limits the delay to 10 min maximum. The delay between resist coating and exposure have also been reported to induce CD instability [14]. We have verified if a delay time between resist coating and exposure degrades the performances in our process conditions and for the targeted dimensions. We compared the Process of Reference (PoR) with a wafer that awaited 4 h in the cleanroom atmosphere before exposure, the resist being already spin-coated in standard conditions. This delay was setup as the typical waiting time for standard wafer processing. Both wafers were printed in the same exposure-dose matrix, and we measured the smallest features for all doses. The resolution limit with the 4 h delay increases to 44 nm, compared to 41 nm with the PoR. The SB3045 EBL tool allows processing wafers two by two, keeping each wafer under vacuum while the other one is exposed, to prevent any impact on the patterns. Both wafers are then developed within a few minutes. Thus, we processed the wafers two by two instead of launching the full batch of wafers, to avoid any delay before and after exposure.

#### 4.3. Trimming optimization

Once the lithography PoR is established, we optimized the etching process to push down the NPs diameter. The main adjustment parameter is the resist trimming before the pattern transfer into underlying materials. We have applied three trimming times  $T_1 < T_2 < T_3$ , and compared the post-etch CDs and profiles. The litho-etch CD bias increases accordingly, with respectively  $b_1 = -16$  nm,  $b_2 = -19$  nm, and  $b_3 = -24$  nm, leading to reduced NPs diameters as summarized in Fig. 4. The pillars profile is straight in all three cases, but with  $T_2$  and  $T_3$  trimming times we observed defective pillars, meaning we are at the limit of the process window with a reduced yield. Given the fact that SET devices require a single isolated NP, we have selected the process with the highest yield, with  $T_1$  as our reference trimming time.

### 5. PoR assessment

#### 5.1. Calibrated NPs diameter

The PoR previously defined, for both lithography and etch processes, was demonstrated to efficiently pattern NPs with the required

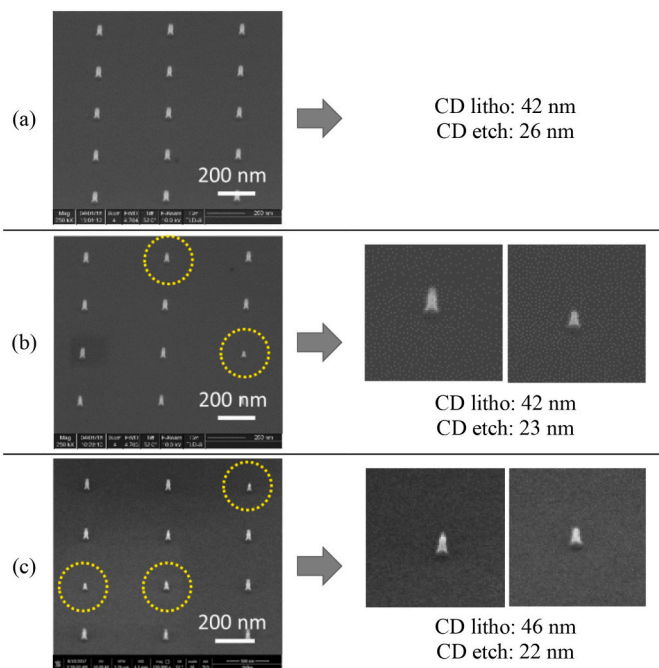


Fig. 4. NPs profile after etching process with a resist trimming step time (a)  $T_1$ , (b)  $T_2 > T_1$ , and (c)  $T_3 > T_2$ . Typical defective pillars are circled and enlarged in the right column. The mean CD over the wafer after lithography and etching is also indicated.

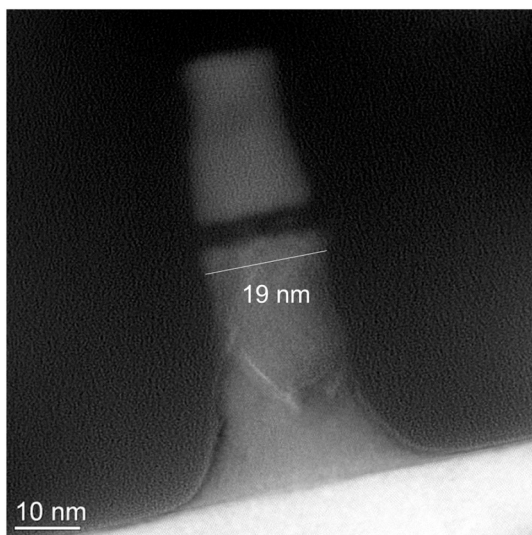


Fig. 5. Isolated NP obtained with the process of reference and imaged using EFTEM with Si plasmon loss filtering. The diameter close to the  $\text{SiO}_2$  layer is below 20 nm.

morphology. As mentioned in section 3.2, the CD-SEM measurements can not be considered as accurate. To fully validate the NPs diameter, we have used EFTEM imaging. We calibrated the TEM high magnifications using the Si lattice standard, and middle to lower magnifications using the so-called ‘MAG-I-CAL’ calibration standard [15], which is a Si-SiGe multilayer film stack calibrated by X-ray diffraction. With this procedure, the measurement error remains within  $\sim 5\%$  and CD measurements can then be considered as accurate. The measurement in Fig. 5 confirms that the PoR succeeds in patterning sub-20 nm multi-layer NPs.

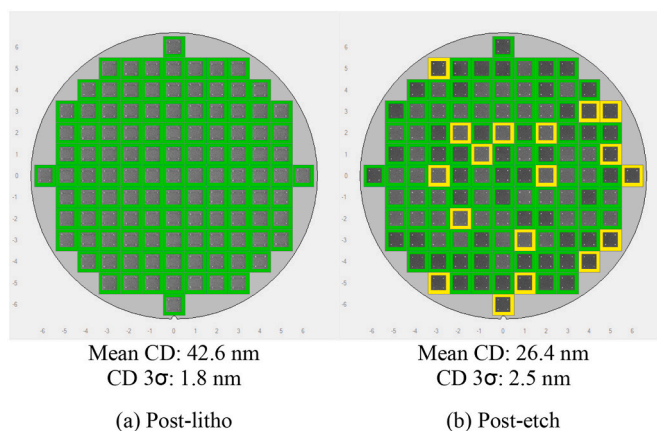


Fig. 6. CDU maps of two wafers: (a) after lithography step, and (b) after etching and stripping step. Green chips CD is within a  $\pm 5\%$  range around the mean wafer CD; yellow chips CD is within a  $\pm 10\%$  range around the mean wafer CD. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

### 5.2. Process uniformity and reproducibility

The PoR was then assessed in terms of intra-wafer CD Uniformity (CDU), and reproducibility within the target range of the embedded  $\text{SiO}_2$  thickness. As statistical measurements are mandatory for such evaluation, we used CD-SEM measurements which, again, do not provide the real NPs diameter but give a reliable assessment of the CD uniformity and reproducibility.

To evaluate the CDU, we measured the CD of 4 NPs in all 113 chips of two wafers: the first wafer after the lithography process, the second wafer after the etching process. The resulting uniformity is given by the  $3\sigma$  value of the measurement. After lithography, we got a 1.8 nm CDU for a mean CD of 42.6 nm, and after etching, we got a 2.5 nm CDU, for a mean CD of 26.4 nm. The CDU maps as shown in Fig. 6 reveals that most of the 113 chips, whether after lithography or etching, are within a  $\pm 5\%$  range around the wafer mean value.

In parallel, we tested the robustness and reproducibility of the PoR when modifying the embedded oxide thickness within the 6 nm to 10 nm targeted range. In this case, the mean CD was measured after etching on seven chips, and we controlled the NPs profile with tilted SEM imaging. One can see in Fig. 7 that the NPs' mean CD is very close to the PoR value (26.4 nm), and that the profile remains straight with the three oxide thicknesses, namely 6.5 nm, 8 nm and 10 nm.

### 6. Conclusion

We have defined and optimized a process to structure isolated multi-layer nanopillars with a diameter down to 19 nm for isolated NPs, which is close to the requirement for a room-temperature operating SETs device as defined for IONS4SET technology. Furthermore, this 200 mm CMOS-compatible process shows a wafer CD uniformity of 2.5 nm, and the pillars profile are almost straight for embedded gate

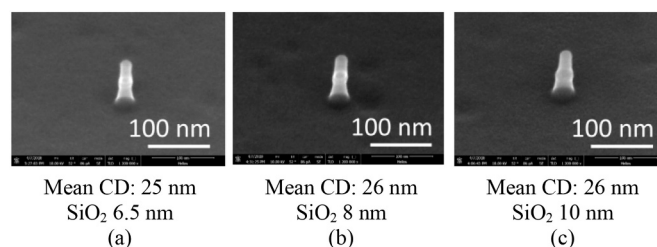


Fig. 7. Mean CD and profile of NPs with three different embedded  $\text{SiO}_2$  thicknesses - (a) 6.5 nm, (b) 8 nm, and (c) 10 nm.

oxide thicknesses from 6.5 to 10 nm. To complete the present work and reach the pillar diameter to the targeted value of < 12 nm, an additional CD reduction step is required and has been investigated using low-temperature-oxidation within the project.

### Author Statement

**M.-L. Pourteau:** Formal analysis, Data Curation, Writing - Original Draft, Writing - Review & Editing, Visualization.

**A. Gharbi:** Conceptualization, Methodology, Formal analysis, Investigation, Data Curation, Writing - Review & Editing, Visualization, Project administration.

**P. Brianceau:** Conceptualization, Methodology, Investigation, Writing - Review & Editing,

**J.-A. Dallery:** Investigation, Writing - Review & Editing.

**F. Laulagnet:** Investigation, Writing - Review & Editing.

**G. Rademaker:** Writing - Review & Editing, Project administration.

**R. Tiron:** Conceptualization, Supervision, Funding acquisition.

**H.-J. Engelmann:** Formal analysis, Investigation, Data Curation, Writing - Review & Editing, Visualization.

**J. von Borany:** Writing - Review & Editing, Project administration, Funding acquisition.

**K.-H. Heinig:** Supervision.

**M. Rommel:** Writing - Review & Editing.

**L. Baier:** Writing - Review & Editing.

### Declaration of Competing Interest

The authors declare that they have no affiliation with any organization with a direct or indirect financial interest in the subject matter discussed in the manuscript.

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