Carbon ion implantation as healing strategy for improved reliability in phase-change memory arrays

G. Bourgeois, V. Meli, F. Al Mamun, F. Mazen, E. Nolot, E. Martinez, J.-P Barnes, N. Bernier, A. Jannaud, F. Laulagnet, et al.

Carbon Ion Implantation as Healing Strategy for Improved Reliability in Phase-Change Memory Arrays

G. Bourgeois*, V. Meli, F. Al Mamun, F. Mazen, E. Nolot, E. Martinez, J.-P. Barnes, N. Bernier, A. Jannaud, F. Laulagnet, B. Hemard, N. Castellani, M. Bernard, C. Sabbione, F. Milesi, T. Magis, C. Socquet-Clerc, M. Coig, J. Garrione, M.-C. Cyrille, C. Charpin, G. Navarro* and F. Andrieu

CEA, LETI, Univ. Grenoble Alpes, 38000 Grenoble, France.
*Corresponding Authors: guillaume.bourgeois@cea.fr, gabriele.navarro@cea.fr

Abstract

In this paper we investigate the effect of Carbon ion implantation in $Ge_2Sb_2Te_5$ based Phase-Change Memory (PCM) targeting reliability improvement in 4kb memory arrays. We show how ion implantation by beam line allows to localize the Carbon in a specific volume of the active layer, demonstrating that a low C concentration (lower than 5 at. %) can be achieved with a high control thanks to dose monitoring. We evidence an outstanding improvement of the PCM cell performances, in both single devices and 4kb arrays, such as programming window widening and reduced variability of electrical parameters. We support our findings by TEM/EDS analyses demonstrating the healing effects of C ion implantation on interfaces and on retarding the phase-change layer segregation mechanisms.

Keywords: Phase-Change Memory (PCM), Reliability, Ion Implantation, 4kb arrays.

1. Introduction

Phase-Change Memory (PCM) is the most mature Non-volatile Memory Technology, showing an excellent compatibility with CMOS Back-End-of-Line (BEOL) integration process and a good scalability coupled to a demonstrated reliability for targeting both standalone and embedded applications [1]. Good thermal stability, high SET speed and large reading window enabling almost analog resistance levels (i.e. Multi-Level Cell) make PCM enough versatile to meet the requirements of automotive applications [2], Storage Class Memory [3] and neuromorphic computing [4]. However, some challenges remain to be achieved for next PCM products generation, like the lowering of programming current, the reduction of the resistance drift, and extremely low bit error rate (i.e. BER < ppm). Among the several studies proposed in order to improve the performance of standard $Ge_2Sb_2Te_5$ (GST) phase change material, light elements doping has been considered a key solution [5]. Main explorations of such strategy, adopt the doping by magnetron reactive (N, O etc.) or co- (C, Si etc.) sputtering of the phase change layer, prone to improve the thermal stability by increasing the crystallization temperature of the target alloy [6][7]. However, the introduction and control of carbon (C) in the GST layer at really low concentrations becomes challenging with standard co-sputtering techniques, which moreover can give rise to residual micro-voids and excess vacancies in the film [8].

In this light, we investigated the reliability of C-implanted GST (C-GST) Wall devices (**Fig. 1a**), obtained by C ion implantation, allowing localizing C whether at GST/electrode interfaces or uniformly in the whole layer (**Fig. 1b**). By SIMS profiles and XPS measurements, we highlight the possibility to perform a fine-tuning of C amount at low concentrations (i.e. less than 5%), confirming the simulated implantation profiles. We point out the benefits of ion implantation on PCM layer morphology and interfaces through TEM/EDS analyses. Therefore, we show through electrical characterization of C-GST single devices and 4kb arrays that C implantation leads to a reduction of the variability of both programming current and of SET/RESET distributions, leading to an improved reading window demonstrated with 100% arrays yield, obtained already with single pulse programming w/o program and verify protocols.

2. Physico-Chemical Characterization

2.1. Experiment design

Amorphous layers of GST were deposited at room temperature on both 200 mm Si and SiO_2 substrates by magnetron sputtering from pure GST target, protected by a 20 nm thick SiN capping layer, for material analyses. GST layers were integrated by same deposition technique in

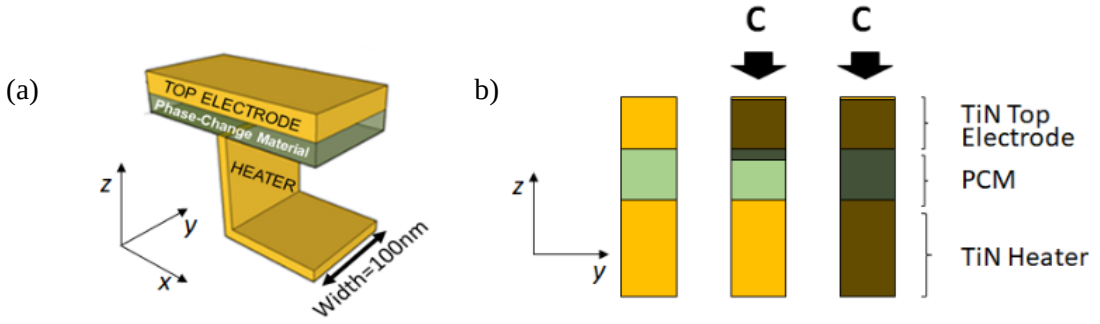

Fig. 1. (a) Simplified scheme of a GST Wall device. (b) C Ion-Implantation description: the black regions highlight the C implanted area through TEC layer after GST/TiN deposition. Different implantation profiles with a perfect control of the C amount at low percentage can be obtained thanks to Ion Beam energy/dose tuning with respect to co-sputtering Carbon deposition.

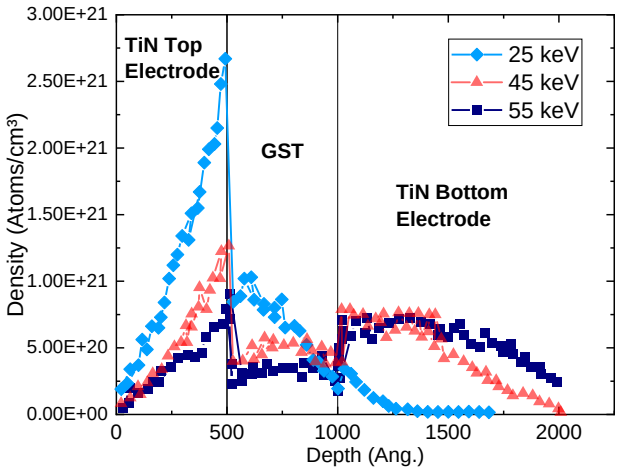

Fig. 2. Implantation profiles from TRIM simulations (C dose of 10^{16} at/cm^2). At 25keV we observe a high C density at the TEC/GST interface whereas a more uniform C profile is achieved at 45 and 55 keV. Higher doses allow passing through GST/Bottom Electrode interface, meaning carbon is also located in the TiN Heater area.

electrical wafers, followed by a TiN top electrode (TEC) deposition. C ion implantation was performed adapting ion beam doses and energies, based on TRIM Monte-Carlo Simulator results, in order to match the implantation profiles between SiN/GST and TiN/GST stacks. Implantation profiles examples, simulated for a dose of 10^{16} at/cm^2 are reported in **Fig. 2**. An energy of 25keV must be used in order to localize C at the interface TEC/GST, while at increasing beam energy (45 and 55keV) a more uniform C implantation is obtained in the GST layer. In order to tune the minimal dose required to improve the physical properties of GST, without deteriorating the device performances, a material study was carried out on GST as deposited amorphous layers (SiN capped) to confirm and match simulations results. Corresponding SIMS profiles from blanket wafers highlight a C concentration peak at the SiN/GST interface at 8 keV (**Fig. 3a**), evaluated by XPS Depth Profiling to correspond to about 6 at. % of C content for a dose of 10^{16} at/cm^2. In the case of 30 keV, for the same higher dose, a homogeneous C content of about 3 at. % is measured in the whole layer (**Fig. 3b**).

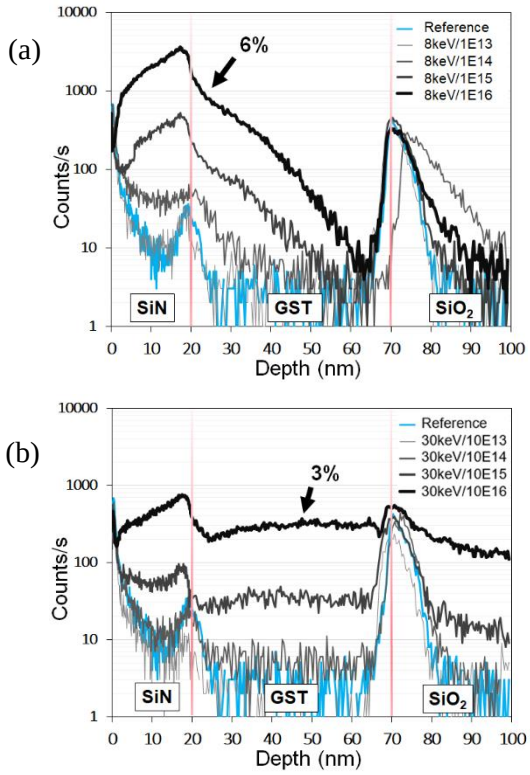

Fig. 3. (a) SIMS profiles of C implanted in 50 nm GST layer through 20 nm SiN at 8 keV increasing the dose from 10^{13} to 10^{16} at/cm^2 (reference is standard GST). As expected from TRIM simulations, the C is localized at the SiN/GST interface. Additional XPS Depth Profiling analyses for 10^{16} at/cm^2 dose allows to highlight a C concentration reaching about 6 at. % at the peak. b) A different profile is observed at 30keV, with a homogeneous C distribution in the whole layer. A concentration of 3 at. % of C is detected with XPS for same 10^{16} at/cm^2 dose.

2.2. C incorporation

Electrical resistivity as a function of temperature (**Fig. 4**) shows how a homogeneous C implantation is responsible for an improved amorphous phase stability against recrystallization [9]. On the contrary, the layer locally implanted at the top surface at 8 keV, does not show any visible effect of C on bulk layer crystallization dynamics. Ge-C bonds are evidenced by FTIR analysis, confirming the

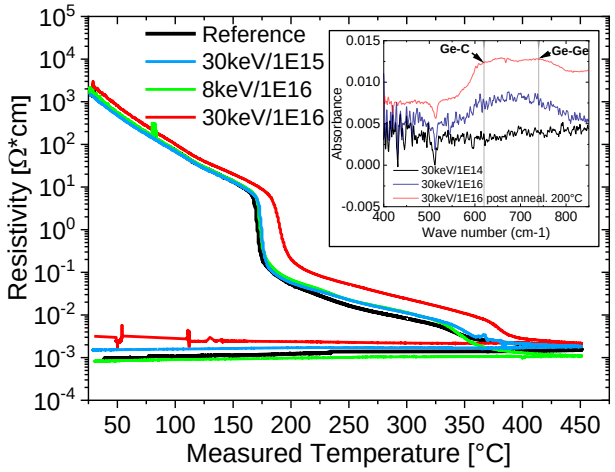

Fig. 4. Resistivity-vs-Temperature measurements on C-doped amorphous layers, showing an increase of the crystallization temperature in 30 keV-10^{16} at/cm^2 C-GST, that confirms the higher stability of C-doped GST against crystallization. In the Inset, FTIR analyses performed on C-doped samples evidence the formation of Ge-C and Ge-Ge bonds respectively at 620 and 740 cm^{-1} after annealing at 200°C.

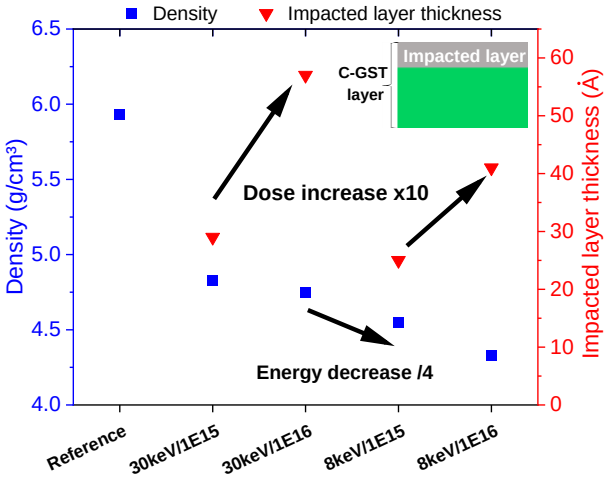

Fig. 5. Extraction of the C-GST layers density and impacted layer thickness by XRR. The decrease of the density is evident in all the C-doped layers, while the impacted thickness increases with the dose value.

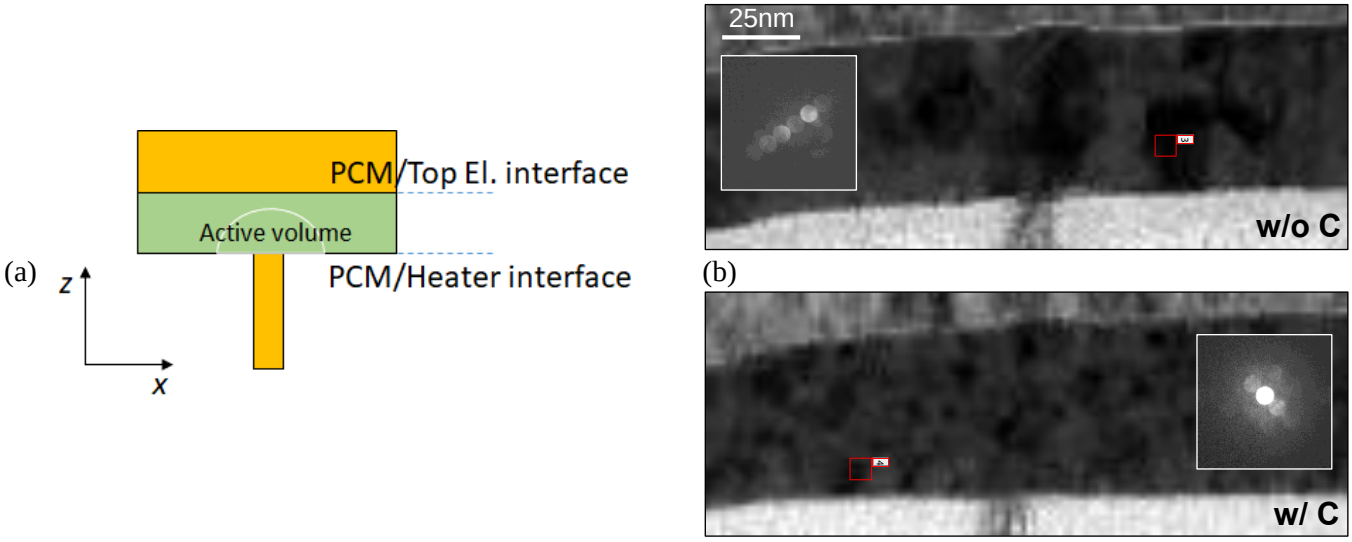

Fig. 6. (a) Simplified scheme of the PCM layer sandwiched between the Heater and the Top Electrode. (b) Corresponding NBED TEM analysis for standard GST (top) and 45 keV C-GST (bottom) devices out of fabrication. A finer and more homogeneous crystalline morphology is observed in C-GST with respect to GST.

right incorporation of C in the amorphous layer matrix. Data extracted from XRR analyses (**Fig. 5)** highlight:

a) a lowering of the density of the implanted layers (less than 5 g/cm^3) with respect to standard GST (equal to about 6 g/cm^3), correlated to a structural relaxation of the material featuring a higher number of defects due to the high dose exposure;

b) an increasing thickness of the impacted region when increasing the dose (from 10^{15} to 10^{16} at/cm^2). This is in accordance with a reduction of the internal stress of the amorhous $Ge_2Sb_2Te_5$ layer [10], with significant benefits in terms of relaxation of the contraints for the following of the BEOL of the integration.

2.3. TEM analyses on PCM devices after fabrication

GST and C-GST were integrated in state-of-the-art "Wall" PCM devices into the BEOL of the fabrication of LETI Memory Advanced Demonstrator (MAD) based on 130 nm CMOS technology. Nano-beam electron diffraction analysis (NBED) of as-fabricated devices performed along xz-plane (**Fig. 6**) highlights the more homogeneous crystalline morphology for C-GST layers with respect to standard GST. Indeed, the delay of the crystallization due to C introduction [6] ensures a less variable virgin state, while bigger and not homogeneously oriented crystals in standard

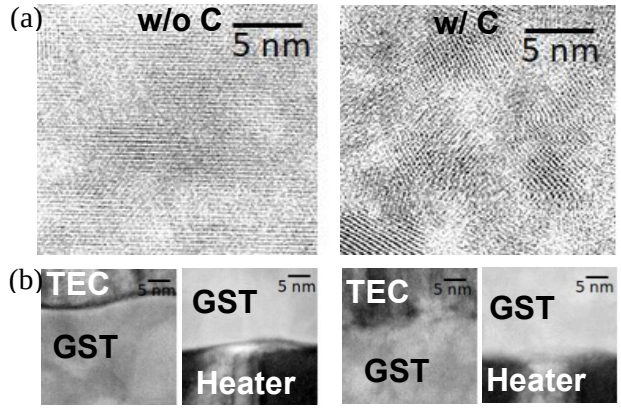

Fig. 7. (a) Bright Field TEM images of the PCM layer (virgin state) highlight smaller crystallites for C-GST (right) wrt standard GST (left). (b) Dark Field TEM images focusing on interfaces between the PCM layer and the TiN electrodes.

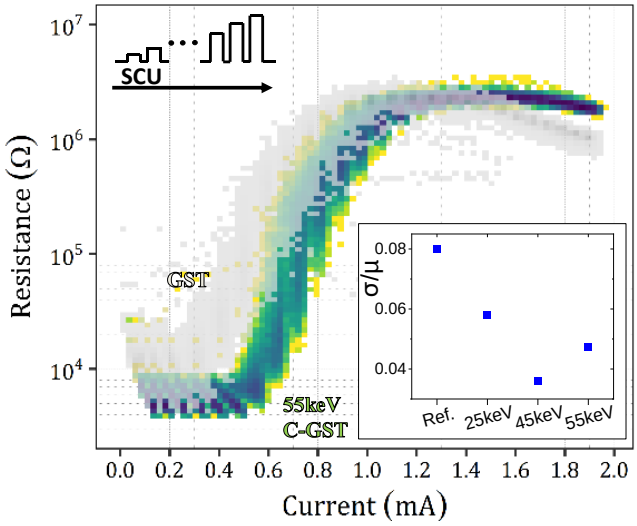

Fig. 8. R-I characteristics in 4kb arrays for the reference (i.e. standard GST) and 55 keV C-GST samples, obtained by a SCU procedure (composed by pulses of increasing amplitude with a duration of 300 ns). C-GST characteristics feature a lower variability than GST (shadowed), with a widening of the PW, made possible by a more reliable SET operation (i.e. a lower mean value for the SET resistance and a lower SET variability). In the inset we report the coefficient of variation σ/μ (std. dev. over mean value) of the programming current for all the studied C ion implantation energies.

GST could induce an intrinsic variability (**Fig. 7a**). Furthermore, TEM images focusing on interfaces between the PCM layer and TiN electrodes (**Fig. 7b**) show that C implantation through the whole layer drastically improves the interfaces quality. This interfaces healing effect under ion implantation is likely due to the breaking of Ti-O bonds that could intrinsically form during deposition, despite the controlled atmosphere. Indeed, Ti readily reacts with oxygen even at very low concentrations. The breaking of unwanted Ti-O bonds can lead to the formation of other bonds (i.e. Ti-Te) beneficial for interfaces adhesion and electronic conduction. As a consequence, we can expect an improvement during the devices initialization step and following programming operations, with a consequent better devices performances, in terms of endurance and array yield

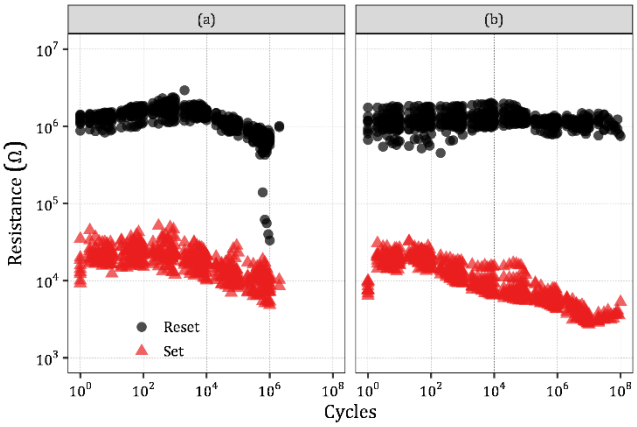

Fig. 9. (a) Endurance performance in standard GST (10 devices) featuring a failure after ~10^6 cycles, while 45 keV C-GST devices (b) cycled with the same conditions show a two decades improvement preserving a reliable programming after 10^8 cycles. RESET pulse: (rise/width/fall time) 10 ns/300 ns/10 ns. SET pulse: 10 ns/300 ns/1 μs (with amplitude equivalent to 60% of the one used for RESET pulse).

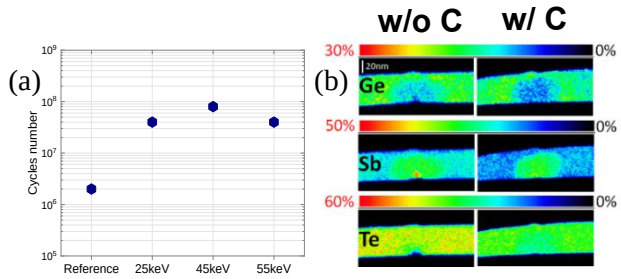

Fig. 10. (a) Better endurance performance confirmed in C-GST single devices up to more than 10^8 cycles (w/o pulse optimization). (b) Ge, Sb and Te TEM EDS analyses performed after 10^6 cycles highlighting a higher elemental segregation in standard GST with respect to 45 keV C-GST which features a homogeneous composition in the active volume.

enhancement (i.e. reduced variability).

3. Electrical Characterization

3.1. 4kb programming characteristics

To accomplish statistical analysis, the measurements were performed in 4kb arrays consisting of 1-Transistor-1-Resistor (1T1R) devices with a heater width of 100 nm. The R-I curves in **Fig. 8** show the SET-RESET transition obtained for all the devices of a GST and 55 keV C-GST 4kb arrays. Minimal SET state is obtained after a staircase-down (SCD) procedure, while a staircase-up (SCU) procedure allows reaching the maximal RESET state (both SCD and SCU using pulses with a duration of 300 ns). C-GST characteristics feature a low variability, with a widening of the programming window (PW) made possible by a reliable SET operation. Such reduced variability is confirmed by the coefficient of variation of the programming current, reduced up to more than twice in 45 keV C-GST.

3.2. Endurance and retention analyses

To compare the endurance capability in standard GST and C-GST, we used equivalent stress conditions (i.e. same

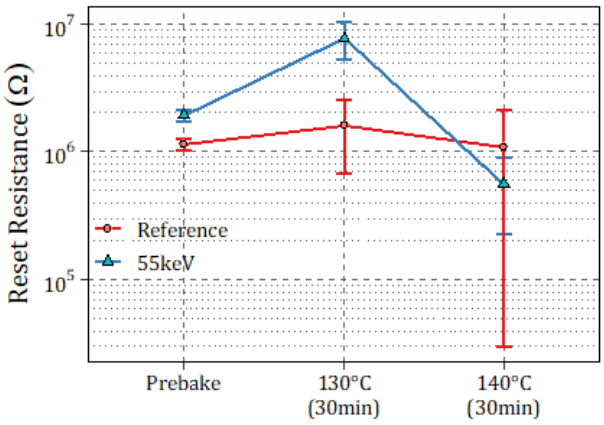

Fig. 11. Data Retention performed on GST and 55 keV C-GST 4kb arrays. C homogeneous distribution in the phase change layer is evidenced by the higher stability of C-GST at 130°C and 140°C.

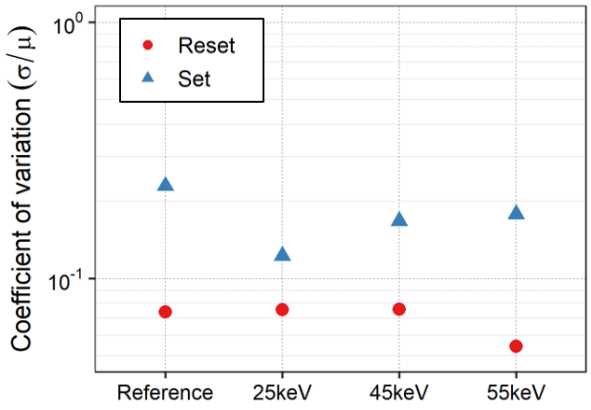

Fig. 13. Coefficient of variation (σ/μ) evaluated on SET/RESET distributions of Fig. 12 for each C implantation energy (dose = 10^{16} at/cm^2).

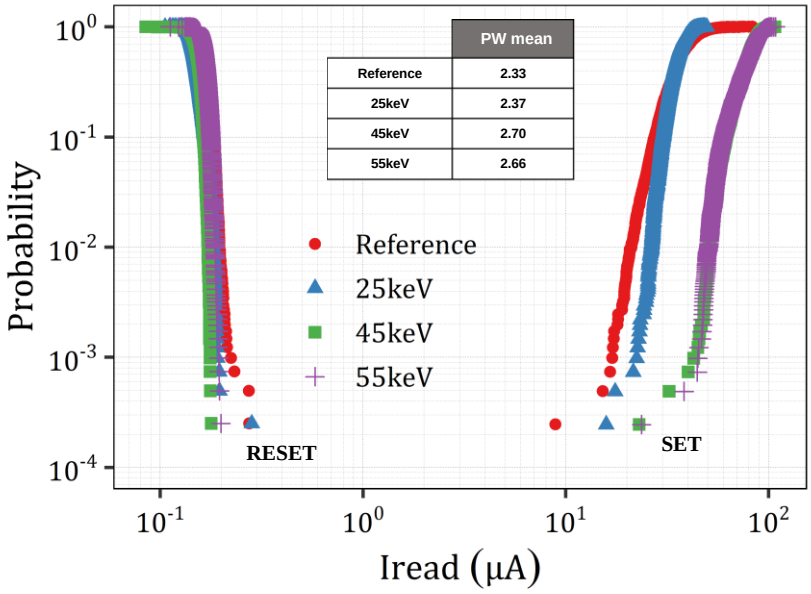

Fig. 12. 4kb SET and RESET distributions showing 100% arrays yield obtained without program-and-verify protocols. A widening of the PW is observed in 45 and 55keV C-GST (PW = $\log_{10}(R_{RESET}/R_{SET})$), thanks to the lowering of the SET resistance state. Programming states obtained after a staircase-down (SET state) and a staircase-up (RESET state), with pulse time width of 300ns.

energy transferred to the devices during the pulses) applying a sequence of SET and RESET pulses with equivalent amplitudes and shapes. The endurance reported in **Fig. 9a** based on single device tests, for standard GST and 45 keV C-GST, shows no impact of C implantation on devices cyclability. On the contrary, C is responsible for an improved endurance up to more than 10^8 cycles if compared to standard GST that start to fail after 10^6 cycles. Moreover C-GST shows a better RESET state stability along cycling, while material evolution is evidenced in standard GST already after 10^4 cycles [11]. It should be noted that no intelligent or optimized endurance procedures were applied voluntarily, in order to compare the behavior of the two materials with same cycling conditions.

Based on same endurance tests, we report in **Fig. 10a** the cycles number obtained for each C implantation energy, confirming the benefits of C, compatible with previous results obtained on GeSbTe doped by sputtering [8][12]. Such improvement at device level is mandatory for an implementation of PCM in large arrays to deploy reliable products [13]. The observed improvement in endurance in C implanted devices, could be correlated with the better electrode/phase-change layer interfaces, as previously observed in Fig. 7b. A more robust interfaces quality and a lower film density variation between amorphous and crystalline phases obtained by C introduction [7][8] prevent from thermal stress during the fabrication [14] and from electrical stress (i.e. unwanted current density peaks), in particular during first programming operations, during the device life time.

In order to understand the material evolution ongoing, we performed EDS analyses (**Fig. 10b**) after 10^6 cycles focusing on standard GST and 45 keV C-GST. EDS analyses highlight a higher elemental homogeneity of the active volume in C-GST cycled devices, also due to C atoms decreasing the atomic migration rate of Ge, Sb and Te [15].

Data retention tests performed on 4kb arrays (**Fig. 11**) reveal an improved stability of the RESET state in 55 keV C-GST

at 130°C, since only relaxation is observed, while standard GST features a crystallization that is accelerated at 140°C. This result is compatible with previously reported improvement of the retention thanks to C doping in phase-change layers [7].

3.3. SET and RESET distributions

Finally, SET/RESET distributions of 4kb arrays (**Fig. 12**) highlight the widening of PW for higher implantation energies with homogeneous C implantation (45 and 55 keV), supported by 100% arrays yield w/o the use of specific program and verify protocols. Implantation localized at the top surface (i.e. 25 keV C-GST) shows a reduced variability in the SET programming (**Fig. 13**), which can be attributed to a reduced thermal conductivity towards the top electrode of the cell (i.e. more efficient SET operation), giving rise to a more uniform crystallization.

3. Conclusions

In this paper, the benefit of C ion implantation in GST based PCM devices performances is demonstrated. Dose/energy parameters are extracted from simulations performed in TRIM Monte-Carlo Simulator to implant C uniformly in the whole layer (i.e. material tuning), or at the TEC/GST interface. Combining different physicochemical analyses, we study the real implantation profiles, the C content in the layers, and we highlight the reduced density, and healing effects of C implantation in GST. C-GST 4kb arrays feature a variability reduction of the electrical parameters with respect to standard GST, in particular observed in the programming current, SET/RESET distributions and retention, supported by a 100% arrays yield. Finally, an endurance enhancement up to more than 10^8 cycles, a more reliable SET operation and a higher programming window, confirm C ion implantation to be a valuable strategy to improve PCM array reliability.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgement

This work has been partially supported by the European 783176 WAKeMeUP Project, financed by European commission, French government and Auvergne-Rhône Alpes Region.

References

[1] P. Cappelletti et al., "Phase change memory for automotive grade embedded NVM applications", J. Phys. D: Appl. Phys. 53 193002, 2020.

[2] F. Arnaud et al., "Truly Innovative 28nm FDSOI Technology for Automotive Micro-Controller Applications embedding 16MB Phase Change Memory", 2018 IEEE International Electron Devices Meeting (IEDM), 10.1109/IEDM.2018.8614595.

[3] G. Navarro et al., "Highly Sb-Rich Ge-Sb-Te Engineering in 4Kb Phase-Change Memory for High Speed and High Material Stability Under Cycling", 2019 IEEE 11th International Memory Workshop (IMW), 10.1109/IMW.2019.8739656.

[4] G. W. Burr et al., "Neuromorphic computing using non-volatile memory" Advances in Physics, : X, vol.2, n°1, 2017, https://doi.org/10.1080/23746149.2016.1259585

[5] J. Kim et al., "Physical and electrical characteristics of Ge_xSb_{100-x} films for use as phase-change materials", Thin Solid Films, pp. 659, 1-6, 2018, https://doi.org/10.1016/j.tsf.2018.05.034.

[6] Q. Hubert et al, "Lowering the Reset Current and Power Consumption of Phase-Change Memories with Carbon-Doped $Ge_2Sb_2Te_5$", 2012 IEEE 4th International Memory Workshop (IMW), 10.1109/IMW.2012.6213683

[7] W. Zhou et al., "High thermal stability and low density variation of carbon-doped $Ge_2Sb_2Te_5$ for phase-change memory application" APL, 105(24), 243113, 2014, https://doi.org/10.1063/1.4904832

[8] J. H. Park et al, "Enhancement of a cyclic endurance of phase change memory by application of a high-density $C_{15}(Ge_{21}Sb_{36}Te_{43})$ film", AIP Advances 6, 025013, 2016, https://doi.org/10.1063/1.4942110.

[9] E. Cho et al., "Enhanced amorphous stability of carbon-doped $Ge_2Sb_2Te_5$: Ab Initio investigation", Applied Physics Letters (APL), 99(18), 183501, 2011, https://doi.org/10.1063/1.3657139

[10] G. D'Arrigo et al., "Mechanical properties of amorphous $Ge_2Sb_2Te_5$ thin layers", Surfaces and Coating Technology 355, 2018, https://doi.org/10.1016/j.surfcoat.2018.02.050

[11] Y. Wang et al., "RESET failure analysis of phase change memory based on $Ge_2Sb_2Te_5$" IEICE Electronics Express, Vol.14, No.17, 1–6, 2017, DOI: 10.1587/elex.14.20170673

[12] C-F. Chen et al., "Endurance Improvement of $Ge_2Sb_2Te_5$-Based Phase Change Memory", 2009 IEEE International Memory Workshop (IMW), 10.1109/IMW.2009.5090589.

[13] B. Gleixner et al, "Reliability characterization of Phase Change Memory", 2009 10th Annual Non-Volatile Memory Technology Symposium (NVMTS), 10.1109/NVMT.2009.5429783

[14] J-T. Li et al, "Thermal effect of $Ge_2Sb_2Te_5$ in phase change memory device", International Conference on Nanoscience & Technology, China 2013, 10.1088/1674-1056/23/8/087804.

[15] T-Y. Yang et al, "Effects of dopings on the electric-field-induced atomic migration and void formation in $Ge_2Sb_2Te_5$", 18th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), 2011, 10.1109/IPFA.2011.5992717.