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Multilevel Programming Reliability in Si-doped GeSbTe for Storage Class Memory

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Abstract-Phase-Change Memory (PCM) demonstrated to be a promising Non-Volatile Memory technology to address Storage Class Memory (SCM) applications that can be distinguished in memory-type and storage-type. In this work we show how α GeSbTe (α GST) alloy can address both SCM types, in particular using Si doping. Thanks to electrical characterization of 4 kb PCM arrays, supported by TEM analyses, we demonstrate how Si doping in α GST can lead to a huge improvement of MLC operations using a double-pulse protocol. This result, combined with an improved data retention, proves Si-doped α GST suitability for storage-type SCM, whereas high endurance and high speed in undoped α GST allows to target memory-type SCM.

Keywords- PCM, SCM, GeSbTe, Si-doping, multilevel

I. INTRODUCTION

Phase-Change Memory (PCM) entered recently in the market with the objective to fill the gap in performances between main memory and storage, concretizing the concept of Storage Class Memory (SCM) [1]. In this revolutionized memory hierarchy, SCM can be closer in terms of performance either to memory (M-SCM) or storage (S-SCM). M-SCM requires speed and endurance, on the contrary, S-SCM must be truly non-volatile (i.e. good data retention) and must provide higher density at a lower cost [2]. In order to improve the density without impact on masks addition and costs, multi-level cell (MLC) capability becomes a key feature. In this paper we investigate Si-doping in α GeSbTe (α GST) phase-change material to easily tune the crystallization degree in PCM devices, achieving an extremely low variability of intermediate resistance states. TEM analyses are used to support our findings. Therefore, we demonstrate more reliable MLC operations in Si-doped α GST 4 kb arrays applying a simple double-pulse programming protocol. Finally, our results enable α GST as promising candidate for SCM, making possible to address at the same time M-SCM, thanks to its high SET speed and endurance, and S-SCM, if doped with the right Si content.

II. DATA/RESULTS AND DISCUSSION

α GST and Si-doped α GST with two different Si concentration (α GST+Si1 and α GST+Si2, with respectively lower and higher Si percentage), were integrated in “Wall” PCM 4 kb arrays, for electrical measurements and statistical analysis, and on blanket wafers for material analyses.

The resistivity as a function of temperature of as-deposited amorphous layers is reported in Fig. 1. Both the resistivity and the crystallization temperature increase as the Si amount increases, since likely Si concentrates at the grain boundaries suppressing grain growth and retarding the crystallization process [3]. The resistance-vs-current (R-I) curves (Fig. 2) show that RESET current decreases in Si doped devices, with a reduced variability of R-I characteristic in α GST+Si2. However, the Si-doping leads to a lower crystallization (i.e. SET) speed (Fig. 3).

The subthreshold slope ($STS = d\ln(I)/dV$) measured in RESET devices, reported in Fig. 4, evidences that in α GST the conduction depends considerably on the temperature, whereas STS remains constant with temperature in Si-doped α GST. STS variation as a function of $(kT)^{-1}$ is proportional to the trap-to-trap distance Δz [4] that is higher in α GST than in α GST+Si, indicating that Si-doped α GST contains a higher number of defects introduced by Si, which gives rise to an amorphous structure with a higher disorder and more stable against crystallization.

We analyzed the crystallization process applying a series of short pulses (20 ns) in α GST and α GST+Si2 devices pre-programmed in RESET state (Fig. 5). A gradual expected crystallization is observed in α GST. On the contrary, α GST+Si2 resistance decreases and stabilizes at about $10^5 \Omega$, and only after applying about hundred pulses the resistance starts to decrease again down to the same α GST SET resistance. It confirms that Si retards the crystallization process and brings the advantage of a reliable

intermediate state. This behavior is statistically confirmed in 4 kb arrays using a single squared pulse of $\sim 1 \mu s$ (Fig. 6). Transmission Electron Microscopy (TEM) images of devices programmed in the intermediate state (Fig. 7a) and in SET state (Fig. 7b) evidence that the SET state features a long range crystalline structure, otherwise the intermediate state contains localized crystalline grains embedded in an amorphous matrix. To establish the best protocol to achieve multiple resistive states (MLC) in α GST and α GST+Si2 arrays we studied different programming pulses varying durations and current amplitudes, starting either from SET state (Fig. 8c-d) or from RESET state (Fig. 8a-b, Fig. 9). In α GST, the variability is higher in each test realized, while α GST+Si2 shows a low variability when a $1 \mu s$ long squared pulse is applied on RESET cells (Fig. 8b). An even finer control (Fig. 9c) with low variability (Fig. 9d) of the programmed resistance is obtained in α GST+Si2 tuning the pulse fall time. The endurance of the 3 states (SET, RESET and intermediate) is showed to depend on RESET pulse duration (i.e. energy). A low energy 30 ns RESET pulse allows to reach 10^5 cycles with no degradation of the programmed states (Fig. 10), while a longer RESET pulse of 300 ns, leads to an early degradation of both SET and intermediate states, with a probable Si migration outside of the active region of the device. Endurance tests with different SET/RESET pulses durations (i.e. energy) were realized to extrapolate the maximum endurance achievable with the minimum programming time (Fig. 11) [5]. The failure conditions to calculate the number of cycles take into account a reduction of the RESET resistance and of the reading window, but we added for α GST+Si2 the condition on the degradation of the SET state, which is correlated to the loss of the intermediate state (Fig. 10a). Indeed, the endurance in α GST+Si2 could be higher than 10^8 (inset in Fig. 11), despite the loss of MLC behavior. We extrapolate a higher endurance for α GST than in α GST+Si2 (MLC).

Furthermore, Si-addition in α GST improves the RESET and the intermediate state retention at $100^\circ C$ as illustrated in Fig. 12, due to the higher crystallization temperature of Si-doped α GST (Fig. 1).

A multilevel iterative program-and-verify (PV) protocol is proposed in which the programming current (I_n) is updated at each iteration, depending on whether the resistances obtained are lower or higher than the target range, and the device pre-programmed in the RESET state (Fig. 13). Already using only a double-pulse operation (RESET + programming) the percentage of devices in the 4 kb array reaching the target resistance range is higher in α GST+Si2 than in α GST. A single PV iteration is not sufficient for α GST to reach the same α GST+Si2 yield, demonstrating the high suitability of α GST+Si2 in MLC operations.

III. CONCLUSIONS

This work investigates the effects of Si-doping in α GST. In particular, we show an improvement of MLC capability in Si-doped α GST and a better data retention than undoped α GST. These characteristics make α GST suitable for S-SCM if properly doped with Si, and at the same time M-SCM thanks to the high speed and high endurance of undoped α GST (Fig. 14).

ACKNOWLEDGEMENTS

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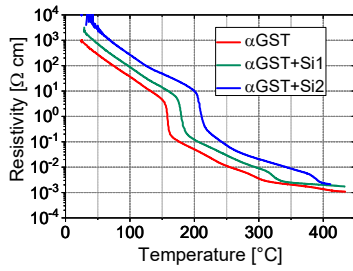


Fig. 1. Resistivity of as-deposited α GST, α GST+Si1, α GST+Si2 as a function of temperature measured at a rate of $10^\circ\text{C}/\text{min}$.

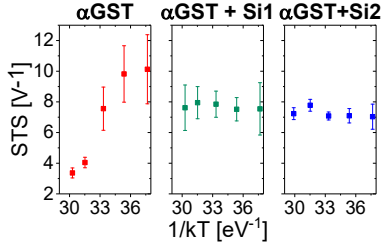


Fig. 4. Subthreshold slope (STS) calculated at different temperatures (4 devices for each composition) is represented as a function of $1/kT$.

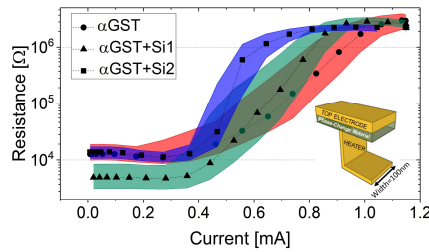


Fig. 2. Resistance-vs-Current characteristics for α GST, α GST+Si1, α GST+Si2 based PCMs: median, 16th and 84th percentiles (corresponding to 1σ) of the resistance values obtained in 4kb arrays are represented. On the bottom right is reported the scheme of a typical "Wall" PCM device used in this work.

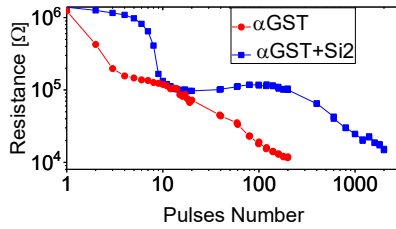


Fig. 5. Resistance achieved in α GST and α GST+Si2 devices, starting from a RESET state, applying consecutively a sequence of short pulses with 10 ns rise/fall time and 20 ns width time.

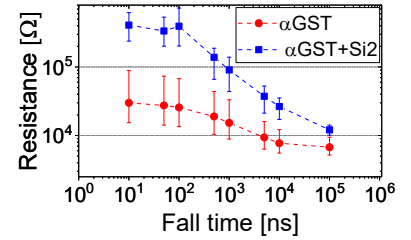


Fig. 3. SET programming speed test performed in 4 kb arrays with constant pulse width (300 ns) and increasing pulse fall time: median, 16th and 84th percentiles of the resistance values are represented.

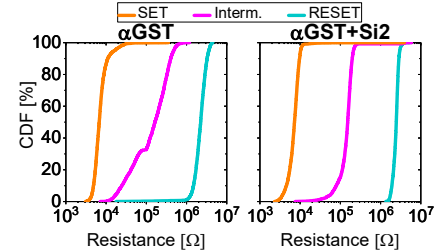


Fig. 6. Cumulative distributions of resistances measured in α GST and α GST+Si2 4 kb arrays. The intermediate state is achieved with a current of 0.2 mA and a long width time pulse ($\sim 1\mu\text{s}$).

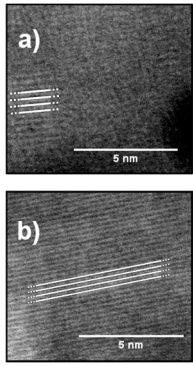


Fig. 7. TEM images performed in the active region of two α GST+Si2 devices programmed respectively in the intermediate state (a) and in the SET state (b).

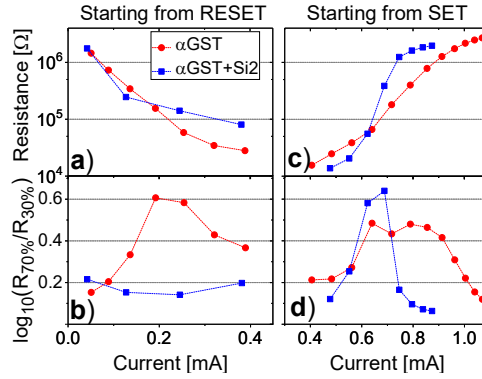


Fig. 8. Intermediate states achieved starting from RESET state (a,b) with $1\mu\text{s}$ square pulses and from SET state (c,d) with 300 ns square pulses. Median (a,c) and variability (b,d) of the resistances in 4 kb arrays are represented.

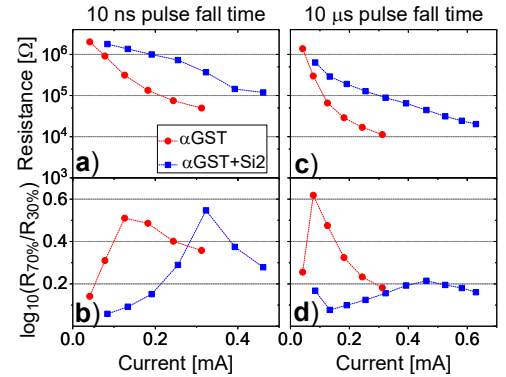


Fig. 9. Intermediate states achieved starting from RESET (a,b) with 10 ns pulse fall time (a,b) and $10\mu\text{s}$ pulse fall time (c,d), the width time is 300 ns for both. Median (a,c) and variability (b,d) of the resistances in 4 kb arrays are represented.

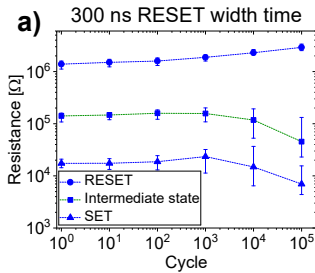


Fig. 10. Endurance test performed in α GST+Si2 applying a RESET pulse with a width time of 300 ns (a, top graph) and 30 ns (b, bottom graph) on a population of about 100 devices.

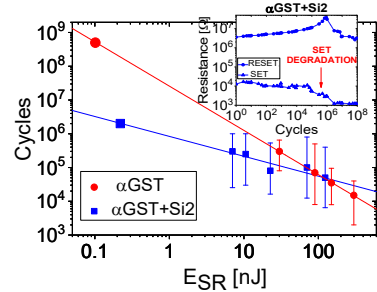


Fig. 11. Number of cycles achieved for different SET+RESET pulses duration (i.e. energy) in α GST and α GST+Si2 devices allowing to extrapolate a higher endurance in α GST. Each condition was applied on a population of about 40 devices. Median and 1σ are represented. In the inset, an endurance test on a α GST+Si2 device.

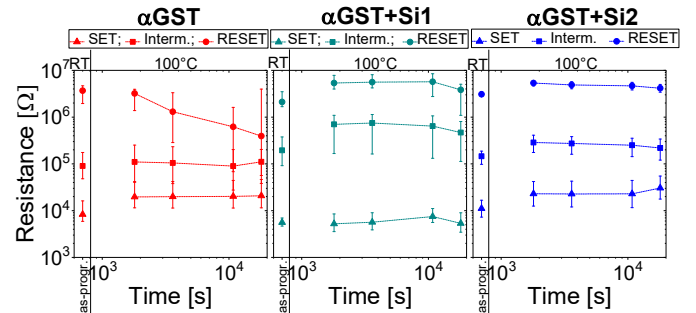


Fig. 12. Data retention at 100°C of SET, RESET and an intermediate state for the three compositions measured in 4kb arrays. Median and 1σ are reported after programming (as.-progr.) at room temperature (RT) and along time after annealing at 100°C .

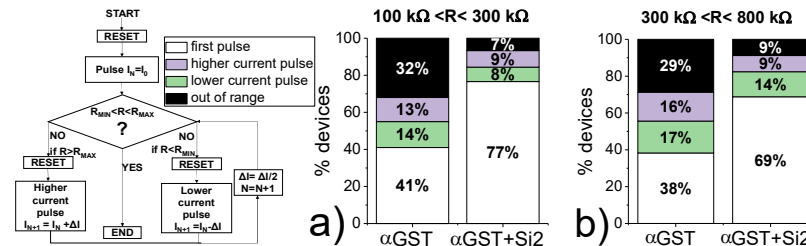


Fig. 13. Program-and-Verify (PV) protocol used to get intermediate resistive states in α GST and α GST+Si2 4kb arrays. The target intermediate resistance range is reported above the graphs a) and b). In white, the percentage of the devices getting the target after the first programming pulse, in purple and in green the devices getting the target after a single-step of PV and in black those remaining out of the range.

| | Retention at 100°C | Multilevel capability | Speed | Endurance |
|------------------|----------------------------------|-----------------------|-------|-----------|
| α GST | Low | Low | High | High |
| α GST+Si2 | High | High | Low | Low |

Storage-type SCM Memory-type SCM

Fig. 14. Summary of the features achieved in α GST and α GST+Si2 based PCM devices, showing the possibility to target both S-SCM and M-SCM specifications.