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Phase-Change Memory Electro-Thermal Analysis and Engineering Thanks to Enhanced Thermal Confinement

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Abstract

In this paper we compare the performances of SiN with respect to an optimized SiC encapsulation in Wall based Phase-Change Memory (PCM) integrating a Ge-rich Ge-Sb-Te alloy (GGST) suitable for high temperature stability in automotive applications. Thanks to the electrical characterization of 4kb arrays, 3D electro-thermal simulations and TEM analyses performed on programmed devices, we demonstrate the higher programming efficiency in SiC-based PCM devices, thanks to the lower thermal conductivity of the optimized encapsulation. Indeed, the uniform temperature profile achieved in the active layer of SiC encapsulated PCM leads to a retention of one hour at 250 °C. A theoretical model is here proposed to describe the electro-thermal behavior of the device, linking the electrical properties, such as the resistance as a function of current characteristics, to the thermal conductivity of the materials that constitute the device. Finally, thanks to our findings, we provide some guidelines to achieve drastic current reduction via the thermal engineering of the next generation PCM technology.

Keywords: Phase-Change Memory (PCM), thermal confinement, encapsulation layer, thermal conductivity, electro-thermal simulations.

1. Introduction

Phase-Change Memory (PCM) is the most mature among the emerging non-volatile memories (NVM) and it represents a reliable alternative to Flash technology. Indeed, it recently entered the market addressing Storage Class Memory (SCM) applications [1]. Moreover, PCM demonstrated to fulfill the automotive market requirements thanks to the phase-change material engineering. In particular, the use of Ge-rich Ge-Sb-Te alloys (GGST) ensures a data retention of ten years for temperatures higher than 150 °C [2]. Nevertheless, the main challenge to be overcome in PCM to target ultra low power applications in advanced technology nodes is the programming current reduction. Main efforts in recent years have been oriented to the development of scaled architectures [3, 4] and to the engineering of the active material [5, 6]. However,

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the main part of the power used during the programming operations of a PCM device is represented by the heat losses [1], making the PCM performance to be far from the adiabatic limit represented by a perfect thermal isolation and zero losses [7]. Only in the last years, with the increasing in maturity of the PCM technology, the engineering of thermal barriers and of the thermal conductivity of the surrounding dielectrics became the object of preliminary studies confirming the huge improvement achievable already in analytic devices [8, 9] and demonstrating its even higher necessity in ultra scaled PCM [10]. In this framework, we propose the investigation of the thermal improvement in heater-based (i.e. "Wall") state-of-the-art PCM structures [4] based on GGST alloy. Thanks to the introduction of an optimized SiC encapsulation layer featuring low thermal conductivity we highlight the benefit of an improved thermal isolation, with respect to standard SiN, by statistical electrical results obtained on 4kb arrays. In particular, we show the higher efficiency of the RESET operation (i.e. amorphization), which leads to a more uniform amorphous region and an improved data retention [11]. The electrical results are validated here by 3D electro-thermal simulations and Transmission Electron Microscopy (TEM) observations combined to Energy-dispersive X-ray (EDX) spectroscopy performed on programmed devices. Finally, we present a physical model to correlate the resistance-vs-current (RI) characteristic to the thermal conductivity of the dielectrics surrounding the cell, validating it thanks to the electrical and thermal data acquired. We provide a clear demonstration of the importance of the thermal properties engineering not only of the phase-change layer (PCL) but also of the dielectrics surrounding the heater, and we show the correlation of such properties to the final electrical characteristics of the PCM device.

2. Device fabrication and electrical characterization

The thermal conductivity of the SiN and SiC layers used as encapsulation were measured by 3ω method [12] giving a value of 0.41 $Wm^{-1}K^{-1}$ for SiC and 1.39 $Wm^{-1}K^{-1}$ for SiN [11]. The SiN and SiC encapsulation layers were deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) on the sides of the PCM device after the etching of the PCL (**Fig. 1**), based on a GGST alloy integrated by sputtering from single target. The PCM devices were fabricated in the Back-End-Of-Line (BEOL) process of our LETI Memory Advanced Demonstrator (MAD), based on 130 nm CMOS technology, used for statistical electrical parameters evaluation thanks to embedded 4kb arrays. The used BEOL process thermal budget is estimated in the order of about 30 minutes at 400 °C. For our electrical and physico-chemical analyses we considered devices with a wall width of about 80 nm and in the following we will refer to the devices by the material of their encapsulation (i.e. SiC or SiN).

The RI characteristics were measured for both SiC and SiN devices in 4kb arrays. After a seasoning procedure of ten SET/RESET cycles, the devices were initialized in the SET state (i.e. crystalline phase) with a pulse having a long fall time (SET-init) in order to achieve the lowest possible SET resistance state (i.e. rise/width/fall times equal to 10ns/300ns/10µs) for both SiC and SiN cells. The gradual resistance increase towards the RESET state is obtained with a staircase-up sequence of squared pulses (SP) of increasing voltage (i.e. current) amplitude, having rise/width/fall time equal to 10ns/300ns/10ns, pre-programming the device in the SET state with a SET-init pulse before each SP. The results are reported in **Fig. 2**. The different starting SET resistance, obtained by the specific procedure described above, is likely related to a different Ge expulsion during the forming operation [13] and the likely presence of residual amorphous regions due to the different thermal isolation, as it will be confirmed in following analyses. The different starting resistance, influences the "melting current" (I_m represented by the first detection of resistance increase in the RI curve), as already reported in previous works [14]. In particular, SiN based devices feature a melting current about 100 µA lower than the SiC based one. Both RI curves present two different slopes after reaching I_m, identified as s_1 and s_2 and reported in **Table 1**, highlighting a steeper resistance increase in SiC (i.e. higher s_1 and s_2).

An isochronal annealing of one hour at increasing temperatures (from 150 °C up to 250 °C) was applied to test the data retention performances comparing SiC and SiN. The results are reported in **Fig. 3** and are performed on a population of 2kb (half 4kb matrix) for both SET and RESET states. The SET state in both devices faces a known SET drift [15] up to 150 °C before to trigger the crystallization mechanism at higher temperature with a consequent resistance decrease. SiC devices show a very good SET and RESET retention

material	s_1 $[dec/mA]$	s_2 $[dec/mA]$
SiC	3.41 ± 0.36	1.74 ± 0.01
SiN	1.96 ± 0.03	0.95 ± 0.01

Table 1. Slopes (s_1, s_2) and variance for both SiC and SiN devices, obtained from the RI characteristics reported in **Fig. 2**.

up to 250 °C, while SiN devices programmed in RESET state face a 25% of failures after such annealing. As demonstrated in the following, the different behavior is likely related to a different in the amorphous region morphology between SiN and SiC which is achieved in the device active volume (i.e. programmed volume) after programming it in the RESET state.

3. Electro-thermal simulations and TEM/EDX analyses

We performed 3D electro-thermal simulations in COMSOL Multiphysics in order to analyze the impact of the encapsulation on the PCM cell, introducing SiC and SiN thermal conductivities previously measured. Methods and parameters used are described in previous works [16]. The different initialization is taken into account by tuning the electrical conductivity of the PCL to get a match between the simulated and the experimental SET resistance. Being the structure symmetric with respect to the z-axis in the zy-plane (see Fig. 1), only half of the structure is simulated. The temperature profile achieved in the two systems is reported in **Fig. 4**. The volume and the shape of the region reaching a temperature higher than 930 K (i.e. melting temperature of the phase-change material) is not the same in the two structures. In SiC the melted region in the PCL is larger and more uniform along the y axis, while in SiN the temperature decreases moving from the center (y = 0 a.u.) to the heater/encapsulation interface (y = 0.4 a.u.). This explains why SiC has a higher resistance when programmed at 1.2 mA in RESET state in Fig. 2, being the amorphized volume thickness more uniform in SiC than in SiN. A more specific analysis is presented in the next subsections for both SiN and SiC, describing in detail how the temperature profile changes in the PCM device increasing the programming current. In this investigation, the value of the simulated I_m is represented by the current at which the PCL starts to melt.

3.1. SiN encapsulation

In order to understand the temperature profile achieved in the device, we analyzed the isotherms reaching 930 K in both the PCL and the heater and measured their distance from the PCL/heater interface (h_{930K}). The evolution of h_{930K} in the PCL and in the heater at the center of the cell (i.e. y = 0 a.u.) and at the PCL/encapsulation interface (i.e. y = 0.4 a.u.) are reported as a function of the applied current in a.u. since the simulated device has a different width than the measured one (**Fig. 5a**). SiN based PCM starts to melt at the center of the heater width for an applied current of 0.4 a.u., whereas the melting at the PCL/encapsulation interface is achieved at 0.6 a.u.. Only at high current the melted thickness becomes homogeneous on the heater surface, and the heat propagation in the heater becomes really important. The position of the maximum temperature (T_{max}) along the z-axis during the programming operations in both previous analyzed regions of the cell (i.e. y = 0 a.u. and y = 0.4 a.u) is reported in **Fig. 5b**. At low current, T_{max} is localized inside the PCL at both y positions, while at increasing current the scenario changes: in the center we observe a gradual localization of T_{max} at the PCL/heater interface, while at the PCL/encapsulation interface T_{max} is already inside the heater. TEM/EDX images acquired along zx and zy plane of SiN devices programmed in the RESET state are reported in **Fig. 6**. The EDX maps along the zy plane (Fig. 6a) shows a not uniform active region on the top of the heater, well evident in the Sb map, compatible with what observed in simulations. On the contrary, along the zx plane (Fig. 6b), the elemental distribution results to be more homogeneous due to the signal integration along the whole lamella thickness, which confirms a higher elemental profile change mainly only along the y-axis. A slight evidence of the shape of the active region is however present in the Sb and Te maps.

3.2. SiC encapsulation

Same analyses performed for SiN are reported here for SiC in **Fig. 7** (simulations) and **Fig. 8** (TEM/EDX). The melting of the PCL is reached for both center and border at 0.5 a.u.. with a h_{930K} evolution at increasing current almost identical at both y positions. This confirms that the thickness of the melted region (i.e. that becomes amorphous volume after the RESET pulse application) is uniform over the heater/PCL interface along the y-direction, as expected from Fig. 4b. The position of T_{max} (Fig. 7b) at increasing current is also confirming a good homogeneity of the temperature distribution along the y-axis in the cell (i.e. well matched behavior between center and border). As observed for SiN, at low current T_{max} is localized in the PCL, while increasing the current T_{max} shifts inside the heater. The TEM/EDX of a RESET cell along zy plane (Fig. 8a) shows a uniform elemental distribution over the heater/PCL interface in all the Ge, Sb and Te maps. Moreover, the active volume is clearly evidenced along zy plane (Fig. 8b) since uniformly achieved on the whole heater/PCL surface (y-direction) and along the whole lamella thickness (of about one hundred nm), with an elemental distribution compatible with previous works [17, 13]. Such homogeneity, achieved thanks to SiC encapsulation, is in agreement with simulations results.

4. Electro-thermal theoretical analysis and discussions

The double slope behavior evidenced in the RI characteristic of both devices in Fig. 2, can be correlated to the different programming scenario that is achieved in the cell for different current amplitudes. As observed in simulations, the transition of the temperature profile from the PCL to the heater, is the origin of the double slope. In first approximation we can describe the electro-thermal behavior of the cell in 2D along the zy plane, as previously reported [4]. We can consider that the resistance value R achieved in the PCM device after the pulse application can be expressed as a function of the amorphous thickness obtained in the cell:

$$R \simeq \int_0^{h_{am}} \rho_{am} \frac{dz}{\pi z\ w} \propto ln(h_{am}) \tag{1}$$

where h_{am} is the amorphous thickness, ρ_{am} the resistivity of the amorphous phase and w the width of the heater along the y direction. We considered a uniform semi-cylindrical amorphous shape over the heater. In such system, the heat distribution is driven by the stationary heat transfer equation, that can be simplified as:

$$\frac{\partial^2 T}{\partial z^2} \simeq -\frac{\rho_{ON}\ I^2}{k_{th,eff}} \tag{2}$$

where ρ_{ON} represents the device resistivity when the PCL is melted during the pulse application, T is the temperature along the z-axis, $k_{th,eff}$ is the effective thermal conductivity associated to the overall system, while I is the current applied to the device and which has the role to induce a specific temperature profile inside the cell thanks to the achieved current density J at the PCL/heater interface ($I = Jwt$ with t the heater thickness along the x-axis). Considering the height of the melted region equal to the height of the amorphous final region ($h_{930K} = h_{am}$) we can write from equation eq. (2):

$$\Delta T_i \propto \frac{I^2}{k_{th,eff}} h_{am}^2 \tag{3}$$

where ΔT_i represents the temperature increase achieved at the heater/PCL interface (with respect to room temperature), and giving rise to the following correlation between h_{am} and I:

$$\frac{dh_{am}}{dI} \propto \frac{\sqrt{\Delta T_i\ k_{th,eff}}}{I^2} \tag{4}$$

Introducing the known correlation between power (P) and temperature we have:

$$\Delta T_i = R_{TH} P \propto R_{TH} I^2 \tag{5}$$

where R_{TH} is the global thermal resistance of the device. We can finally simplify eq. (4), considering the linear proportionality between R_{TH} and the reciprocal of the effective thermal conductivity of the system $k_{th,eff}$:

$$\frac{dh_{am}}{dI} \propto \frac{R_{TH}\ \sqrt{k_{th,eff}}}{\sqrt{\Delta T_i}} \propto \frac{1}{\sqrt{k_{th,eff}}} \tag{6}$$

This correlation is in agreement with expectations, namely that the thickness of the amorphous region achieved in the cell when a specific current is applied increases when the thermal conductivity of the surrounding materials is reduced. Therefore, since the resistance R depends on h_{am}, we can finally correlate the slope of the RI curve of Fig. 2 (i.e. s_1 or s_2) to the thermal conductivity of the system:

$$s = \frac{d\ ln(R)}{dI} = \frac{d\ ln(R)}{dh_{am}} \frac{dh_{am}}{dI} \propto \frac{1}{\sqrt{k_{th,eff}}} \tag{7}$$

The electrical results obtained from 4kb were performed on totally equivalent devices, except for the different encapsulation layer. This allows us to validate the relation in eq. (7), by calculating the ratios between the slopes in Table 1 and correlating them with the ratios between the measured thermal conductivities. Therefore, the ratio between the two s_1 is SiC and SiN, and the two s_2 should depend only on the ratio between the thermal conductivities of the two materials and this is confirmed by the following calculation:

$$\frac{s_{1,SiC}}{s_{1,SiN}} = \frac{s_{2,SiC}}{s_{2,SiN}} = \frac{\sqrt{k_{th,SiN}}}{\sqrt{k_{th,SiC}}} \sim 1.8 \tag{8}$$

This evidences that the difference between the evolution of SiC and SiN RI curves is strongly related to the value of the thermal conductivity of the encapsulation layer which is in direct contact with the PCL and the heater. Therefore, the choice of the encapsulation layer is fundamental in the tuning of the zy plane temperature profile of a Wall based PCM and further optimization can allow an even steeper slope in the RI curve, leading to a current reduction for the RESET operation.

The lower uniformity along y-axis observed in SiN devices can explain the lower I_m found in Fig. 2 with respect to SiC. Indeed, some amorphous residuals featuring low thermal conductivity could be generated by such non-homogeneous temperature profile, reducing the current needed to melt the active volume in the PCL. The amorphous residuals are compatible also with the increased SET resistance in SiN devices with respect to SiC.

An other validation of eq. (7) can be obtained by comparing the transition from s_1 to s_2 observed in both encapsulation layers. Our hypothesis, confirmed in simulations, supports a transition of T_{max} from the PCL at low currents towards the heater at higher currents. This is an effect which depends on both the phase-change material electrical resistivity evolution in temperature and the amount of PCL that triggers the melting during the programming operations. Based on such hypothesis, we can consider that the main change between the two regimes, in terms of materials surrounding T_{max}, would be along the x-axis, since along y-axis the encapsulation dielectric remains unchanged. Indeed, when T_{max} is inside the PCL, it is surrounded by the phase-change material itself along x-axis as it is visible in the zx scheme of Fig. 1. In such case the thermal conductivity of the PCL influences s_1. On the contrary, when T_{max} is localized inside the heater, it is surrounded by a SiN based dielectric (referred as "DIEL." in the scheme of Fig. 1) along the x-axis, with an effect on s_2. Such SiN is of the same nature as the one used for the encapsulation (i.e. PECVD) with equivalent thermal conductivity. The ratio between s_1 and s_2 is equivalent in both SiC and SiN devices:

$$\frac{s_{1,SiC}}{s_{2,SiC}} \sim \frac{s_{1,SiN}}{s_{2,SiN}} \sim 2 \tag{9}$$

This confirms the hypothesis of the equivalent origin of the transition between the two slopes in both encapsulation layers, namely the change of position of T_{max} at increasing current. Following our reasoning it would mean that:

$$\frac{s_1}{s_2} = \frac{\sqrt{k_{th,SiN}}}{\sqrt{k_{th,PCL}}} \sim 2 \quad \rightarrow \quad k_{th,PCL} \sim 0.37\ W/mK \tag{10}$$

This result is in agreement with previous works reporting the thermal conductivity of fcc GeSbTe alloys [18, 19]. Considering the heterogeneity of GGST layer after BEOL process, facing phases segregation (i.e. formation of fcc GeSbTe phase and Ge phase) as reported in [13, 17], the thermal conductivity value found in our calculation is in agreement with the presence of grain boundaries and residual amorphous regions in the PCL, outside the active volume. Moreover, being the thermal conductivity of crystalline Ge higher than fcc GeSbTe, the thermal transport in the GGST system should be driven by the GeSbTe phase segregated.

This last result highlights the high importance of the engineering of the dielectrics surrounding the heater element in a Wall structure, in order to make the programming operation more efficient. For a given PCL, the encapsulation layer thermal conductivity influences the steepness of s_1 while the thermal conductivity of the dielectrics surrounding the heater influences s_2. Therefore, in a Wall PCM structure featuring a highly resistive heater element, with a T_{max} localized inside the heater at each programming current, the slope s_2 dominates the RI characteristic and the engineering of the dielectrics surrounding the heater becomes fundamental for drastic current reduction.

5. Conclusion

In this work we report the improved electrical performances in Wall based state-of-the-art 4kb PCM arrays thanks to the engineering of the device encapsulation introducing an optimized SiC layer featuring low thermal conductivity. Thanks to a more homogeneous amorphous volume obtained in the PCL, we demonstrate an improved data retention in GGST alloys of more than one hour at 250 °C. Moreover, the programming operation becomes more efficient being the SET to RESET transition steeper due to the improved thermal confinement. The results are supported by 3D electro-thermal simulations and TEM/EDX analyses. Finally, a theoretical model is proposed revealing the correlation between the slopes of the RI characteristics and the thermal conductivities of the materials constituting the device. The model is validated by using the measured thermal conductivities of the dielectrics surrounding the PCL and the heater, and the PCL thermal conductivity available in literature. Finally, we provide a demonstration of the strong impact of the dielectrics thermal conductivities and of the thermal boundaries surrounding the heater element, providing a path towards ultra low power next generation PCM devices.

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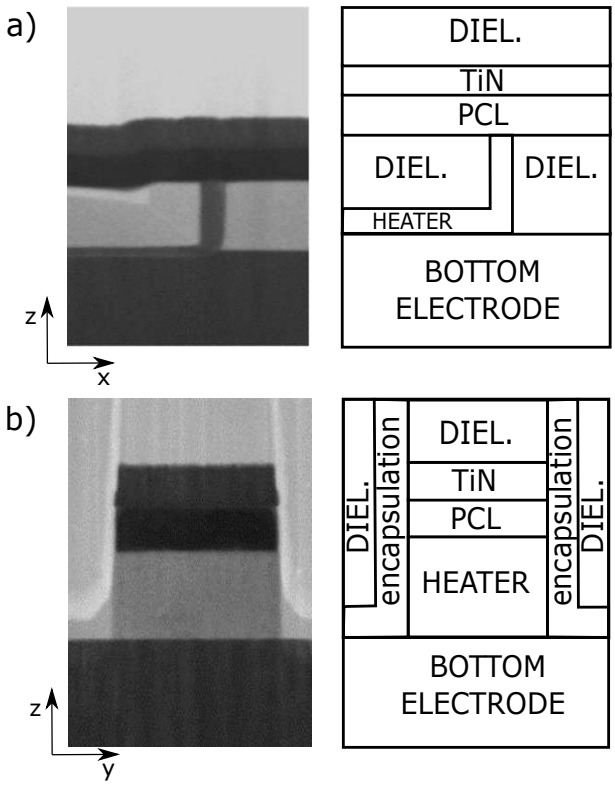

Fig. 1. Simplified description of our heater based PCM device. TEM images performed on the zx (a) and zy (b) planes on a PCM device with a nominal heater width of 300 nm are reported along with the structure description. The encapsulation layer (SiN or SiC), the heater, the phase-change layer (PCL) and the and dielectrics (DIEL.) are evidenced.

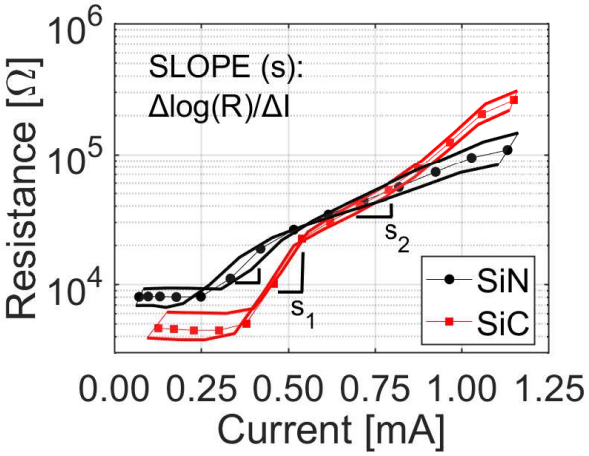

Fig. 2. Resistance as a function of the programming current (RI) for 4kb PCM arrays based on GGST alloy with respectively SiN and SiC as encapsulation layers. The slopes s_1 and s_2 are calculated as $\partial ln(R)/dI$ for both devices and reported in **Table 1**.

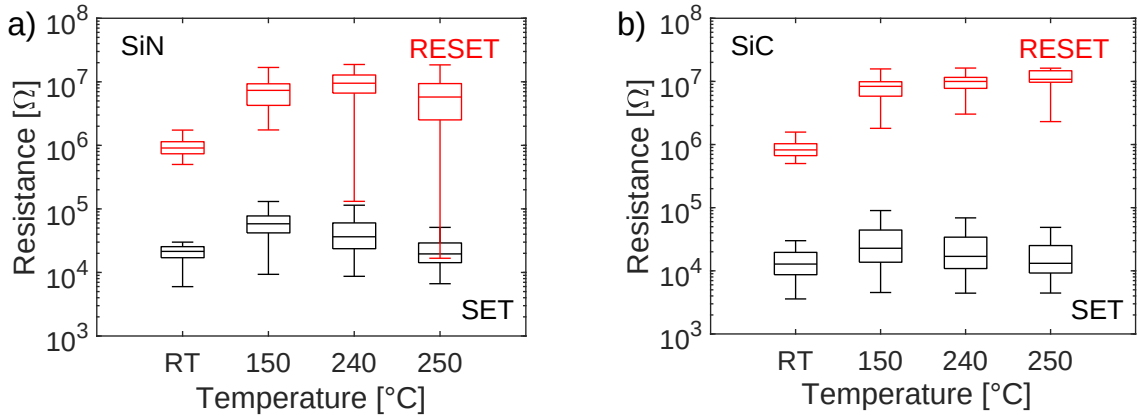

Fig. 3. SET and RESET data retention performed by isochronal annealing of one hour at increasing temperatures for both SiN (a) and SiC (b) where the minimum resistance value in the box represents the first quantile, while the bar covers the whole range of data measured. About the 25% of SiN based devices face a RESET failure at 250 °C while SiC ones retain RESET up to more than one hour at the same temperature. The SET resistance faces a resistance drift for both SiC and SiN up to 150 °C, compatibly with previous works [15], followed by a crystallization.

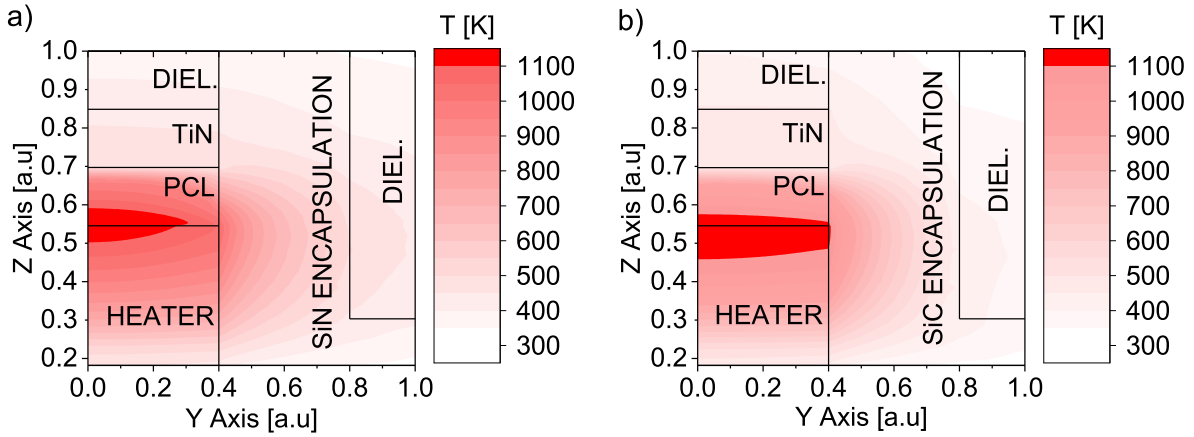

Fig. 4. Temperature profile simulated for both SiN (a) and SiC (b) for same applied current. The SiC device presents a more uniform temperature profile along the y-direction and a temperature gradient oriented along the z-axis.

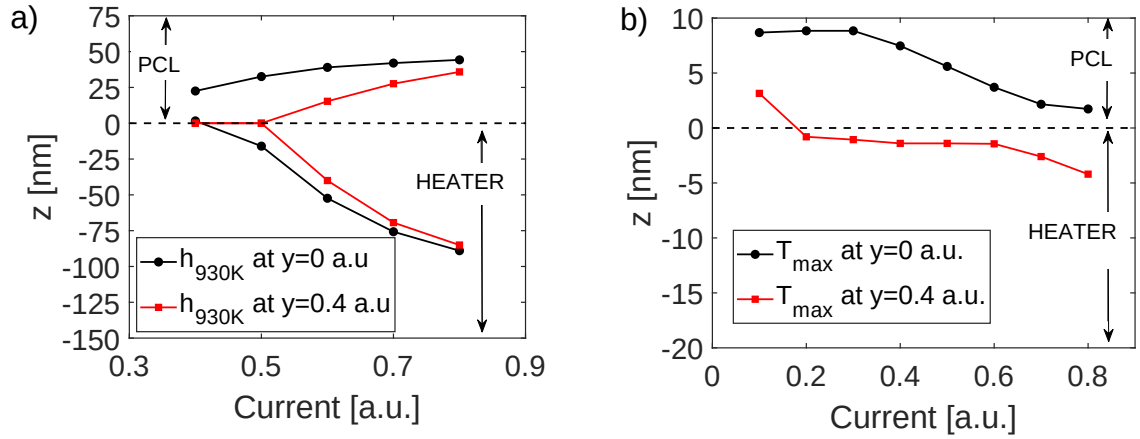

Fig. 5. Evolution of the melted region thickness h_{930K} (a) and of the maximum temperature T_{max} (b) achieved at the center of the cell (y = 0 a.u.) and at the PCL/encapsulation interface (y = 0.4 a.u.) as a function of the applied current in SiN devices. The dashed line represents the interface between the heater and the PCL.

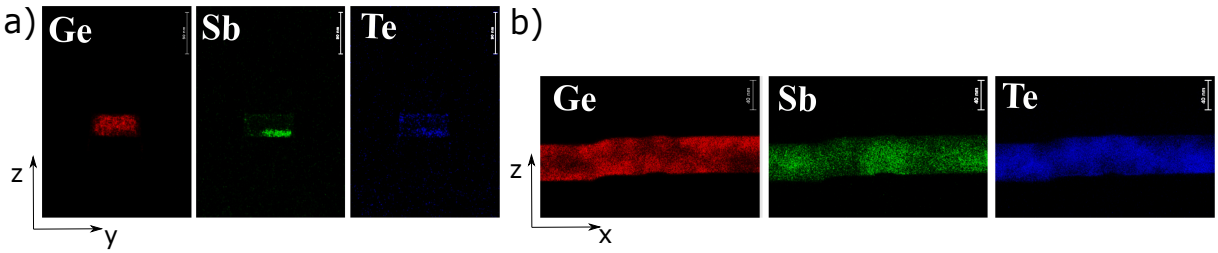

Fig. 6. TEM/EDX analyses performed on SiN encapsulated PCM programmed in RESET state. The elemental maps represent the distribution in the PCL of the three elements: Ge, Sb, Te in both zy (a) and zx (b) plane. The non uniformity of the programming in SiN devices is evidenced in particular in the zy plane analysis, where elements are not uniformly distributed over the heater/PCL interface.

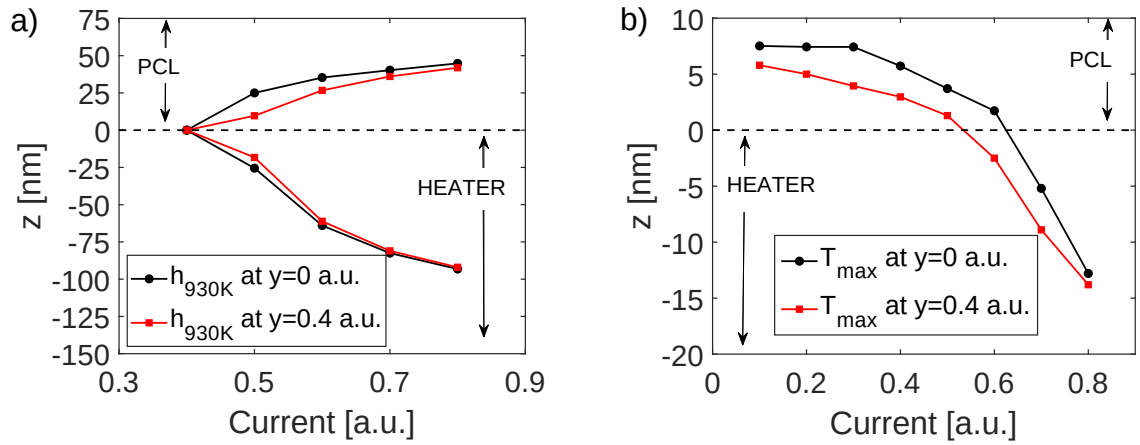

Fig. 7. Evolution of the melted region thickness h_{930K} (a) and of the maximum temperature T_{max} (b) achieved at the center of the cell (y = 0 a.u.) and at the PCL/encapsulation interface (y = 0.4 a.u.) as a function of the applied current in SiC devices. The dashed line represents the interface between the heater and the PCL.

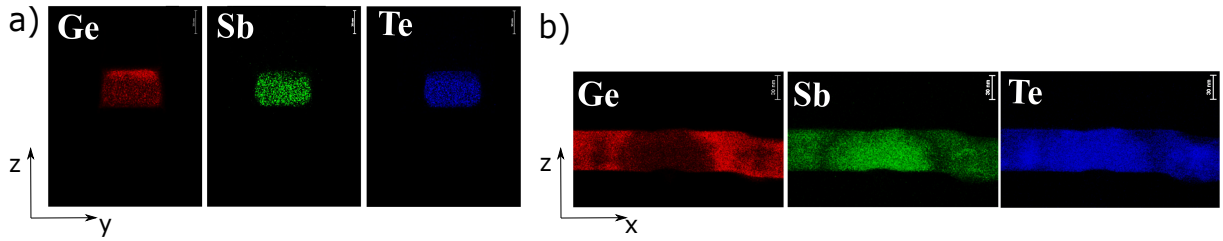

Fig. 8. TEM/EDX analyses performed on SiC encapsulated PCM programmed in RESET state. The elemental maps represent the distribution in the PCL of the three elements: Ge, Sb, Te in both zy (a) and zx (b) plane. A good uniformity of the temperature profile achieved in the device during the programming operation is confirmed in both planes analyses.