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Transfer of an ultrathin single crystal silicon film from a Silicon On Insulator to a polymer

Authored by:

L G Michaud[1], E. Azrak[1], C Castan[1], F Fournel[1], F Rieutord[2], S Tardif[2] and P Montméat[1]
1 Univ. Grenoble Alpes, CEA, LETI, 17 Avenue des Martyrs, F-38000 Grenoble, France
2 Univ. Grenoble Alpes, CEA, IRIG, MEM, 17 Avenue des Martyrs, F-38000 Grenoble, France

Abstract

This study reports the manufacturing of Silicon On Polymer (SOP). It describes the transfer of a 200 mm diameter silicon thin film from a silicon on insulator (SOI) substrate to a flexible polymer. The thickness of the single-crystal silicon film was less than 200 nm and the transfer was achieved by bonding the SOI wafer to a temporary silicon carrier with an adhesive polymer. Various parameters of the transfer were investigated: adherence of the stack, temperature of bonding, temporary carrier and Si film thickness. The substrate and the SOI buried oxide were removed by mechanical grinding and chemical etching. The Si thin film was held on a flexible tape and the temporary carrier was dismounted. SOPs consisting of 20 to 205 nm thin Si films on a flexible polymer (230 µm) were successfully obtained. 200 mm diameter full wafers or patterned wafers could be transferred.

Keywords: nanomaterials, single-crystal, silicon, bonding

1. Introduction

Silicon based materials are commonly used in microelectronics and micromechanical systems. Their main advantages are their excellent chemical, mechanical and electronic properties. Progress in integrated circuits has always been driven by efforts to improve performances in terms of operating speed, power consumption and so on. For the past 20 years, many teams have been focusing on the development of circuits on unconventional substrates, namely flexible polymers. Number of applications are foreseen: displays [1-2-3], solar cells [4-5-6], flexible transistors [7-8], radio frequency devices [9], sensors [10] or biosystems [11-12]. Flexible and stretchable electronics otherwise offer linear elastic mechanical responses to large strain deformations, resulting in high performances electronic and optoelectronic devices [13-14]. To that end, materials are usually obtained by engineering geometric patterns of stiff silicon thin films on compliant and soft substrates [15].

The fabrication of a Silicon On Polymer (SOP) structure is a challenging step. The main technological roadblock is that many usual semi-conductor processes, such as chemical or thermal treatments, are not compatible with the organic backbone of polymers, not to mention that highly volatile monomers precursors are usually not welcome in a clean room environment. Nevertheless, various alternatives have been developed to join a silicon (or a semi-conductor) film with a polymer substrate. The targeted thickness for the silicon thin film is less than 500 nm to keep it flexible, while the thickness of the polymer substrate can range from microns to millimeters, depending on its mechanical properties.

One method to manufacture SOP consists in the deposition of amorphous silicon or micro/nano-crystalline silicon films on the polymer surface by Chemical Vapor Deposition (CVD). Heat-resisting polymers such as poly-imide (PI) with a glass transition higher than 350°C are often used, as the deposition temperature of amorphous silicon is typically between room temperature and 250°C. The thickness of the silicon film typically ranges from 50 to 700 nm [16-17-18-19-20-21]. Low-temperature deposition (e.g. room temperature) usually requires an annealing step (20 s at 900 °C in N_2) to obtain a more crystalline silicon film [22].

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As compared with polycrystalline semi-conductors, single-crystal materials offer a high degree of uniformity of structure and thus a better resistivity and their use allows to increase the performances of the circuits. Besides the manufacturing reliability and reproducibility are increased [23]. Several groups have recently highlighted the contribution of single-crystal nano-films of silicon for various devices: transistors [24-25-26-27] as well as synaptic devices [28]. Manufacturing a SOP made of single-crystal silicon cannot be achieved by growing the Si film on the flexible substrate. One can actually bond an existing Si film to the polymer. In order to transfer films of sub-micron thickness, the fabrication starts from a Silicon On Insulator (SOI) substrate, with a top single-crystal Si thin film bonded to a SiO_2 buried oxide layer (BOX).

The so-called "stamping" approach consists in first patterning the Si film and partially etching the BOX under the Si patterns with a concentrated HF solution. A piece of polydimethylsiloxane (PDMS) is then brought into conformal contact with the top surface of the wafer and carefully peeled off to pick up the Si patterns (stamping). The Si patterns on PDMS can then be transferred again on a polymer foil such as polyethylene terephthalate (PET) or PI. This method has been widely studied by the J.A. Rogers' group to obtain Si stretchable and bendable Si ribbons of a thickness from 20 to 300 nm [29 -30 -31 -32]. Other crystalline SOP from 200 nm [33-34-35] to 3 µm [36] were obtained through this type of process. Crystalline AsGa [37], SiC [38] or PZT [39] films can also be transferred onto a polymer surface. This approach offers great opportunities to design device structures that exploit mechanical strain to achieve unusual electronic responses. Nevertheless, the stamping step is hardy feasible in an industrial environment and other methods have been proposed to obtain SOP.

Wafer thinning (mechanical grinding, polishing and etching) can be directly performed onto a thick mono crystalline silicon bonded to the polymer substrate. The thickness of the residual Si film is 1 µm [40] to 10 µm [41] and the crystalline film is highly stressed. Spalling [42] can also be used for the separation of a 15 µm thin film from the started wafer. Finally, temporary bonding combined with ion implantation is an outstanding alternative. SOP structures thinner than 500 nm can be manufactured [43-44].

In our previous work [45], we have demonstrated that transferring a 200 nm thick single-crystal film onto a flexible polymer was feasible. The SOP structure was used for tensile strain experiments. The present paper follows this first work and the objectives of here is to fully describe, characterize and optimize a process for transferring a single-crystal silicon film considerably thinner than 200 nm thick onto various polymers. The process used to fabricate a SOP is implemented on 200 mm wafers in a clean room environment and based on temporary bonding combined with various thinning methods. Full 200 mm or patterned Si films are transferred onto a flexible polymer substrate. We can emphasize the novelty of this work because first, to our knowledge, no manufacturing process of SOP in a clean room environment and on industrial tools has ever been described. Secondly the process is polyvalent, it can be performed for full 200 mm wafers or for a patterned wafers for a large scale of silicon thicknesses. At least the crystalline properties of the silicon thin film is also maintained all along the process. All of this opens up new directions for flexible electronics or circuits.
The process and the associated characterizations are presented in the first part of the paper. In the second part, many improvements and alternatives of the process are described, with a focus on limitations in terms of silicon thickness.

2. Experimental

2.1. Process

The full process for the transfer of a silicon ultra-thin film onto a polymer is based on temporary wafer bonding. As shown schematically in figure 1, 9 steps are involved.

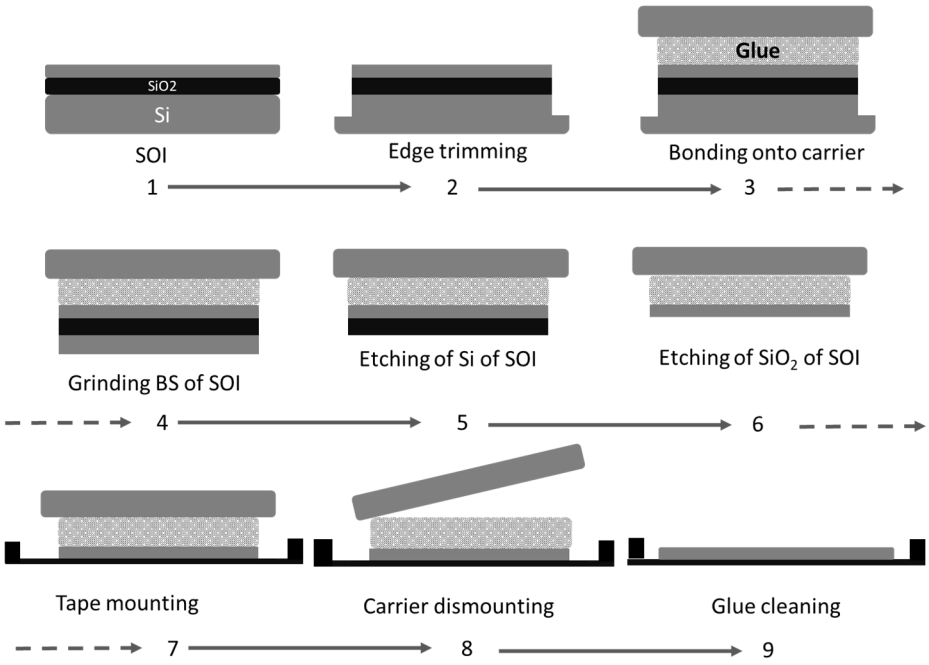


Figure 1: transfer process

A 200 mm SOI Unibond™ wafer made of a 205 nm thick [100] silicon film over a 400 nm thick buried oxide layer was first edge trimmed (width=1.5 mm, depth= 280 µm) on a DISCO dicing tool prior to bonding. Particles were removed from the surface of the trimmed wafer by megasonic cleaning with isopropanol (step 2).

The SOI was then bonded to a temporary carrier (Si wafer) with, on top, a 40 µm thick polyolefin-based temporary adhesive (Glue BrewerBOND® 305). The temporary carrier was made of a silicon wafer coated with a monolayer of a fluorinated polymer (3M Novec EGC 2702) cured at 150 °C under air for 30 min. The bonding process of step 3 was performed from 150°C up to 275°C under vacuum in an EVG520 bonder. The back-side silicon substrate of the SOI was fully removed during steps 4 to 6. A coarse grinding down to 200 µm was first performed, followed by a fine grinding down to 50 µm, on an Okamoto tool. The remainder of the Si substrate was removed by anisotropic wet chemical etching in a SEZ 203 etching tool, using the buried oxide as an etch-stop layer. The dismounting of the carrier was completed through a chemical etching of the oxide in diluted HF (50% in water). The thinned stack was then mounted onto a dicing tape (230 µm thick acrylic and polyolefin-based polymer FURUKAWA SP537T-230) held on a DISCO metallic frame (step 7). An automatic laminator was used for the frame mounting. During step 8, the temporary carrier was mechanically removed at room temperature. The mounting on frame and the dismounting of the carrier were all performed automatically in an EVG850DB tool. The last step 9 consisted in the removing of the glue by a chemical cleaning with D-Limonene.

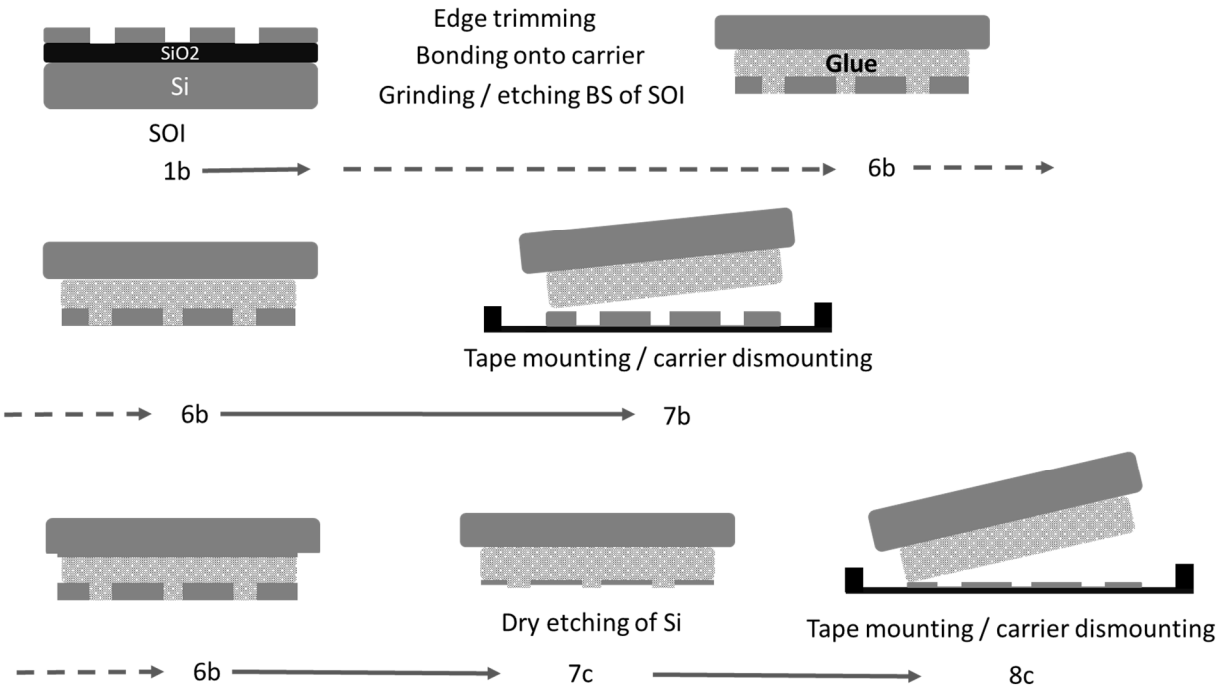


Figure 2: alternative process

Alternative processes were also tested (Figure 2). They mainly consisted in using photolithography to fabricate silicon patterns for transferring 2 X 24 mm² ribbons or disks with 20 mm diameters. In that case, the fluorinated polymer was coated on the patterned SOI, leading to the simultaneous dismounting of the carrier and the glue (step 7b). A 1X photolithography with a JSR 420 resist was used. Various thicknesses of Si were also tested: from 20 to 205 nm. The tailoring of the Si thickness of the SOI substrates was then based on an oxidation at 950°C (VT412) followed by a wet etching in HF (SEZ 203) of the thermal oxide thus formed.

Another alternative consisted in reducing the Si thickness when the Si thin film was already transferred onto the glue and the temporary carrier (step 7c). In that case, a dry etching in a P500E tool was performed (C_2F_4 plasma).

2.2. Characterizations

The adherence energy of the bonded stack with and without a fluorinated layer was obtained by the double cantilever beam (DCB) technique proposed by Maszara [46]. It consists of a blade insertion in the silicon bonded structure and an infra-red measurement of the debonding length. The El-Zein[47] formula was used to calculate the adherence energy. The defectivities of the various structures were evaluated by optical inspection with a KLA Surfscan SP2 wafer level defect and surface quality inspection system. The water angle of the fluorinated surface was measured with a drop shape analyzer Kruss DSA100. The thickness of the silicon thin film was evaluated using ellipsometry (Nanometrics and Woollam) and X-ray reflectivity XRR (JVX5200). High Resolution X-ray Diffraction (HRXRD) measurements were also performed using a Bruker D8 diffractometer with a copper anode ($\lambda_{K\alpha}$ = 1.54056 Å). ω-2θ scans around the (004) Silicon Bragg peak gave us access to its full-width at half-maximum (FWHM) and to thickness fringes. In the case of the silicon thin film on SOI, the silicon thickness was evaluated by ellipsometry on 9 different points for a wafer. In the case of a silicon thin film on SOP, the silicon thickness was evaluated by ellipsometry, XRR and HRXRD on 13 different points for a wafer.

Scanning acoustic microscopy (SAMauto PVA TEPLA, 140 MHz acoustic head frequency) was used to control the bonding interface quality after bonding and grinding. The total thickness variation (TTV) values of the Si thinned substrate and of the full stack (Si carrier / glue / Si 50 µm) were obtained with an optical measurement in a FRT Microprof tool (mean of two 200 mm diameter profiles after grinding).

Finally, a Raman spectrometer (Horiba LabRam HR, 632.81 nm laser, 17mW) was used to measure the FWHM and shift of the 520 cm^{-1} silicon peak. A bulk silicon sample was used as a reference and peaks were fitted using a python routine. The biaxial strain ϵ_{xx} can be obtained using equation (4) with the Raman peak shift $\Delta\omega$ and the strain shift coefficient b_{biax} [48-49]. The biaxial stress is expressed in equation (5) using Hooke's law and silicon biaxial Young modulus $B_{100} = 180\ GPa$ [50]. The laser power was limited to 10% of its nominal value to avoid thermal stress [51].

$$\Delta\omega = b_{biax}\epsilon_{xx} = -723\epsilon_{xx} \quad (4)$$

$$\sigma_{biax} = \frac{\Delta\omega}{b_{biax}} B_{100} \quad (5)$$

3. Results and discussion

3.1. Determination of the bonding parameters

One of the key parameters of temporary bonding is the adherence of the stack. The adherence of the Brewer 305 adhesive with the silicon surface is evaluated around 2 J/m². We have already shown [52] that a suitable adherence was less than 1 J/m² and that a fluorinated polymer (3M EGC 2702) could be used to control the adherence between a silicon surface and an adhesive [53]. The temporary carrier was thus prepared by coating a mono layer of 3M EGC 2702 onto a silicon wafer. The water angle of the coating after curing of the film was stable around 105°. The coating was thus highly hydrophobic, at variance with the starting silicon wafer with its native oxide, which was highly hydrophilic (water angle less than 5°, then).

This carrier was bonded onto a silicon wafer coated with 40 µm of Brewer 305-30 adhesive. In order to investigate the impact of temperature on the adherence, several bonding temperatures ranging from 150 to 275°C were tested (figure 3). All the adherences were close to 0.2 J/m², a value ten times lower than the Si/glue adherence of 2 J/m², confirming the antisticking behavior of the fluorinated polymer. This adherence of less than 1 J/m² is also supposed to be suitable for a temporary bonding process. No significant impact of temperature was noticed: the fluorinated polymer acted as an adhesion barrier between the adhesive and the silicon surface.

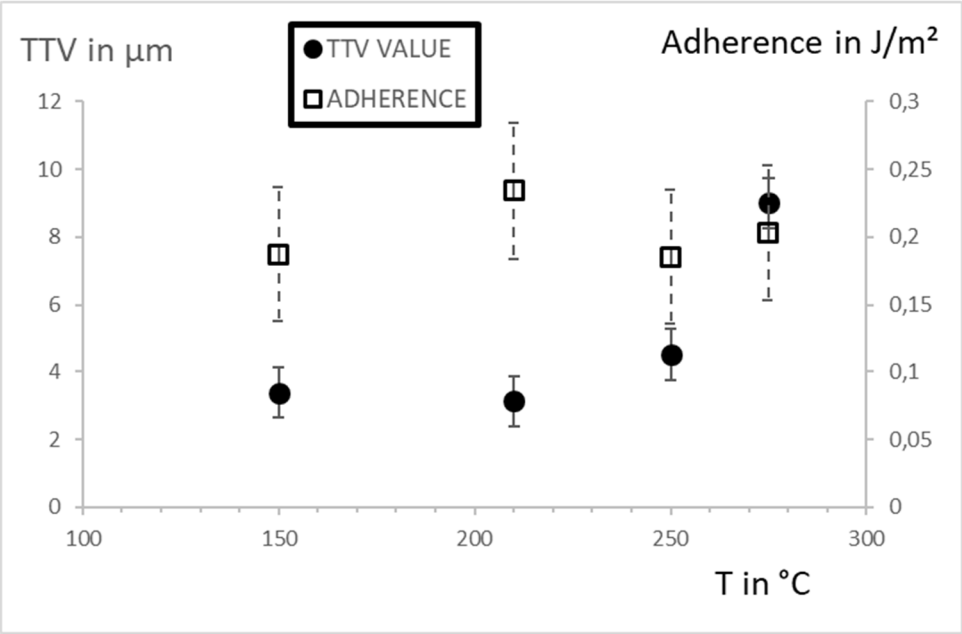


Figure 3: impact of the bonding temperature on the adherence of the structures and on the TTV value after backside grinding

The silicon backside of each stack was then thinned down to 50 µm. Figure 3 shows the evolution of the TTV value of the thinned silicon wafer with the bonding temperature. The best values of 3 µm were obtained for the lowest temperatures (210 and 150°C) while 275°C resulted in the largest and worst TTV value, 9 µm.

Each structure was successfully dismounted and the 50 µm silicon film was transferred onto a dicing tape. After the separation, the water angle of the carrier wafer was still 105°, indicating that the fluorinated layer withstood the complete temporary bonding processes. The temporary carrier can thus be reused for further processes, which is a boon.

For the next bonding processes, we decided to use 210°C as the reference bonding temperature since it yielded the best TTV value and a suitable adherence for grinding and dismounting.

3.2. Transfer of the SOI 205 nm thin film

3.2.A. bonding and grinding

The thickness of the starting SOI substrates was measured for 10 wafers of the same batch. 49 points polar maps yielded top Si thickness of 206 ± 11 nm and buried oxide thickness of 403 ± 2 nm.

The edge trimming of the SOI wafer resulted in a significant particular contamination of the surface: 1300 defects were observed with a threshold detection of 500 nm. As shown in supplementary ESI 1, a megasonic cleaning of the surface reduced the particular contamination level to about 300 (with the same threshold of 500 nm).

An acoustic microscopy picture after the bonding of the trimmed SOI with the carrier is provided in figure 4a. No voids are observed. Nevertheless two singular areas exhibit a pale color representative

of the stronger force/pressure of the two clamps that prevent the wafer from moving during the bonding process. The thickness of the glue is smaller in those locations.

The grinding of the back side of the SOI was done in two steps, first down to 200 µm, then to 50 µm. Acoustic microscopy pictures of the various stacks are shown in figures 2b and 2c. No defects are observed. The clamps areas are once again visible, without cracks or delaminations in those regions, however.

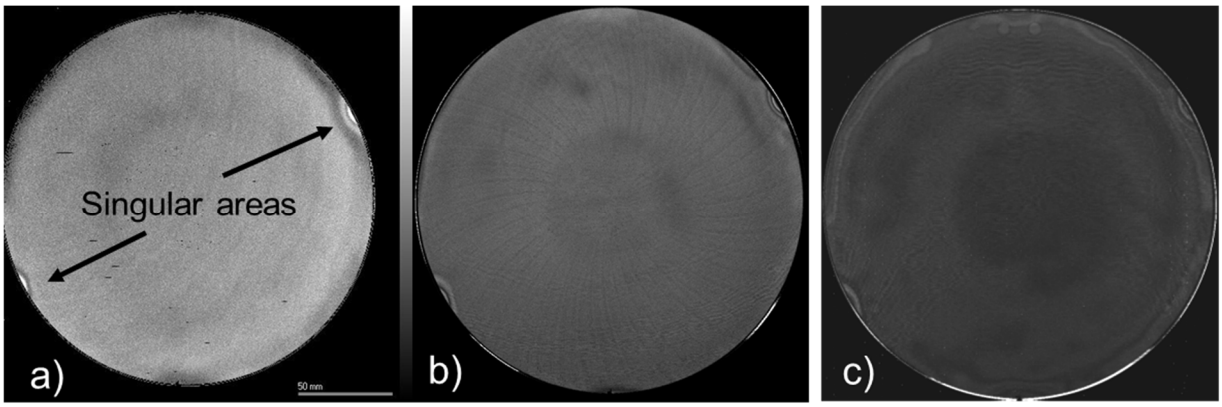


Figure 4: 200 mm acoustic microscopy pictures of the bonded stack (a), stack coarse-grinded to 200 µm (b) and stack fine-grinded to 50 µm (c)

The edge region was very fragile during the coarse grinding to 200 µm. A significant fraction of the wafers exhibited defects in those regions: around 20 % for a batch of 10 wafers. As shown in figure 5b, delamination then happened at the borders of the thinned wafer. In that case, the stack did not withstand the grinding process down to 50 µm and a partial splitting of the thinned wafer occurred (see supplementary ESI 2). Nevertheless, an annealing at 200°C for 30 min at 1 bar suppressed the delamination. The stack then withstood grinding down to 50 µm without any damage (see figures 5c and 5d).

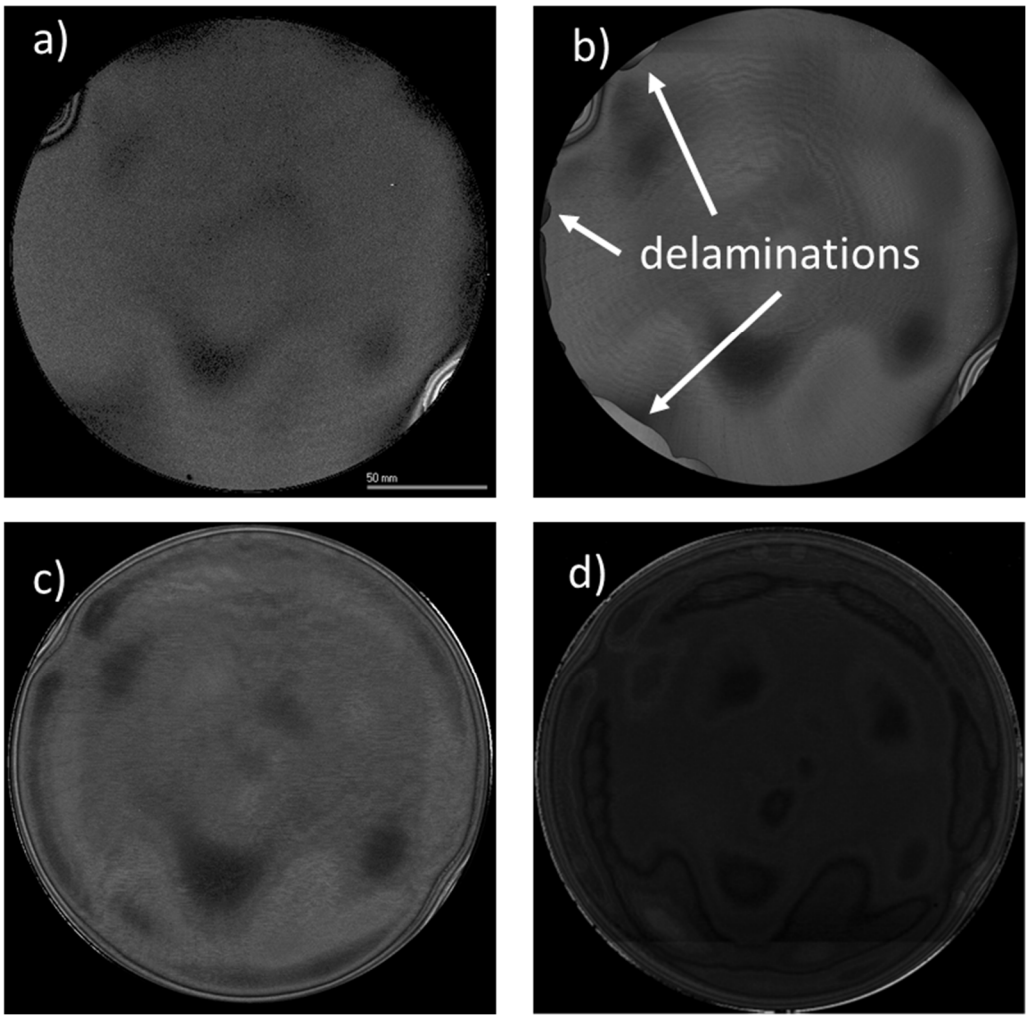
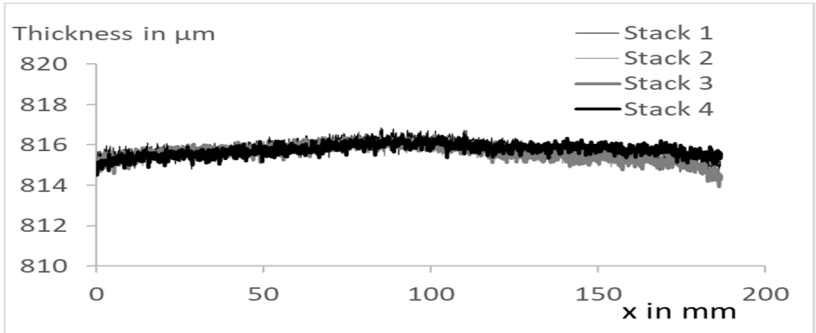


Figure 5: 200 mm acoustic microscopy pictures of the bonded stack (a), a stack coarse-grinded to 200 µm before (b) and after (c) delamination curing and a stack fine-grinded to 50 µm (d)

After grinding down to 50 µm, the profiles of the complete thinned stack (Si carrier / glue / thinned wafer) and the single thinned wafer are provided in figure 6. Profiles are very flat, with TTV values less than 2 µm. The TTV values of the thinned-down wafers only are larger: 4 ±0.2 µm. An edge exclusion of 5 mm yields ~ 2 µm TTV values, showing that the larger thickness variations are mainly due, for the thinned wafers, to edge effects. The TTV value of the thinned wafer is governed by the bonding process used, as shown in previous studies [54]. Here, the most favorable value is for the wet etching, in the following, of the residual 50 µm thick Si wafer.



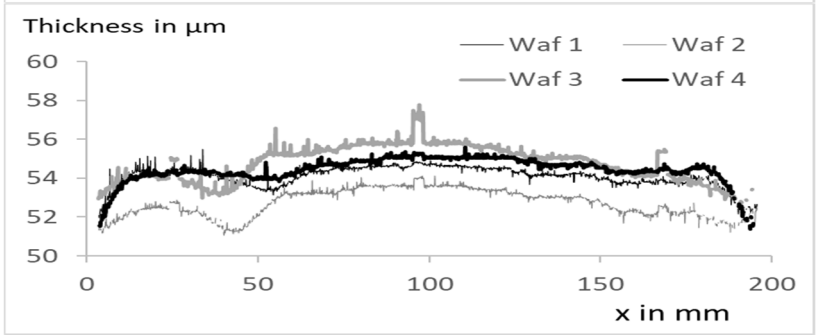


Figure 6: 200 mm profiles of the thinned stacks, top: Si carrier 725 µm / Glue 40 µm / Si 50 µm, bottom: Si 50 µm

3.2.B. Wet etching

The removals of the remaining 50 µm of silicon and the 400 nm of SiO_2 were performed by wet etching. The resulting stack is provided in figure 6a. We obtained a SOP, with 205 nm of Si attached to a 40 µm thick polymer film.

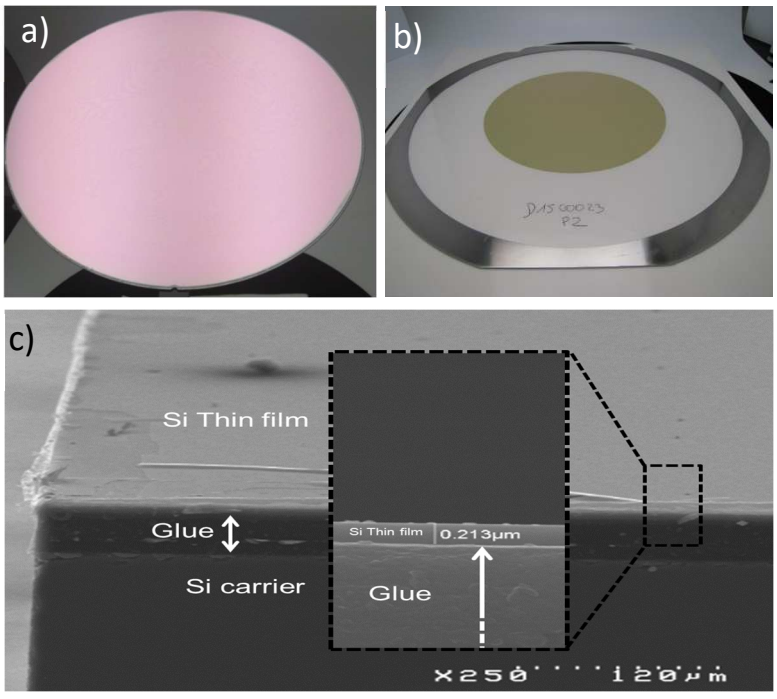


Figure 6: Snapshots of the Si thin film attached to the temporary carrier (a) and attached to the frame after the dismounting of the temporary carrier (b). Cross-sectional scanning electron microscopy picture of the Si thin film onto the carrier (c)

The defectivity of the Si thin film was evaluated. Results are shown in figure 7. 180 defects (with a size larger than 1 µm) were observed: most of them were particles or small scratches (see supplementary ESI 3).

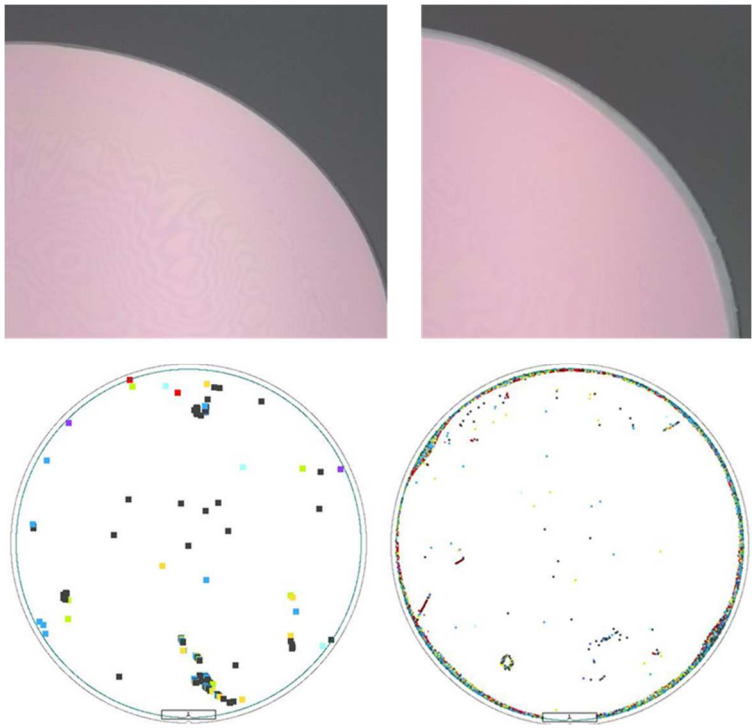


Figure 7: Snapshots and defectivity analysis (threshold of 1 µm) for a 205 nm Si thin film transferred without delamination after grinding (left) and with delaminations (right) after grinding (200 mm diameter wafers).

The overall quality of the thin silicon film is very good. The thickness of the Si thin film was evaluated by spectroscopic ellispometry for 10 wafers of the same manufacturing batch. 9 points were measured on each wafer. The thickness was 198 ± 5 nm, which was consistent with the initial thickness of the SOI wafers (206 ± 11 nm). The cross sectional Scanning Electron Microscopy image provided in figure 6c also confirms the thickness of the Si film.

Defectivity analysis was performed onto a stack previously cured to remove delaminations induced by the grinding process. In that case, the number of defects observed after the etching was much larger with about 3300 defects. The majority of the defect were located at the wafer edges (3000

defects) and the other were located on the central part of the wafer (around 300 defects). The central part of the wafer was thus similar to the central part of the wafer from the standard process without any thermal treatment post grinding. Snapshots of both types of wafers (figure 7) indicate that the silicon thin film is not present on the border of the cured wafer (exclusion of 5 mm) whereas the silicon covers the full surface for the standard process. The lack of silicon on the border explains the large number of defects. This over etch is consistent with a penetration of the silicon etching solution through delaminated area of the stack. The thermal treatment post grinding has not completely removed delamination, in opposition to what was be expected contrary to what seem the acoustic microscopic picture in figure 5c)

Figure 8a shows an omega-2theta scan around the (004) Si bragg peak for SOP held by a rigid carrier. For this characterization, a dry etching of the silicon was performed beforehand to reduce the thickness to around 100 nm. Thickness fringes are clearly visible and the FWHM of the peak is 179.6 +/- 3.9 arcsec, indicating a good quality crystalline structure [55]. Dynamical scattering theory modeling of the omega-2theta scan resulted in a silicon thickness of 92.8 ± 2.5 nm. Spectroscopic ellipsometry and X-ray Reflectivity (XRR) were performed, giving silicon thicknesses of 93.6 ± 2.8 nm and 98.2 ± 2.8 nm, respectively. Non-crystalline or tilted silicon layers will not contribute to HRXRD, in opposition to XRR and ellipsometry. The small thickness differences between the three methods likely indicate that a few nanometer of silicon have been damaged by the plasma etching, with most of the Si layer remaining fully single crystalline during the transfer process.

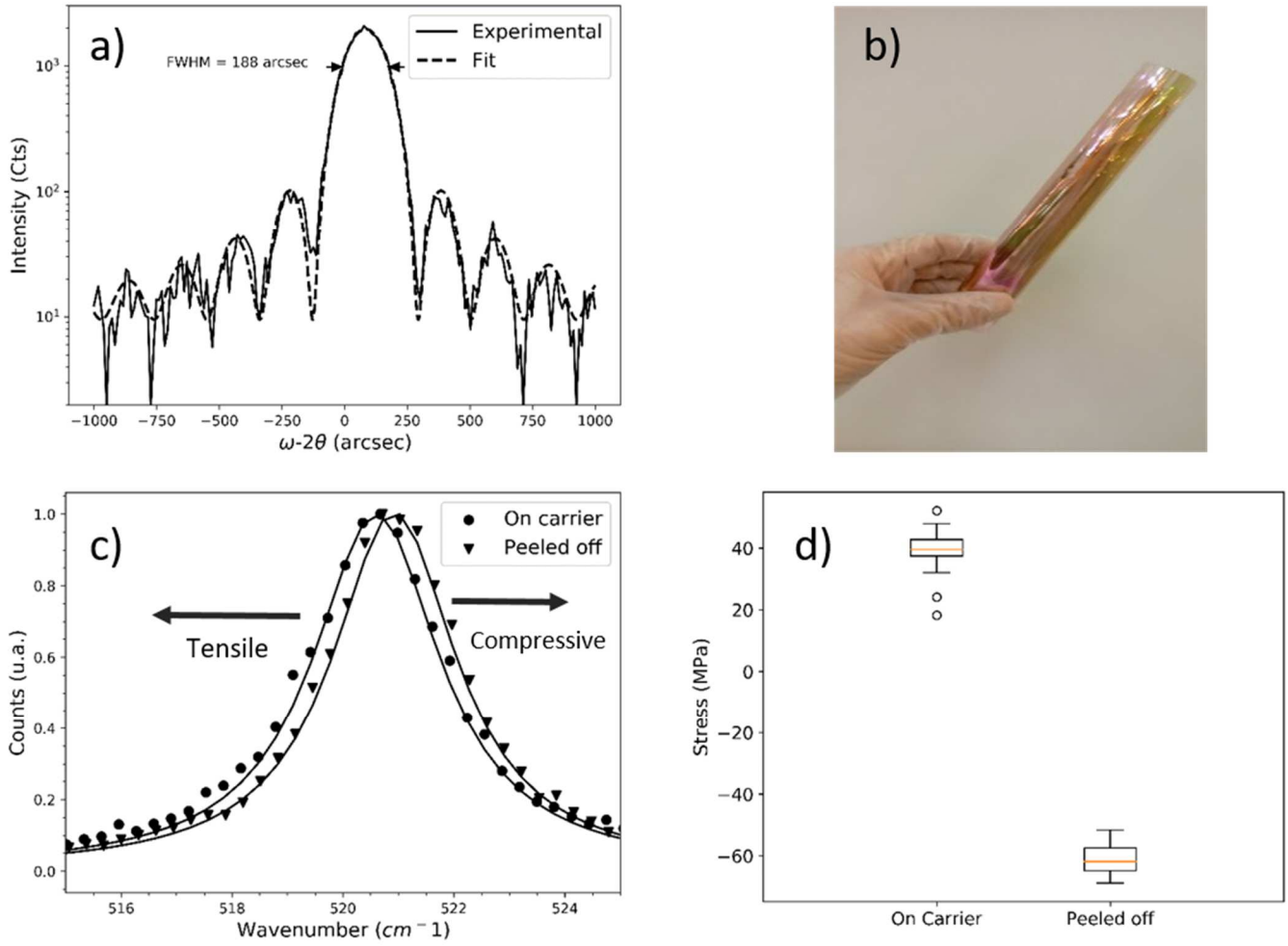


Figure 8: Omega-2theta scan around the (004) Si bragg peak for the SOP on the rigid carrier (a), snapshot of a SOP cylinder after a peeling from the carrier: the Si is on the external side of the cylinder (b), Raman spectrum of a 205 nm SOP before and after a peeling from the rigid carrier (c), Corresponding biaxial stress value in the (001) plane for a 500x500µm² surface (d)

Raman spectroscopy yielded a FWHM of 2.70 +/- 0.06 cm-1 for the silicon peak at 520.54 cm^{-1} on a 500 x 500 µm² area with 16 data points. Such a result is consistent with the 2.76 cm^{-1} FWHM of the 520.70 cm^{-1} peak of a bulk single crystal Si reference sample. Similar values are given in the literature [56] and confirms once again the good crystalline quality structure. Furthermore, the Raman peak FWHM remains constant under uniaxial tensile stress [57].

One option for the separation of the carrier is to peel the glue and Si film from the rigid carrier. In that case, a very flexible SOP is obtained: 205 nm of silicon onto 40 µm of polymer. As shown in figure 8b, we obtain a cylinder shape where the Si is on the external side of the cylinder. Stress measurement of a 205 nm thick SOP film, before and after being peeled off, are provided in figure 8d as well as Raman spectra acquired on the top silicon layer in figure 8c. When held by the carrier, the silicon presents a positive, i.e. tensile stress of 38.6 MPa. Note that the omega-2theta scan shown in figure 8a also provides an estimation of the in-plane biaxial stress for the SOP film: 75.1± 33.7 MPa. There a significant dispersion but the value of the tensile stress is consistent with Raman measurements. After being peeled, the silicon attached to the polymer presents a negative, i.e., compressive stress of 61.2 MPa. The bonding was performed at 210°C as described in 3.2.A. A thermal expansion mismatch between the silicon substrate ($2.6x10^{-6}$ $°C^{-1}$) and the glue (8×10^{-5} $°C^{-1}$) induced a thermal stress when the structure was cooled down under the glass-transition temperature of the polymer (90°C) down to 20°C. Compressive values have already been reported in the literature for SOP structure [58 59].

3.2.C. Transfer onto the tape

After mounting the stack onto a metallic frame with the tape, the dismounting of the temporary carrier was performed very easily, which was expected given the weak energy of the stack (0.2 J/m²). The water angle of the removed carrier was 103°, i.e. very close to the initial value of 105°, showing the ability of the fluorinated polymer to withstand the grinding and wet etching of the full transfer. Moreover, the carrier was reusable for further transfers. The Si thin was sandwiched between two polymers: the glue (40 µm) and the dicing tape (230 µm). The snapshot of the resulting SOP held on a frame is shown in figure 6b. No significant cracks are observed. The transfer of a 205 nm thick Si film from a 200 mm SOI to a 200 mm SOP is thus successful, validating our process flow with a temporary carrier.

D-Limonene was used for the temporary glue stripping from the surface of the Si thin film. The resulting structure (Si 205 nm on the 230 µm of the tape) presents wrinkles as shown in figure 9b. A stretching of the tape strongly reduced this waviness. The buckling of a silicon thin film on a soft substrate is well documented (see review [60]). Buckling induces wrinkles through mechanical strain mismatch [61-62], thermal strain mismatch [63-64] or other methods such as surface treatments [65-66]. In our structure, the lamination of the tape onto the Si thin film induces a significant compressive strain. The release of the strain in the tape results in a wrinkling of the Si thin film.

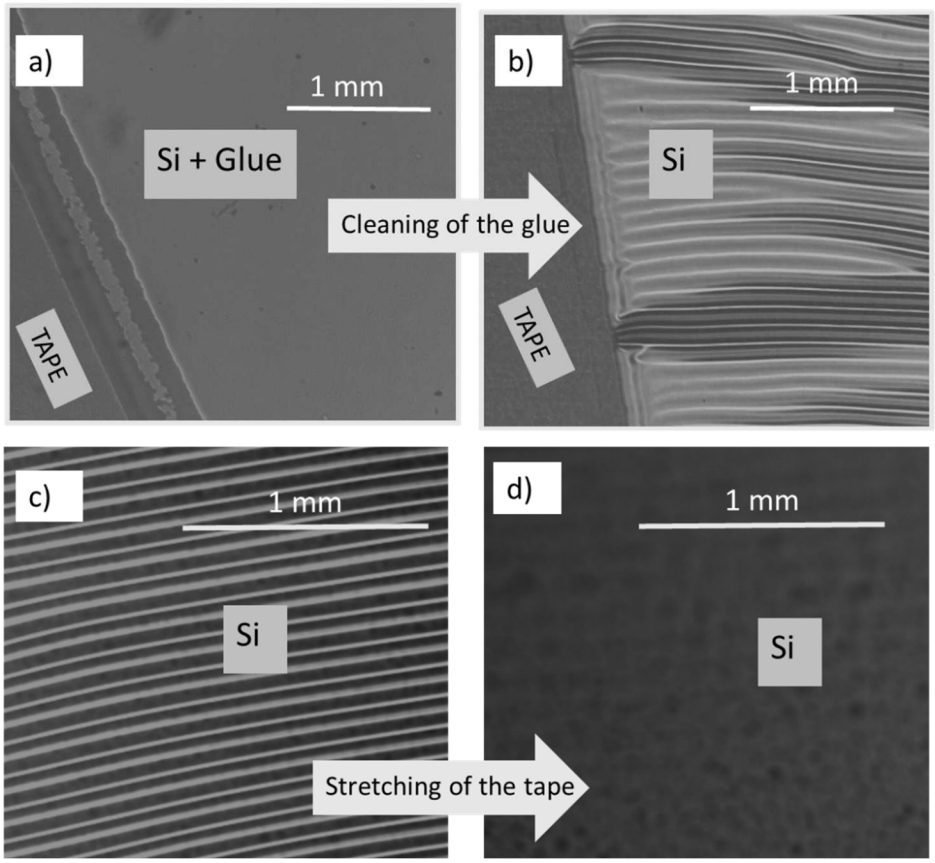


Figure 9: Microscopy pictures of the 205 nm Si film transferred onto the 230 µm tape with glue (40 µm) on top (a), after a stripping of the glue (b) and (c), and after the stretching of the tape (d).

3.2. Alternative processes

3.2.A. Location of the fluorinated layer: on the carrier

3.2.A.1. Simplification of the process

In order to simplify the flow, two simplifications were evaluated:

- Suppression of the cleaning of the trimmed wafer before bonding
- Suppression of the trimming prior to bonding

The removal of the cleaning had no impact on the quality of the transfer. We assume that the adhesive polymer encapsulated the particles generated by the trimming.

Without any trimming, the edge of the thinned wafer was very fragile and the grinding process often resulting in border defects. Without trimming, around 50 % of the wafers exhibited defects for a batch of 10 wafers whereas a trimming process led to only 20% of defects. The trimming is thus mandatory for a safe and reliable SOP fabrication process.

3.2.A.2. Transfer of thinner 200 mm silicon films

SOI wafers with various thicknesses of silicon were fabricated. Supplementary ES4 details the properties of the Si thin films: besides 205 nm thick films, 20, 60, 100 and 150 nm films were

fabricated. The transfer of thinner Si films (150 to 60 nm) was also satisfactory. Nevertheless, when the thickness of the silicon film decreased, the SOP defectivity increased (threshold size: 1 µm). While the number of defects was 500 for a 205 nm thick film, it reached 2000 defects for a 60 nm thin film. Some defects are shown in figure 10. A particle led to a large crack for the 60 nm thick film, whereas there were no cracks for a 205 nm thick film. An intermediate size is observed for the 100 nm thin film. Snapshots of various Si films attached to temporary carriers after the chemical etching are provided in ESI 5.

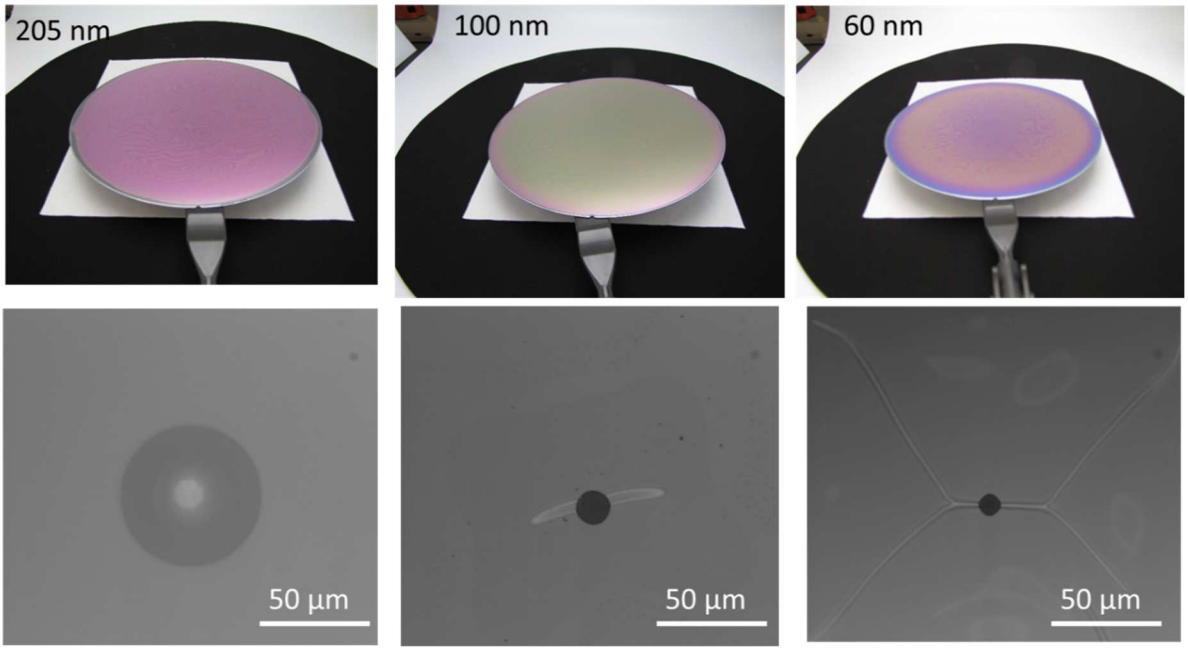


Figure 10: Snapshots of 200 mm diameter Si films attached to their temporary carriers (top) and top-view scanning electron microscopy pictures of defects (bottom) for 205 nm (left), 100 nm (center) and 60 nm (right) thick starting Si films.

3.2.B. Location of the fluorinated layer: on the SOI

The location of the fluorinated layer drives the dismounting process. An option consists in coating this layer on the top of the SOI thin film prior to bonding. As shown schematically in figure 2, after dismounting, the Si thin film was bonded onto the tape without any glue on top, then (only the monolayer of fluorinated polymer is still present). An aggressive stripping of the glue is not necessary to obtain the silicon film on tape, then.

3.2.B.1. Transfer of patterns with various thicknesses

Such a process was used with a patterned SOI to transfer 2 X 24 mm² ribbons or disks with 20 mm diameters. The silicon thicknesses were 20, 50, 100 and 205 nm, then. Bonding and grinding for the transfer were satisfactory. Figure 11 provides microscopy pictures of the silicon rectangles for various thicknesses after the chemical etching. No cracks are observed for the 205 and 100 nm thick Si films. Large and numerous cracks appear for the 50 and 20 nm thick Si films, however. This is mainly due to the buried oxide layer. Indeed, this thermal oxide has a compressive stress of around 300 MPa. The stress can be partially relaxed due to the polymer layer. If the silicon film is too thin, it cannot withstand the relaxation. One solution could be to use SOI wafer with thinner buried oxide layer. It could then be too thin to stop the chemical silicon etching after grinding, however.

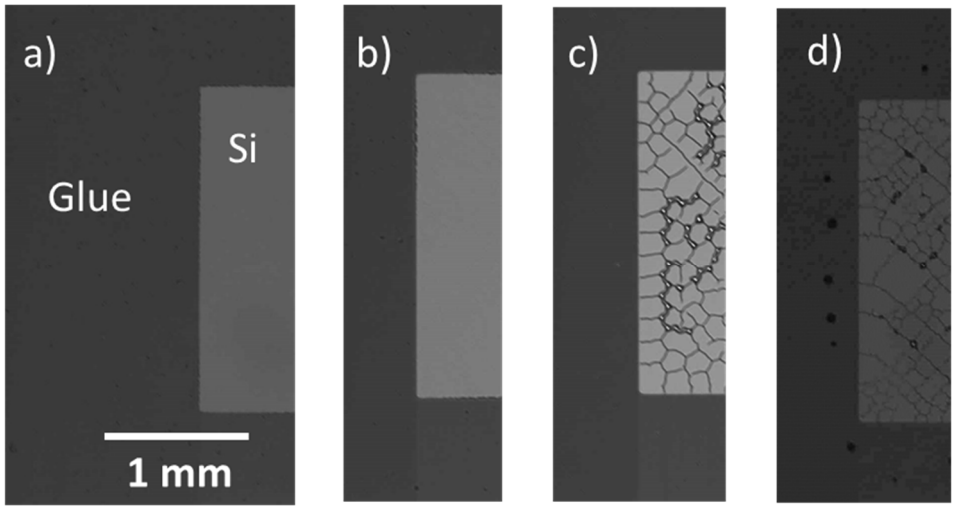


Figure 11: Microscopy pictures of the transfer of patterns in 200 (a), 100 (b), 50 (c) and 20 (d) nm thick Si films on temporary carriers

The transfer onto the tape was performed for the 200 and 100 nm thick films. No cracks were observed. The successful transfer of 100 nm thick silicon patterns onto a polymer is shown in figure 12 e.

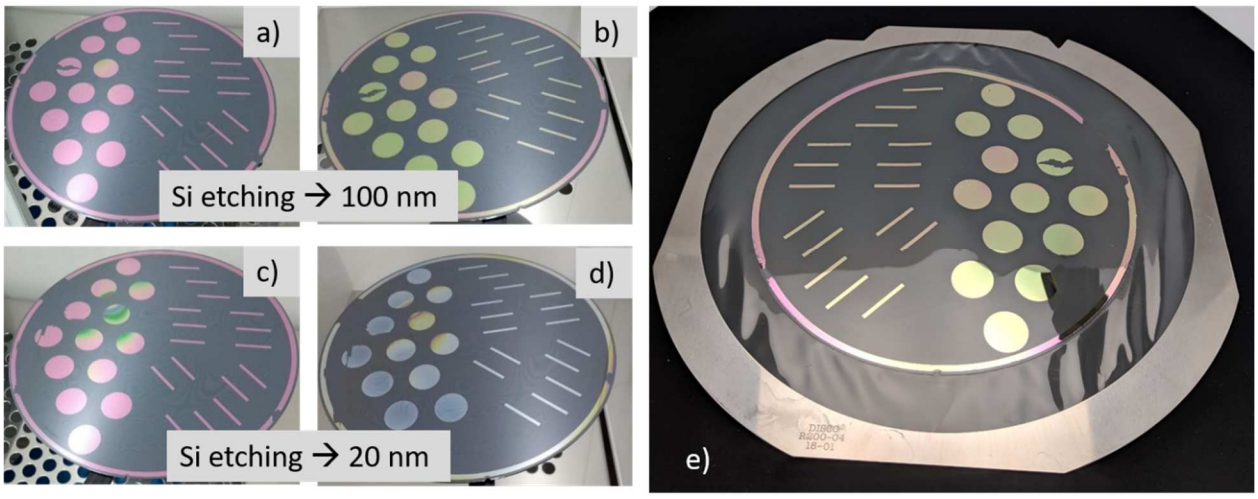


Figure 12: Snapshots of the transfer of patterns in 205 nm thick Si films on carriers prior to (a) and after dry etching of Si to 100 nm (b), prior to (c) and after dry etching of Si to 20 nm (d). Snapshot of 100 nm thick Si patterns on a tape (e).

The location of the fluorinated polymer plays a role on the quality of the transferred Si thin film when attached to the temporary carrier. A 60 nm thin film can be transferred without any cracks when the fluorinated layer is coated on the carrier (part 3.2A.2), whereas the transfer of a 50 nm thin film lead to cracks when the fluorinated layer is coated on the SOI. This behavior is not well understood. We can nevertheless assume that the fluorinated layer on the SOI eases the buried oxide relaxation as the adherence between the top silicon film and the glue is definitely weaker, then.

3.2.B.2. Transfer of patterns and dry etching

Another possibility to reduce the thickness of the Si film was to used dry etching. Dry etching was performed when the 205 nm thick film was still attached to the temporary carrier and free of cracks. Pictures of the wafers after dry etching down to 100 and 20 nm are shown in figures 12a to 12d. The

etching did not alter the quality of the initial 205 nm patterns, as no additional cracks appeared for 100 nm or 20 nm. The final thickness of the Si films were very close to the targets, 94 and 21 nm (spectroscopic ellipsometry), and 99 and 23 nm (XRR), respectively. Dry etching combined with the transfer process yielded a single-crystalline 20 nm thick silicon film onto a polymer.

4. Conclusion

To conclude, we have successfully developed a process in order to transfer single crystalline thin silicon films from SOI substrates onto polymers with standard 200 mm industrial tools. To that end, a specific bonding process has been developed and optimized. It was based on a fluorinated temporary carrier with a suitable adherence to correctly handle, thin down and dismount the silicon film. The process yielded Silicon On Polymer (SOP) structures with a silicon thickness ranging from 20 to 205 nm and a polymer thickness of 230 µm. The crystalline quality of the film was kept throughout the process and full 200 mm wafers or patterns could be transferred. The overall defectivity of the film depended on its thickness. These results outline the versatility of the process and supply a way to manufacture structures for 3D integrated circuits and flexible electronics.

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Graphical abstract

Manufacturing of Silicon On Polymer nano-structures: transfer of an ultrathin single crystal silicon film from a Silicon On Insulator to a polymer