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# Development of industrial processes for the fabrication of high efficiency n-type PERT cells

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ABSTRACT

In this work, two process simplifications for n-type PERT (passivated emitter rear totally diffused) bifacial solar cells are investigated. Both are based on a single thermal treatment for elaborating boron and phosphorus doped regions aiming at reducing the number of high temperature steps of standard process. The first simplification shows a mixed co-diffusion from a gaseous source of phosphorus and a boron doped dielectric layer elaborated by low frequency plasma enhanced chemical vapor deposition (PECVD). The second exhibits two independent ion implantations, followed by a co-anneal/activation step. In both cases, implied open-circuit voltages are similar to standard process (~660–670 mV) and emitters allow good contacting by screen-printing ($\rho_c$=3.0–5.0 mΩ cm$^2$). PERT cells resulting from these processes show very promising performances with efficiency up to 19.7% on industrial 156 × 156 mm$^2$ pseudo square Cz wafers.



## 1. Introduction

N-type silicon is known to provide higher bulk lifetime as well as lower sensitivity towards metal impurities [1,2] and light induced degradation (compared to p-type Si) [3]. Nonetheless standard n-type cell process with reduced cost is still required for a mass production involving such a promising material. Conventional n-type PERT solar cells exhibit two diffused areas: a boron doped emitter and a phosphorus doped back surface field (BSF). Both are the result of diffusion in separate furnaces respectively under $BCl_3$ (or $BBr_3$) and $POCl_3$ atmospheres, resulting in a complex and high-thermal budget process [4]. In order to reduce costs, one option would be to gather these two high-temperature gaseous diffusion steps in a single one, consisting in a simultaneous diffusion of boron and phosphorus, called co-diffusion. However, elaborating boron and phosphorus doped regions at the same time, in one furnace, from two different gaseous sources is almost impossible due to cross-doping issues. Based on the co-diffusion principle, two promising alternative dopant sources are investigated. The former involves ion implantation [5,6] and the latter a highly doped dielectric [7]. The use of doped dielectrics is quite new and there are to our knowledge only few cell results [8,9]. The main challenges for both processes are to obtain a uniform emitter doping, a good contact by screen-printing and a good passivation. This paper aims at presenting process simplifications resulting from both dopant sources and at comparing them to the standard process in terms of emitter features, passivation and cells parameters.

## 2. Description of processes and techniques

N-type PERT bifacial solar cells were made on industrial 156 × 156 mm$^2$ pseudo square Cz wafers ($\rho$=2.5 Ω cm) according to both simplified process flows presented in Fig. 1 referred as processes B and C (middle-right) in this paper. Standard cells based on two separate gaseous diffusions were also made as reference process flow, referred as process A.

The first process simplification (process B) involves a mixed co-diffusion from a $POCl_3$ atmosphere and a boron doped silicon oxide layer ($SiO_x$:B). In order to replace the boron gaseous source, a boron doped dielectric layer was considered to act as dopant source and barrier to phosphorus diffusion. After an alkaline texturization, the $SiO_x$:B thin layer is deposited by low frequency plasma enhanced chemical vapor deposition (PECVD) from $SiH_4$, $N_2O$ and $B_2H_6$. This layer is processed at a temperature below 450 °C which removes a high temperature step. The mixed co-diffusion is then made in a standard diffusion furnace from a $POCl_3$ atmosphere. At the front,

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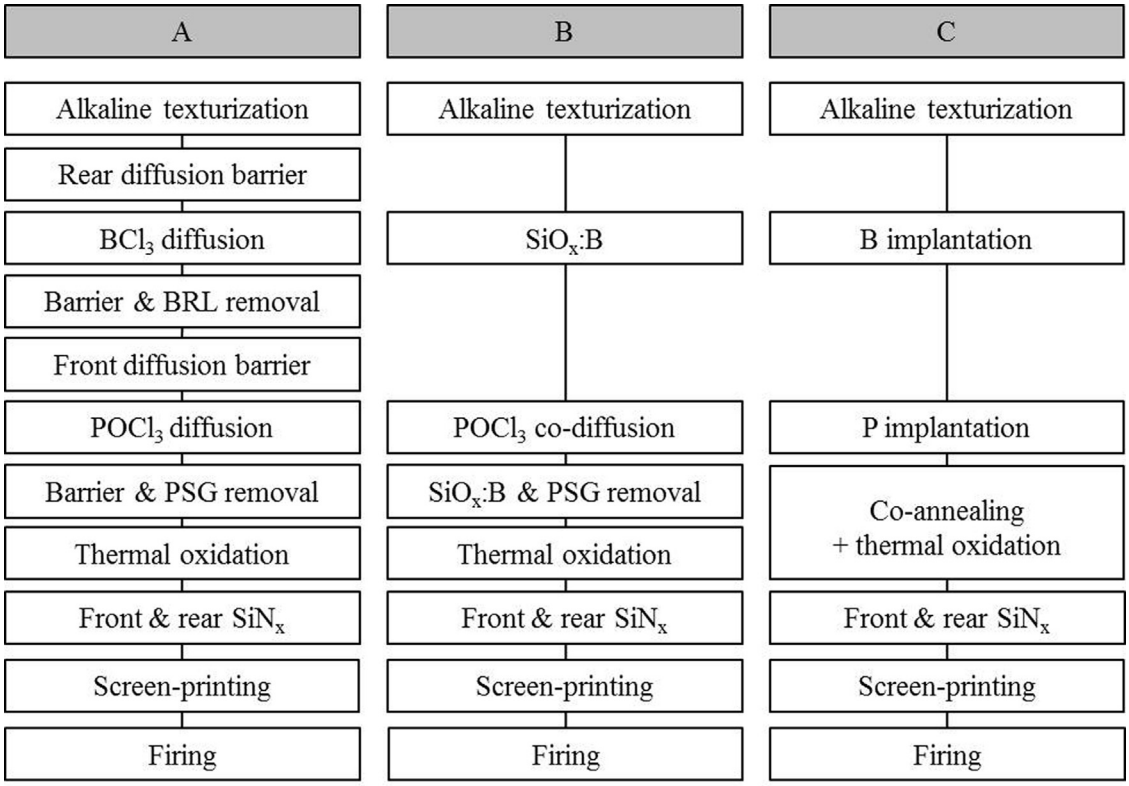


**Fig. 1.** N-type PERT bifacial solar cells process flows: (A) separate diffusions (standard process), (B) mixed co-diffusion, and (C) $I^2$ co-annealing.

boron diffuses from the dielectric while BSF is created by gaseous diffusion of phosphorus. After a chemical step for $SiO_x$:B and phosphorus silica glass etching, a passivation and anti-reflecting stack is added on both sides, consisting in thermal silicon oxide and PECVD silicon nitride ($SiO_2/SiN_x$). Finally, emitter and BSF are contacted during a firing step after screen printing of Ag/Al and Ag paste, respectively. Two independent ion implantations ($I^2$) for emitter and BSF fabrication are used in the second process simplification (process C). After an alkaline texturization, phosphorus and boron atoms are implanted on rear and front side respectively. Both dopants are then electrically activated during a co-annealing step under oxidizing atmosphere. Ion implantation damages are cured and both dopants diffuse simultaneously while emitter and BSF are passivated by high quality thermal $SiO_2$ layer. Both sides are then covered with PECVD $SiN_x$ layer. The metallization scheme is similar to standard and mixed co-diffusion process flows.

It results that mixed co-diffused and $I^2$ co-annealed process flows are shorter and move from 12 to 9 and 8 steps respectively. Moreover, the former has two high temperature steps and the latter only one which results in both cases in a lower thermal budget that significantly reduces solar cell cost and opens door to the use of a wider range of silicon material.

Passivation on each emitter was evaluated using symmetrical texturized and boron diffused or implanted samples. For mixed co-diffused samples, the boron doped dielectric layer was first chemically removed (HF dip). All samples were then coated with a passivation stack ($SiO_x/SiN_x$) on both sides and fired. Quasi Steady State Photoconductance (QSSPC) technique was used to measure implied open-circuit voltages ($iV_{oc}$) and emitter saturation current density ($J_{0e}$). Electrochemical capacitance voltage (ECV) was used to determine active boron concentration profiles in emitters. 81 points probe mappings (with an edge exclusion of 15 mm) were made and non-uniformity was calculated using $(\max-\min)/(\max+\min)100$. Solar cell performances were measured by using I-V analysis under standard test conditions (AM1.5G 0.1 W/cm² solar spectrum, $T=25$ °C) on a golden chuck. Reflectivity ($R$) curves were measured on cell precursors (i.e. devices with PERT structure but no metallization). Internal Quantum Efficiency (IQE) data were calculated from External Quantum Efficiency (EQE) measured on a $1\times3$ mm² spot between cells fingers.

## 3. Emitters properties

### 3.1. Doping features

Emitter properties of the three processes were compared regarding sheet resistance ($R_{sheet}$) and boron concentration profiles. B and C process parameters were optimized in order to obtain an equivalent $R_{sheet}$ as obtained by standard diffusion process. It is now well-known that good emitter doping and non-uniformity can be obtained from $BCl_3$ (or $BBr_3$) diffusion and boron implantation. From boron doped silicon oxide, it is also possible to tune the emitter profile by changing deposition parameters and co-diffusion step conditions. For example, two different profiles can be obtained by increasing $SiO_x$:B layer thickness which leads to a deeper and more doped emitter since more boron atoms are available for diffusion (see Fig. 2). Others parameters provide access to emitter profile optimization in terms of depth or boron surface concentration (red curve).

Fig. 3 shows emitter $R_{sheet}$ mapping for each process. Process A exhibits a 71.6 Ω/sq mean $R_{sheet}$ value with a non-uniformity of 1.2%. Process B shows a similar mean $R_{sheet}$ value whereas that obtained by process C is somewhat 15 Ω/sq higher, reaching an average 88.2 Ω/sq. Both B and C processes present very good $R_{sheet}$ distribution with a low non-uniformity (2.5% and 0.9% respectively).

Corresponding boron concentration profiles after oxidation step, obtained by the ECV technique, are presented in Fig. 4. Boron profile of process A has a maximum concentration around 9.5e19 at/cm$^3$ and a depth of 400 nm. Process B profile has a slightly lower maximum concentration (7.8e19 at/cm$^3$) while process C profile gives a much lower surface doping level at 3.2e19 at/cm$^3$. Concerning emitter depth, *I²* co-annealed sample profile is much deeper than the two others and reaches almost 650 nm, due to a higher temperature of co-annealing step justified by the need of implantation induced damages curing and full boron activation. Although emitters have different doping profiles, they have quite identical contact resistivity ($\rho_c$=3–5 mΩ cm$^2$), which enables good and comparable contacting by screen-printing.

### 3.2. Passivation aspects

Passivated (thermal $SiO_2$+PECVD $SiN_x$) emitter characteristics are shown on Fig. 5 in terms of $iV_{oc}$ and $J_{0e}$ values. It is clear that an analogous 656 mV $iV_{oc}$ value is obtained whatever the fabrication process is. It allows us to expect similar solar cells $V_{oc}$ values. A 86 fA/cm² $J_{0e}$ is measured for mixed co-diffused samples, which confirms the good emitter quality obtained using the boron doped dielectric layer. However, it is doubled for *I²* co-annealed samples. Despite the high anneal temperature used for boron activation, the annealing seems to have not been long enough to totally activate implanted boron atoms and to cure implantation damages [6]. Nevertheless, these implantation co-annealing conditions are optimal for cells fabrication.

Monitoring of bulk minority carrier lifetime and wafer resistivity along the process was done for a fair comparison of the three processes performances (see Fig. 6). In this case, three sample batches were prepared according to each process flow (without metallization). After doped regions chemical etching and surface cleaning, samples were passivated with a good quality $SiN_x$ layer. Some unprocessed wafers were passivated with the same layer as a reference. Standard diffusion and mixed co-diffusion samples exhibit the best effective lifetime, near the reference initial bulk lifetime, while *I²* co-annealed samples lifetimes are a bit lower. Nevertheless, it does not impact significantly $iV_{oc}$ values.

On the other hand, it is seen that the different temperature and time of thermal steps within the three process flows can affect silicon wafer properties. In particular, oxygen-related thermal donors (TD) are n-type dopants that appear in oxygen-rich silicon

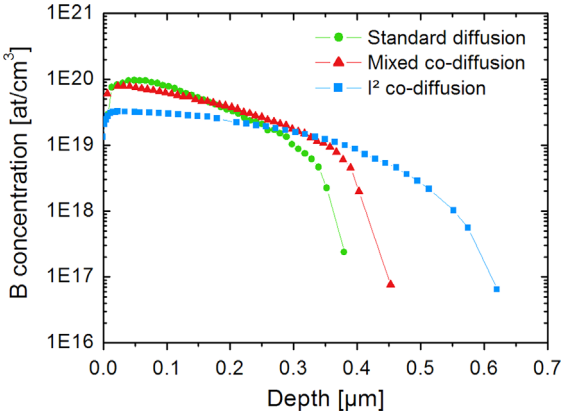


**Fig. 4.** Boron concentration profiles measured by ECV measurements.

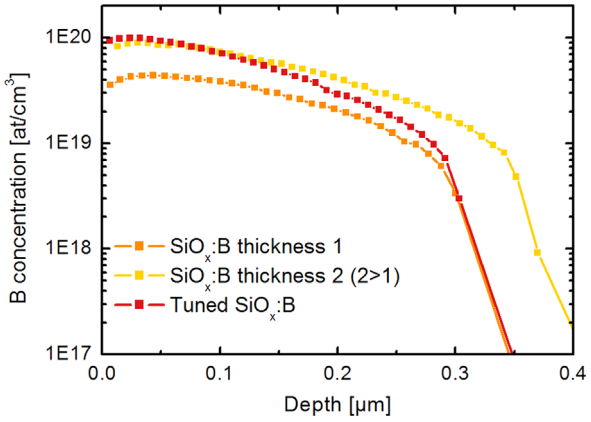


**Fig. 2.** Example of different boron emitter profiles obtained from $SiO_x$:B layer, measured by ECV measurements.

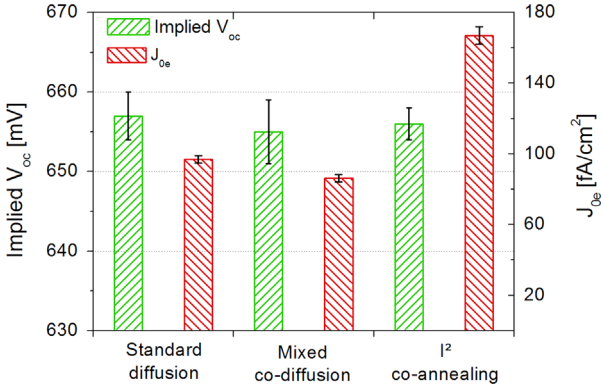


**Fig. 5.** Implied $V_{oc}$ and $J_{0e}$ values determined by QSSPC measurements for each process after a firing step.

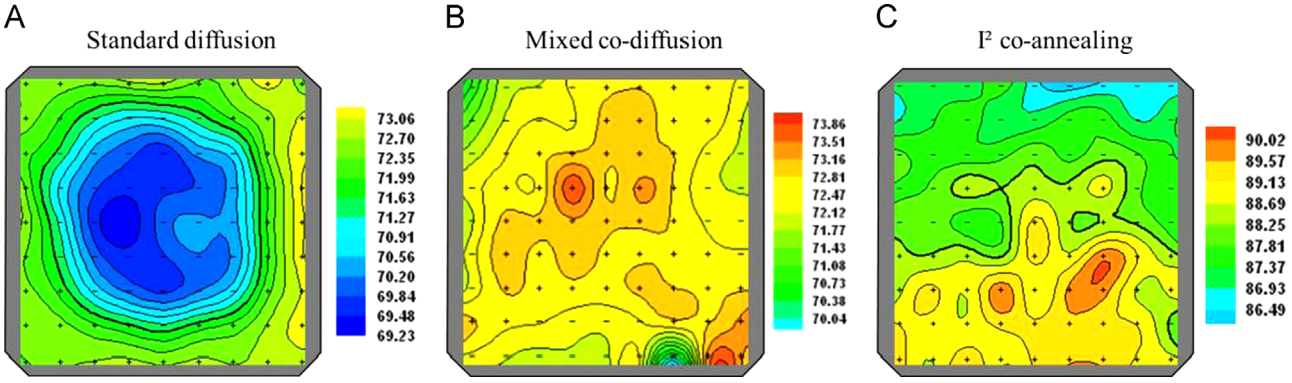


**Fig. 3.** Emitter $R_{sheet}$ mappings. 4-point probe measurement on textured 156 psq wafers.

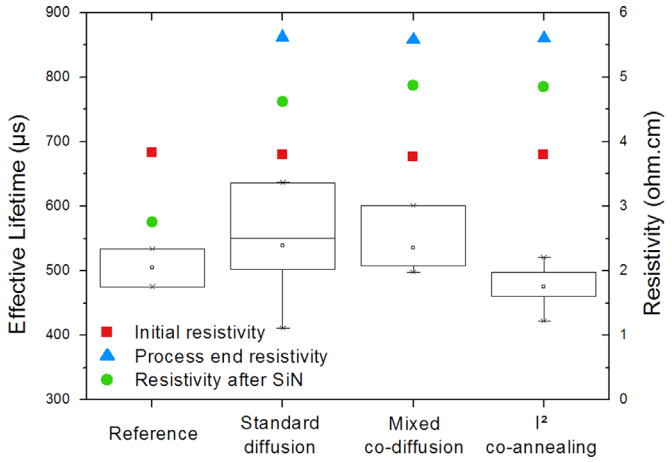


**Fig. 6.** Effective bulk lifetimes (box plots) determined by QSSPC measurements (@1 sun illumination) and resistivity (symbols) for each process. Resistivity was measured after high temperature (HT) step ( > 800 °C) and after passivation by a good quality silicon nitride deposited at 450 °C.

and that impact wafer resistivity [10,11]. TD are generated when wafers are annealed in the temperature range 450–600 °C while higher temperature anneals cause their destruction. An increase in TD density leads to a decrease in bulk resistivity. The different PERT process flows mentioned in this paper involve both thermal steps which are liable to create and to destroy TD. Therefore, end process resistivity needs to be monitored for better process flow comparison since it directly impacts recombination (especially Shockley–Read–Hall) and as a consequence, $J_{cc}$ and $V_{oc}$ values.

The resistivity of our samples was measured using 4-points probe technique. For processes A and B, it moves from 3.8 to 5.6 Ω·cm after high temperature processing ( > 800 °C), which follows the literature. During the deposition of the $SiN_x$ passivation layer at 450 °C, new thermals donors are created, leading to a diminution of wafer resistivity. This phenomenon is also observed for our processed and unprocessed samples whose resistivity decreases of 1 Ω·cm in average. The difference of resistivity after passivation is not high enough to impact $iV_{oc}$ values and it indicates that thermal budgets of the three processes are quite similar.

Considering the integration of these emitters into PERT solar cells, implied $V_{oc}$ was also measured on cell precursors including a standard passivation stack ($SiO_2/SiN_x$). Each process shows close $iV_{oc}$ values around 660 mV. These good results encouraged us to fabricate PERT solar cells from each process flow.

## 4. Solar cell results

The *I–V* parameters of 239 cm² n-type PERT bifacial solar cells made by standard (A) and alternative (B and C) processes are listed in Table 1. Results tend to say that open-circuit voltages ($V_{oc}$) of alternative and simplified processes are higher to those obtained with the standard process, with an increase of 3–4 mV. The difference observed between $iV_{oc}$ and cell $V_{oc}$ (about 10 or 15 mV) is due to well-known emitter degradation during screen-printing and firing steps that degrade emitter [12]. Short-circuit current densities obtained under A and C processes are equivalent whereas it is slightly higher for B cells (attributed to a less deep and recombinating emitter as mentioned in part 3). Very good conversion efficiencies are achieved. Process B and C champion cells exceed 19.7% efficiency and are about to equal standard process best cells in a foreseeable future. These efficiencies are mainly limited by low fill factor and pseudo fill factor (PFF) values.

**Table 1**
Photovoltaic parameters of fabricated solar cells (156 × 156 mm² pseudo square area).

| Process type | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm²) | FF (%) | PFF (%) | $\eta$ (%) |
|---|---|---|---|---|---|
| Standard diffusion | 642.8 | 39.0 | 78.5 | 82.7 | 19.7 |
| Best cell | 643.2 | 39.1 | 78.5 | 82.8 | **19.8** |
| Mixed co-diffusion | 646.6 | 39.2 | 77.1 | 82.3 | 19.5 |
| Best cell | 649.4 | 39.3 | 77.1 | 82.5 | **19.7** |
| *I²* co-annealing | 645.8 | 39.0 | 77.7 | 81.9 | 19.6 |
| Best cell | 645.8 | 39.0 | 78.0 | 81.9 | **19.7** |

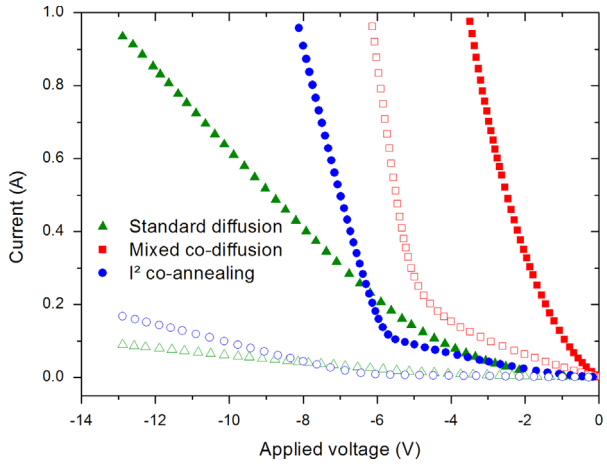


**Fig. 7.** Reverse dark current–voltage characteristics in linear drawing, measured before (filled symbols) and after (open symbols) cell edges removal by laser ablation. Cells surface moves from 239 cm² to 229.4 cm².

In case of mixed co-diffused cells, this is probably due to a light deposition of $SiO_x$:B layer on wafer rear side periphery leading to an increased shunt. A gain of 1.0–1.5% in FF is revealed after cell edges removal by laser ablation, leading to efficiencies over 20.0%. Although this issue needs to be solved to totally master the mixed co-diffusion process, doped dielectrics open the door to higher conversion efficiencies.

Solar panels are made of typically 60 cells and each one attempts to produce current in direct proportion to the amount of sunlight it receives. The connection of cells in series can lead to reverse biasing of some cells in case of shading of the module. Therefore the reverse characteristic of the solar cells should be optimized in such a way that as little power as possible is dissipated under reverse bias. In order to have better reliability and security for integration, cells breakdown voltage ($V_{bd}$) must be maximized and breakdown as soft as possible [13].

Some reverse dark *I–V* measurements were carried out on cells of each process flow, before and after edges removal by laser ablation (see Fig. 7). The $V_{bd}$ values were extracted from reverse characteristics at cross section point between asymptotes in zero and maximum reverse voltage. Before laser ablation, reverse dark *I–V* curves interpretation is quite hazardous since we do not know exactly junction features on cell edges. However, it is noticeable that a lower shunt resistance was obtained for mixed co-diffused cells. For *I²* co-annealed cell, a soft breakdown starting from −1 V is observed, followed by a hard breakdown starting around −6 V. The standard process flow provides cells with lower hard breakdown slope whereas it is much higher for mixed co-diffused cell which would lead to higher dissipated power in case of shading. As high quality monocrystalline Cz n-type silicon was used, the early breakdown is not due to bulk metal contamination like in multicrystalline silicon [14]. In order to get rid of junction issues on cell edges, these have been removed by laser processing on

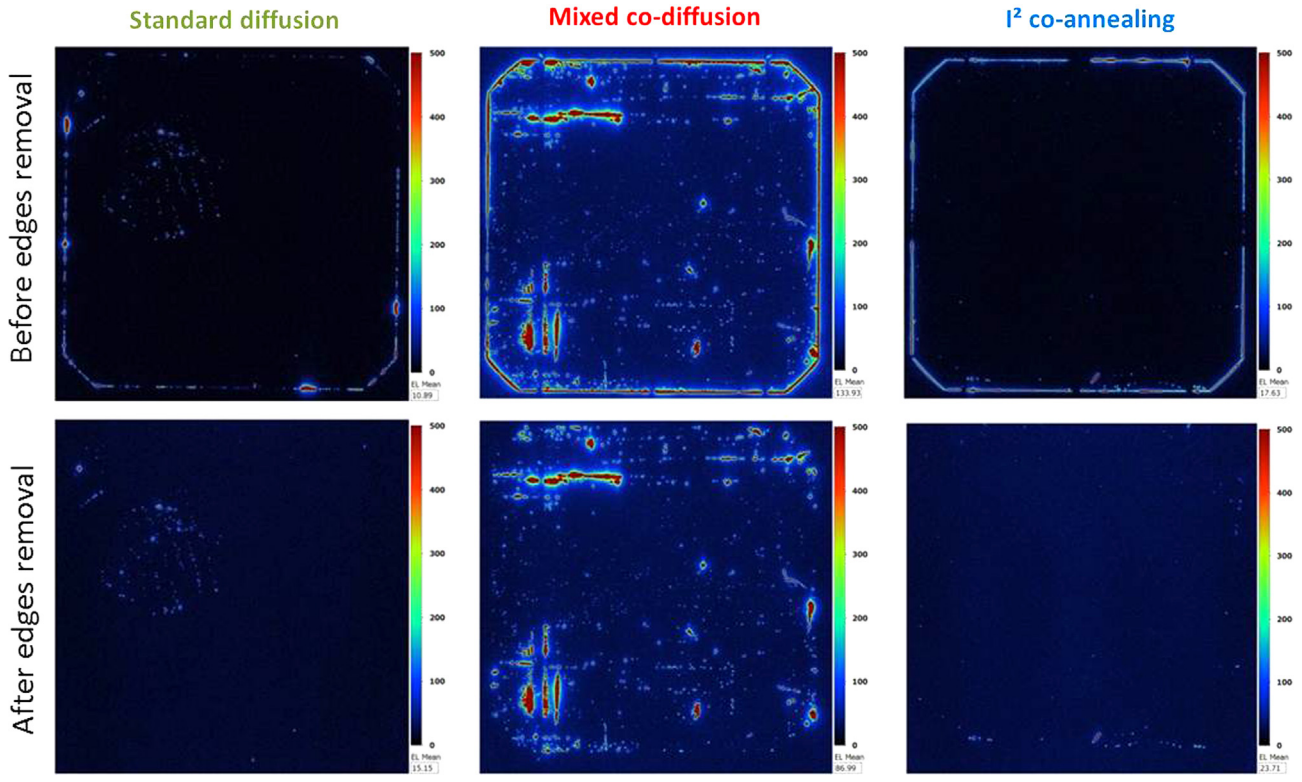


**Fig. 8.** Reverse Bias Electroluminescence mappings, before and after cell edges removal by laser ablation.

wafer rear side (to avoid shunting of p–n junction). After edges removal, curves of standard and $I^2$ co-annealing process are softened and their $V_{bd}$ are $-5$ and $-6.5$ V respectively. These data are comparable to those obtained in previous work [15]. Initially, mixed co-diffused cell $V_{bd}$ is really low ($< -2$ V) and it is significantly improved (moving to $-5$ V) after laser processing.

The two classic mechanisms leading to breakdown of reverse-biased p–n junctions are tunneling (Zener effect) and avalanche multiplication (impact ionization) [16]. These two effects can be distinguished by varying the temperature and observing the voltage shift of the reverse dark $I$–$V$ curve. For the three processes, the breakdown current was reached at higher reverse voltages when increasing temperature from 25 to 60 °C. This positive shift tends to say that avalanche multiplication is the dominant mechanism of breakdown in all cases. On the other hand, the reverse dark $I$–$V$ characteristic is also linked to emitter doping profile. If we consider the curves after laser ablation, the implanted emitter doping profile is much deeper, which could lead to a large avalanche effect area but with a low ionization rate since the doping slope is relatively low. The two other emitters are more abrupt which could explain a lower $V_{bd}$ (high field obtained more quickly) due to an increased tunneling effect.

As mentioned in [15], three types of defect signatures can be evidenced by Reverse Bias Electroluminescence (ReBEL) mappings: edge defects, handling-induced defects and diffusion-induced defects. In the three cases, laser processing eliminates edge defects localized along cells perimeters, which is clearly confirmed on ReBEL mappings presented in Fig. 8. For $I^2$ co-annealed cells, only few edges handling-induced defects remain after edges removal and for standard diffused cells, a large defects spot is notable, due to handling (vacuum wand) during rear diffusion barrier deposition. The removal of major defects for both processes explains the good reverse dark $I$–$V$ curves. The third defect type, boron diffusion-induced defects, seems to be the reverse bias behavior limiting factor of mixed co-diffused cells after laser processing. During $SiO_x$:B layer deposition, a larger boron rich layer (BRL) is developed, confirmed by the observation of a different dewetting behavior compared to the other processes. A larger BRL is potentially more virulent, which induces more defects on wafer front side. This is in line with ReBEL mapping which shows a higher defect density for mixed co-diffused cells.

## 5. Conclusion

We conclude that simplified processes are very promising alternatives to standard n-type PERT bifacial solar cells process manufacturing. Both are comparable in terms of doping, passivation and conversion efficiency. 19.5% average cell efficiency was achieved using mixed co-diffusion process and 19.6% for $I^2$ co-annealing. Besides, both propose a process simplification that leads to diminish the number of high thermal steps, essential for a large scale cost-effective fabrication process.

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## References

[1] D. Macdonald, L.J. Geerligs, Recombination activity of interstitial iron and other transition metal point defects in p and n-type crystalline silicon, Appl. Phys. Lett. 85 (18) (2004) 4061–4063.
[2] J.E. Cotter et al., p-Type vs. n-type silicon wafers: prospects for high-efficiency, commercial silicon solar cells, in: Proceedings of the 15th Workshop on Crystalline Silicon Solar Cells & Modules: Materials and Processes, 2005.

[3] L.J. Geerligs, D. Macdonald, Base doping and recombination activity of impurities in crystalline silicon solar cells, Prog. Photovolt.: Res. Appl. 12 (4) (2004) 309–316.
[4] J. Zhao et al., High efficiency PERT cells on n-type silicon substrates, in: Proceedings of the 29th IEEE, 2002, p. 218.
[5] T.S. Boscke, et al., Fully ion implanted and coactivated industrial n-type cells with 20.5% efficiency, IEEE J. Photovolt. 99 (2013) 2156–3381.
[6] A. Lanterne et al., High efficiency fully implanted and co-annealed bifacial n-type solar cells, in: Proceedings of the 3rd SiliconPV, vol. 38, 2013, pp. 283–288.
[7] R. Keding et al., Silicon doping performed by different diffusion sources aiming co-diffusion, in: Proceedings of the 27th EU PVSEC, Frankfurt, Germany, 2012, pp. 1906–1911.
[8] B. Bazer- Bachi, et al., Co-diffusion from boron doped oxide and $POCl_3$, in: Proceedings of the 26th EU PVSEC, Hamburg, Germany, 2011, pp. 1155–1159.
[9] N. Weheier, G. Schraps, H. Wagner, B. Lim, N.-P. Harder, P.P. Altermatt, Boron-doped PECVD silicon oxides as diffusion sources for simplified high-efficiency solar cell fabrication, in: Proceedings of the 28th EU PVSEC, Paris, France, 2013.
[10] V. Cazcarra, P. Zunino, Influence of oxygen on silicon resistivity, J. Appl. Phys. 51 (8) (1980) 4206–4211.
[11] J. Veirman, S. Dubois, N. Enjalbert, J.P. Garandet, D.R. Heslinga, M. Lemiti, Hall mobility reduction in single-crystalline silicon gradually compensated by thermal donors activation, Solid State Electron. 54 (2010) 671.
[12] J. Singer et al., 2d TCAD simulation of high efficiency n-type c-Si solar cell: correlation between the screen-printing metallization and the loss in cell Voc, in: Proceedings of the 27th EU PVSEC, Frankfurt, Germany, 2012.
[13] M.C. Alonso-Garcia, J.M. Ruiz, F. Chenlo, Experimental study of mismatch and shading effects in the *I–V* characteristic of a photovoltaic module, Sol. Energy Mater. Sol. Cells 90 (3) (2006) 329–340.
[14] W. Kwapil, et al., Diode breakdown related to recombination active defects in block-cast multicrystalline silicon solar cells, J. Appl. Phys. 106 (6) (2009) 063530-1–063530-7.
[15] F. Dauzou, R. Cabal, Y. Veschetti, Electrical behaviour of n-type silicon solar cells under reverse bias: influence of the manufacturing process, Sol. Energy Mater. Sol. Cells 104 (2012) 175–179.
[16] S.M. Sze, K. Ng Kwok, Physics of Semiconductor Devices 2007107–110.