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RESEARCH ARTICLE

Understanding of the annealing temperature impact on ion implanted bifacial n-type solar cells to reach 20.3% efficiency

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ABSTRACT

Ion implantation has the advantage of being a unidirectional doping technique. Unlike gaseous diffusion, this characteristic highlights strong possibilities to simplify solar cell process flows. The use of ion implantation doping for n-type PERT bifacial solar cells is a promising process, but mainly if it goes with a unique co-annealing step to activate both dopants and to grow a SiO₂ passivation layer. To develop this process and our SONIA cells, we studied the impact of the annealing temperature and that of the passivation layers on the electrical quality of the implanted B-emitter and P-BSF. A high annealing temperature (above 1000 °C) was necessary to fully activate the boron atoms and to anneal the implantation damages. Low J_{0BSF} (BSF contribution to the saturation current density) of 180 fA/cm² was reached at this high temperature with the best SiO₂ passivation layer. An average efficiency of 19.7% was reached using this simplified process flow (“co-anneal process”) on large area (239 cm²) Cz solar cells. The efficiency was limited by a low FF, probably due to contaminations by metallization pastes. Improved performances were achieved in the case of a “separated anneals” process where the P-BSF is activated at a lower temperature range. An average efficiency of 20.2% was obtained in this case, with a 20.3% certified cell. Copyright © 2014 John Wiley & Sons, Ltd.

KEYWORDS

silicon solar cells; ion implantation; n-type; thermal annealing; phosphorus BSF; boron emitter

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1. INTRODUCTION

During the last decade, the main objective of the silicon based photovoltaic industry has remained the reduction of the global cost of ownership via the increase of the solar cells efficiency or via the simplification of the fabrication process, which also includes the reduction of consumables and of the breakage rate.

In this context, N-type PERT solar cell has been recently identified as a promising candidate that could replace and exceed the current leadership of the conventional p-type solar cell by reaching both high efficiency and a cost-effective (\$/W) process [1]. This structure, shown on Figure 1, benefits from all the n-type silicon advantages: the absence of light induced degradation (LID) [2,3], a low sensitivity to

metallic impurities and a high lifetime potential [4]. Intrinsically bifacial, this structure has also the potential to achieve an increased energy yield (kWh/kWp) in module configuration [1]. The main limitation highlighted up to now is the high number of process steps compared to the simple p-type solar cell process. Indeed, using conventional BBr₃ and POCl₃ high temperature diffusions, several masking steps and chemical oxide removal must be added in order to isolate the front B-emitter from the rear P-BSF [5]. Among the various ways discussed in the literature to simplify this process flow, two solutions have been highlighted: the co-diffusion approach [6] and the use of ion implantation [1,7].

The idea of using ion implantation for the doping of solar cells already appears in the 1980s [8]. But it's only

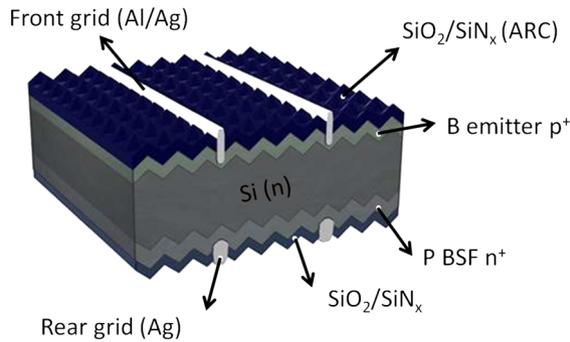


Figure 1. Capture cross section of the n-type PERT solar cell.

recently, thanks to the development of ion implantation tools with higher throughput [9,10], that this technique became compatible with the photovoltaic industry. Since then, its benefits for the fabrication of p-type solar cells have been shown [11]. Unlike diffusion, it has the advantage of precisely controlling the concentration profiles of the junction and of removing the masking and etching steps thanks to its unidirectional doping, but requires an added thermal step to activate the dopants.

In the case of implanted n-type PERT solar cells, the process can be further simplified by the use of a single thermal annealing to activate the front B and the rear P implanted atoms. A thermal oxide can also be grown during the dopants activation annealing, leading to a high passivation quality layer without additional step. However, the main challenge remains the realization of a high quality implanted boron emitter, which needs the use of high annealing temperatures [12].

The best efficiencies reported so far on implanted n-type PERT solar cells with screen-printing metallization grids have reached 20.5% using Al_2O_3 boron passivation [13]. The SiO_2 passivation has also been investigated in several publications, but efficiencies in this case have been limited below 20% due to lower V_{oc} and J_{sc} [14,15]. However, Y. Tao in [15] managed to increase the V_{oc} thanks to a planar rear surface and a lower metal coverage (point contacts). Compared to Al_2O_3 passivation, SiO_2 can bring a significant advantage for industrialization in the case of a concomitant growth during the activation annealing. Therefore we focused our study on this latter passivation technique, using a grid screen-printing on the rear side and no point contacts to keep the bifacial cell advantages.

Our main goal was to develop the simplest process as possible, which involves the use of a “co-anneal” step for B and P dopant activation as well as a SiO_2 -based passivation. For this purpose, we first studied the quality of the B-implanted emitter and P-implanted BSF depending on the annealing temperature and passivation stacks. Symmetrical $p^+/n/p^+$ and $n^+/n/n^+$ structures were used for this study. Complete solar cells were then fabricated with the “co-anneal” process. For a better understanding of the limitations of this process, they were compared to solar cells fabricated using a “separated anneals” approach, where a

second anneal is added to activate the P dopants at a lower temperature. The resulting components are called *SONIA* cells (Solar N-type Implanted Advanced cells).

2. EXPERIMENT

Czochralski (Cz) n-type wafers of $3.5\ \Omega\cdot\text{cm}$ ($239\ \text{cm}^2$) were used for symmetrical samples studies as well as for solar cells fabrication.

2.1. Symmetrical p^+n/p^+ and n^+nn^+ samples

Symmetrical $p^+/n/p^+$ samples were fabricated to measure the B-emitter quality. The influence of the annealing temperature and of the boron implantation dose was studied in the optimal conditions. This involves the use of polished wafers with an Al_2O_3 layer deposition for the emitter passivation. The overall process flow is detailed on Figure 2 (“ Al_2O_3 process”), only the KOH texture is removed. The wafers were implanted with boron using a beamline implanter with doses ranging from 1.10^{14} to 8.10^{14} at/cm². The boron atoms were activated by two different thermal anneals in nitrogen (N_2) ambient, the former with a peak temperature T_p of $950\ ^\circ\text{C}$ and the latter with a T_p of $1050\ ^\circ\text{C}$.

The influence of the passivation layer on the emitter quality was also studied. For this study, symmetrical $p^+/n/p^+$ samples were fabricated in the same conditions than the solar cells processing, meaning that the wafers were textured (KOH 1%) at the beginning of the process. Three different passivation stacks were compared on the boron emitter for a fixed implantation dose and a thermal annealing at $T_p = 1050\ ^\circ\text{C}$ (corresponding to an emitter sheet resistance (R_{sheet}) of $90\ \Omega/\text{sq}$). The formation of the three passivation stacks (named “ Al_2O_3 ”, “etched- Al_2O_3 ” and “ SiO_2 ”) is detailed on Figure 2. In the “etched- Al_2O_3 ” case, an oxidation step was included during the annealing of boron, and the resulting grown SiO_2 layer was then removed by a HF dip before Al_2O_3 deposition.

Finally, $n^+/n/n^+$ samples were fabricated by a similar process flow, to study the impact of the annealing

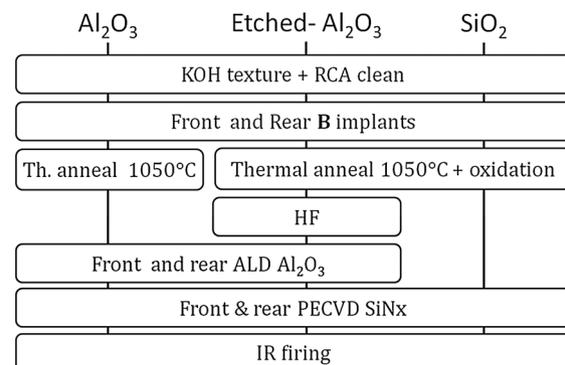


Figure 2. Symmetrical $p^+/n/p^+$ sample process flows depending on the passivation layers.

temperature on the P-BSF electrical quality. Following the P-implantation on textured wafers, thermal anneals of 1 h were used for P activation with peak temperatures ranging from 850 °C to 1050 °C. Two different SiO₂/SiN_x stacks were compared for the passivation (stack A and stack B). A and B differ in the thicknesses of SiO₂ and SiN_x layers. The SiO₂ thickness is larger in stack A along with a thinner SiN_x layer.

An annealing in an infra-red belt-furnace was performed on all the symmetrical samples, before the characterization, to simulate the co-firing cycle of the screen-printed pastes. Samples were then characterized by the QSSPC technique developed by Sinton Consulting [16] to extract the saturation current density of the emitter (J_{0e}), the saturation current density of the BSF (J_{0BSF} or J_{0b}) and their corresponding implied V_{oc} . The R_{sheet} was measured on these samples by four-point probe method. For an accurate measurement of the sheet resistance (R_{sheet}) of the P-BSF, the same process was performed on p-type wafers for each annealing temperature.

2.2. Solar cell fabrication

The two process flows, presented on Figure 3, were used for the fabrication of the *SONIA* cells.

Both processes started by a KOH texture and a RCA clean. In the process named “co-anneal” the RCA clean was followed by the B implantation on the front side and by the P implantation on the rear side. Both dopants were then activated by a thermal anneal at $T_p = 1050$ °C with an annealing scheme called “Anneal HT”. In the “separated anneals” process, the RCA clean was followed by the B implantation on the front side and its activation under the “Anneal HT” at 1050 °C. Next, P ions were implanted on the backside, and a second anneal with a lower temperature range ($T_p < 900$ °C) was used for the P activation (“Anneal LT”). The front and rear side of the cells were then passivated by SiO₂/SiN_x stacks. The stack A was used on the “co-anneal” BSF (BSF_A) and the stack B on the “separated anneals” BSF (BSF_B). Explanation for this

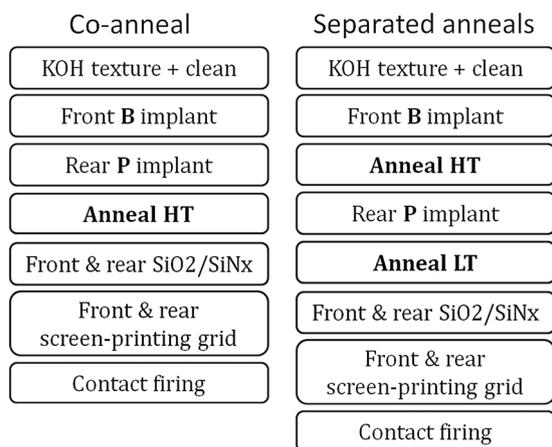


Figure 3. Implanted n-type PERT process flows.

choice will be provided in the following section. The end of the fabrication was similar for both processes. Contacts were ensured by the screen-printing of grids using Al/Ag and Ag pastes on the front and rear side, respectively, with a co-firing in an infra-red (IR) belt-furnace.

Illuminated I–V (AM1.5) and Dark I–V characteristics were measured at 25 °C on a reflective gold plated chuck.

3. RESULTS AND DISCUSSION

3.1. Impact of the annealing temperature and SiO₂ passivation on the B-emitter

The main challenge of the implanted n-type PERT process is the activation of implanted boron atoms. It has been widely demonstrated this last year, that depending on the boron implantation dose, temperatures above 950 °C are necessary, to fully activate the implanted boron atoms and cured the implantation damages [12].

The impact of the annealing temperature on the emitter quality was studied for various implantation doses using the optimal conditions (polished wafers and Al₂O₃ ALD deposition).

Figure 4 a) shows the R_{sheet} measured on SiN_x/Al₂O₃/p⁺/n/p⁺/Al₂O₃/SiN_x samples. For both annealing peak temperatures ($T_p = 950$ °C and $T_p = 1050$ °C), the R_{sheet} values exhibit a strong decrease for an increasing implantation dose, down to 150 Ω/sq for 8×10^{14} at.cm⁻². This trend is explained by an increase of the active boron concentration due to the higher implantation dose as it can be seen on Figure 5 which presents the active boron concentration profiles measured by electrochemical capacitance-voltage analysis (ECV). The differences of R_{sheet} between both annealing temperatures, observed for the lowest implantation doses, were explained by the change in the carrier mobility due to the difference in the boron concentration profile between a 950 °C and a 1050 °C annealing [17].

Figure 4 b) shows the J_{0e} values measured on the same samples. For the lowest dose (1×10^{14} at.cm⁻²), very low J_{0e} values (under 20 fA.cm⁻²) were measured for both annealing temperatures. These low J_{0e} values reveal a complete activation of the boron implanted atoms and the annealing of all the implantation damages. In the case of a higher implantation dose, corresponding to R_{sheet} closer to 100 Ω/sq, only the highest annealing temperature allows us to reach a low J_{0e} value. These results are in agreement with previous studies [12] and confirm that for the formation of a boron emitter suitable for contact by screen-printing metallization (R_{sheet} below 150 Ω/sq), a 1050 °C peak temperature is highly recommended to reach a high emitter electrical quality.

The 1050 °C peak temperature was kept in the following studies to form a 90 Ω/sq boron emitter, thanks to implantation dose optimisations between 8×10^{14} at/cm² and 3×10^{15} at/cm². To estimate the loss due to the use of a SiO₂ layer instead of an Al₂O₃ based passivation, mainly

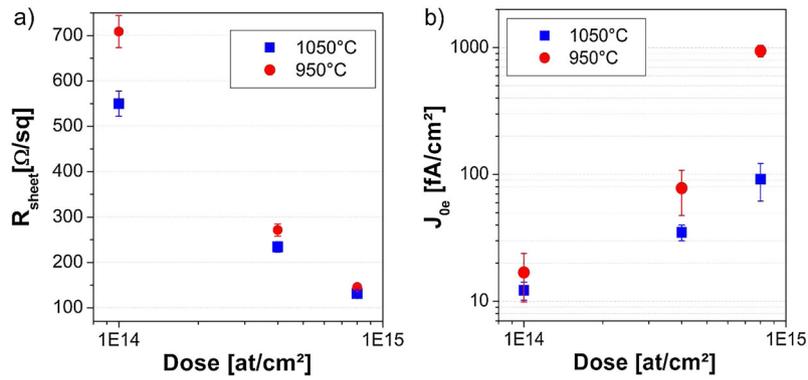


Figure 4. a) R_{sheet} and b) J_{0e} measured on implanted $SiN_x/Al_2O_3/p^+/n/p^+/Al_2O_3/SiN_x$ samples annealed at $T_p = 950^\circ C$ or $T_p = 1050^\circ C$.

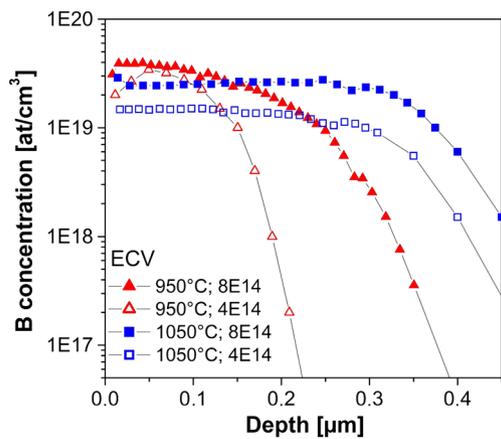


Figure 5. ECV profiles of boron implanted emitters with implantation dose of $8 \times 10^{14} at/cm^2$ or $4 \times 10^{14} at/cm^2$ annealed at $T_p = 950^\circ C$ or $T_p = 1050^\circ C$.

used in literature, we compared the R_{sheet} , implied V_{oc} and J_{0e} values obtained on $p^+/n/p^+$ textured samples.

Results for three different passivation stacks are shown on Figure 6 including Al_2O_3/SiN_x layers deposited after the boron activation or after an emitter etching. Implied V_{oc}

and J_{0e} are improved with an etching step previous to the Al_2O_3 deposition. This was explained by the removal of the damage surface along with a small increase of the emitter sheet resistance. These advantages are also present in the case of the SiO_2 passivation but are not sufficient to reach similar implied V_{oc} values than with the Al_2O_3 layers. An average loss of 6 mV was measured on the implied V_{oc} by using SiO_2 passivation corresponding to a J_{0e} value of $131 fA/cm^2$.

3.2. Impact of the annealing temperature on the P-BSF

Previous results have shown that for high implantation dose a peak temperature of $1050^\circ C$ is needed to activate the boron emitter during solar cell fabrication. Therefore this temperature must also be used for the P-BSF activation in the case of a “co-anneal” process flow. The impact of this high annealing temperature on the P-BSF quality was studied in the following section.

Figure 7 shows the sheet resistance measured on textured p-type $n^+/p/n^+$ phosphorus implanted samples annealed during 1 hour at various temperatures. For a given dose, the R_{sheet} decreases with increasing annealing temperature from $63 \Omega/sq$ at $850^\circ C$ to $33 \Omega/sq$ at $1050^\circ C$.

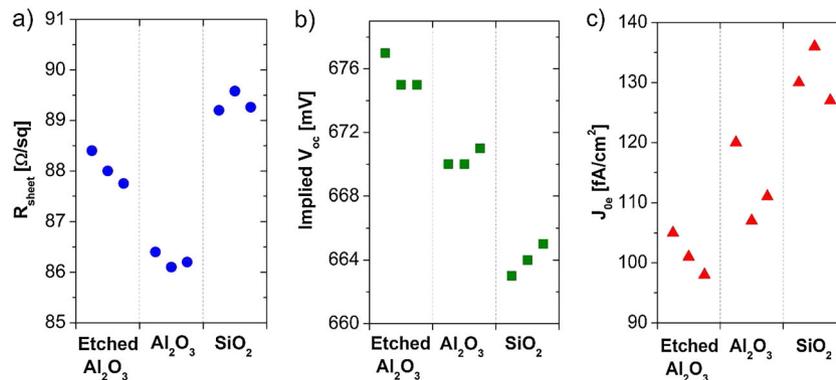


Figure 6. a) R_{sheet} , b) implied V_{oc} and c) J_{0e} measured on boron implanted emitter annealed at $T_p = 1050^\circ C$ with various passivation stacks.

This trend was attributed to a change in the P concentration profile, which shows a reduced surface doping and increased depth at higher annealing temperatures (cf. Figure 8). Indeed,

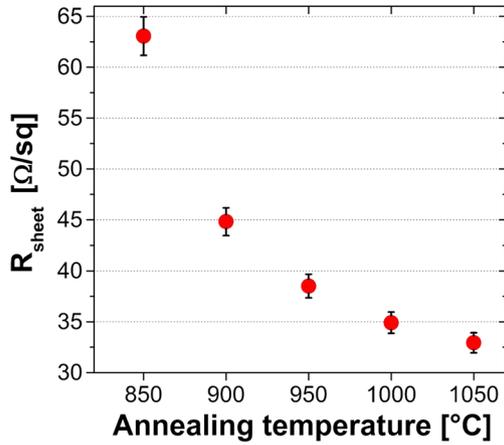


Figure 7. R_{sheet} of implanted phosphorus BSF annealed at various temperatures during 1 h.

as it was highlighted in our previous work on p-type silicon solar cells, all the phosphorus atoms are already activated at 850 °C [18]. Therefore the R_{sheet} decrease is only due to an increase of the carrier mobility for lower concentrated profiles [17].

Figure 9 shows the J_{0BSF} and the implied V_{oc} measured on SiN_x/SiO₂/n⁺/n/n⁺/SiO₂/SiN_x samples using two different SiO₂/SiN_x stacks. For all the conditions, the J_{0BSF} values are below 300 fA/cm² which confirms a high activation rate of the P implanted atoms. An improvement of both parameters is obtained with the stack A (thicker SiO₂ layer) for each annealing temperature leading to J_{0BSF} below 200 fA/cm². An additional benefit is measured at 850 °C with the stack A, where the implied V_{oc} exceeds 670 mV.

SIMS measurements, shown on Figure 10, highlight the variation of the phosphorus concentration profile depending on the passivation stack at 850 °C. In the case of stack A, a large part of the emitter was consumed during the SiO₂ grow leading to a lightly doped emitter of 120 Ω/sq.

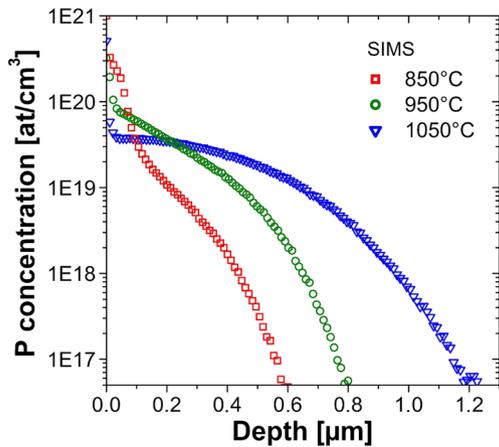


Figure 8. SIMS measurements in the Si of the phosphorus implanted BSF annealed at various temperatures during 1 h followed by an oxidation step.

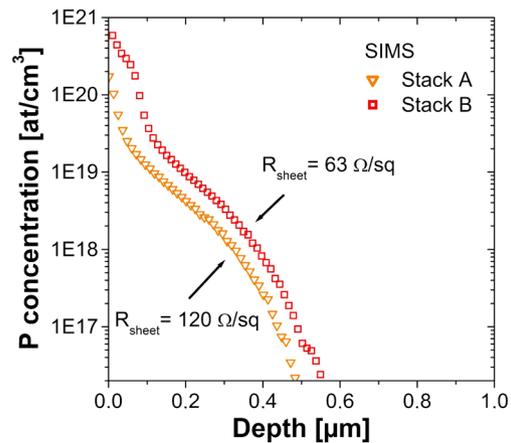


Figure 10. SIMS profiles measured in the Si after P implantation, annealing during 1 h at 850 °C and passivation by stack A or B.

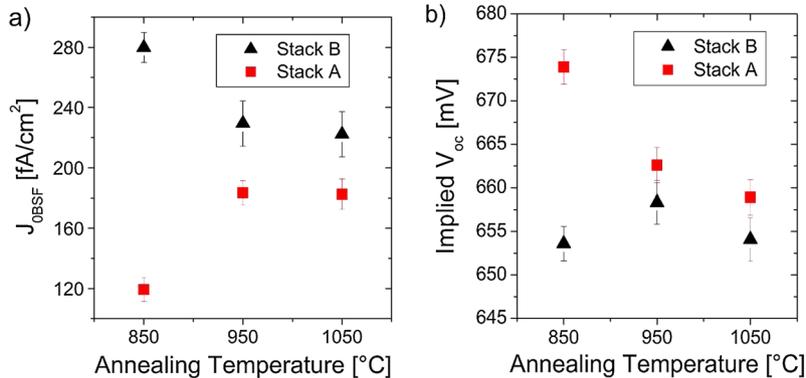


Figure 9. a) J_{0BSF} and b) implied V_{oc} measured on P implanted SiN_x/SiO₂/n⁺/n/n⁺/SiO₂/SiN_x samples annealed during 1 h at various temperatures.

Table I. Variation of the BSF R_{sheet} and of the contact resistivity on the P-BSF depending on the annealing temperature and passivation stack.

Anneal	Passivation	R_{sheet} [Ω/sq]	$\rho_{\text{contact BSF}}$ [$\text{m}\Omega\cdot\text{cm}^2$]
850 °C	Stack B	63 ± 1	5 ± 2
	Stack A	120 ± 4	25 ± 5
950 °C	Stack B	38 ± 1	5 ± 2
	Stack A	41 ± 1	4 ± 2

This explains the strong improvement of the $J_{0\text{BSF}}$ and of the Implied V_{oc} measured in this case (cf. Figure 9).

Al/Ag based metallization pastes were screen-printed on the implanted P-BSF annealed at 850 °C and 950 °C and passivated by stacks A and B. After an IR-firing step in a belt-furnace, the contact resistivity was measured by the Berger method on these samples [19]. Results are shown on Table I along with the sheet resistance measured on each BSF. R_{sheet} and $\rho_{\text{contact BSF}}$ are similar for each passivation stack at 950 °C while a strong increase of both parameters is observed at 850 °C in the case of stack A.

Due to the difficulties to contact the P-BSF with the stack A at low annealing temperature, stack A was kept for solar cell fabrication only in the “co-anneal” approach where the phosphorus is activated at $T_{\text{p}} = 1050$ °C. Despite its lower quality, stack B was integrated in the “separated anneals” solar cells where the annealing peak temperature is lower ($T_{\text{p}} < 900$ °C). The resulting BSF, named BSF_B, corresponds to a more concentrated and thinner BSF than the BSF_A formed in the co-annealed approach (see Figure 8).

3.3. N-type PERT implanted solar cells results

Table II shows the Illuminated I–V parameters measured on solar cells fabricated by both “separated anneals” and “co-anneal” processes with batches of 15 cells. Based on symmetrically textured Cz 156 mm wafers, they were measured on a reflective gold plated chuck and calibrated with a solar cell certified by Fraunhofer ISE CalLab. An average efficiency of 19.7% was measured with the “co-anneal” approach, and an average efficiency of 20.2% in the “separated anneals” case. These results demonstrate the possibility to exceed an efficiency of 20% and a V_{oc} of 650 mV by using SiO₂ passivation and conventional screen-printing grids on bifacial n-type PERT cells. Similar V_{oc} and uniform J_{sc} of 39.1 mA/cm² were measured for both processes. The main difference remains in the value of the FF, which is lower in the case of the “co-anneal”.

Table II. Average I(V) performances of implanted n-type PERT solar cells.

Cell type	iV_{oc} [mV]	V_{oc} [mV]	J_{sc} [mA/cm ²]	FF [%]	η [%]
Separated anneals	667	651.5	39.1	79.1	20.2
Co-anneal	671	650.6	39.1	77.3	19.7

Implied V_{oc} (iV_{oc}), measured before screen-printing steps, exhibit a higher potential for the co-anneal process (cf. Table II). This is in agreement with results obtained on n⁺/n/n⁺ samples where a higher BSF quality was measured at 1050 °C using the passivation stack A than at lower temperature with stack B. However after metallization the drop of V_{oc} is slightly stronger in the case of the co-anneal process, resulting in similar V_{oc} values for both processes.

Spectral responses were performed on both types of solar cells to measure the external quantum efficiency (EQE). The EQE curves and the reflectivity were both measured between the metallization grids (cf. Figure 11). For a better clarity, only the reflectivity of the “co-annealed” process is shown in Figure 11 as the curves were identical for both processes. Despite the difference in the BSF annealing temperature and in the passivation stack, the two different cells resulted in similar EQE curves with the same response for both BSF (BSF_A and BSF_B).

Further characterizations were made to understand the FF gap between the two processes. Dark I–V curves were measured in order to extract the dark shunt resistance (R_{shunt}). Suns- V_{oc} measures were also made to determine the PFF of the solar cell as well as the saturation current density of the second diode (J_{02}) and the series resistance. Series resistances (R_{s}) were calculated by comparing the Suns- V_{oc} and the illuminated I–V curve as described by D. Pysch in [20]. Finally the contact resistivity was measured by the Berger method on both BSF [19]. Results of these measurements are summarized in Table III.

On one hand, a higher series resistance was measured on the “co-anneal” cells. This was explained by a higher contact resistivity on the BSF_A than on the BSF_B. On the other hand, the PFF shows a drop for the “co-anneal” case similar to the drop of the FF and so seems to be the main parameter that drives the FF. It is well known that the PFF can be limited by both the R_{shunt} and the J_{02} value. The R_{shunt} shows a similar value for both processes but J_{02} is one order of magnitude higher in the “co-anneal” case. In conclusion, the main limitation of the “co-anneal” solar cells, with its deep phosphorus BSF, is an especially low PFF due to a deteriorated J_{02} .

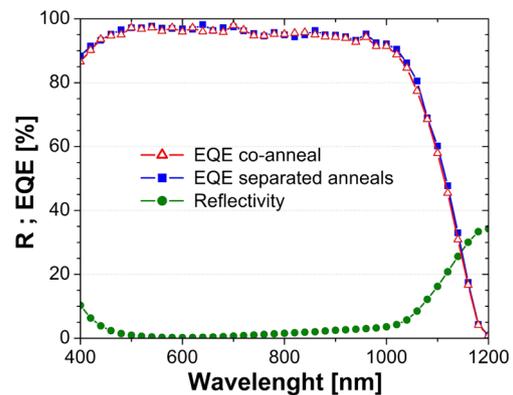
**Figure 11.** Reflectivity and EQE results of each process.

Table III. R_s , R_{shunt} , $\rho_{contact}$ BSF, PFF and J_{02} of implanted n-type PERT cells.

Cell type	R_s [$\Omega \cdot \text{cm}^2$]	$\rho_{\text{contact BSF}}$ [$\text{m}\Omega \cdot \text{cm}^2$]	PFF [%]	R_{shunt} [$\text{k}\Omega \cdot \text{cm}^2$]	J_{02} [nA/cm^2]
Separated anneals	0.60	4.8	83.5	170	2.3
Co-anneal	0.75	17.8	81.9	140	19.0

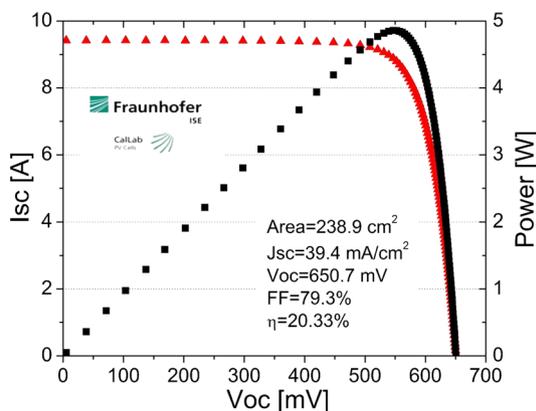
Table IV. Variation of the different parameters after the laser edge isolation of the solar cells.

Cell type	ΔV_{oc} [mV]	ΔJ_{sc} [mA/cm^2]	ΔFF [%]	$\Delta \eta$ [%]	ΔR_s [$\Omega \cdot \text{cm}^2$]	ΔPFF [%]	ΔJ_{02} [nA/cm^2]
Separated anneals	-0.7	+0.2	+0.4	+0.2	-0.17	-0.1	+1.8
Co-anneal	-0.6	+0.2	+0.6	+0.2	-0.21	+0.0	+1.0

The impact of the edges of the solar cell on the PFF and J_{02} values was studied by measuring the solar cells performances before and after the isolation of the edge by laser irradiation (cf. Table IV). For the two processes, even if a small increase of the FF is measured after the laser edge isolation, no variations were observed in the PFF values. The FF increase was only due to a decrease of the series resistance. The absence of improvement of the J_{02} values after the edge isolation show that the high J_{02} measured on the “co-anneal” process in Table III isn’t related to shunt effect that could have occurred at the edge of the cell.

To conclude, the high J_{02} value seems to be due to stronger impact of contaminations induced by screen-printing paste on the less concentrated BSF_A compared to the BSF_B. This explanation was supported by the higher drop of V_{oc} measured after metallization in the “co-anneal” process.

Finally further optimizations on the screen-printing step were performed, leading to the reduction of the front metal shading from 6.6% to 6.1% thanks to narrower finger

**Figure 12.** I(V) curves of the separated anneal solar cell certified by F. ISE CallLab at 20.33%.

widths. Following this optimization, the high efficiency potential of the “separated anneals” solar cells was confirmed by the certification of one of the solar cells by the Fraunhofer ISE CallLab. The solar cells efficiency was measured at 20.3% as shown on Figure 12.

4. CONCLUSION

One of the simplest processes for the fabrication of bifacial n-type PERT solar cells is based on a single high temperature annealing (“co-anneal”), to activate at the same time the implanted boron emitter and implanted phosphorus BSF, and the use of this annealing to grow the SiO₂ passivation layer. Considering implantation doses compatible with low contact resistances by usual screen-printing metallization pastes, it has been demonstrated that only the highest investigated thermal treatment with a peak temperature of 1050 °C offers a low emitter current saturation density J_{0e} . The use of this high temperature for the P-BSF anneal was beneficial in terms of implied V_{oc} potential due a more suitable BSF profile for improved passivation.

Despite the loss in J_{0e} due to the use of the SiO₂ passivation rather than a conventional Al₂O₃ layer, Implied V_{oc} above 670 mV were reached during solar cells fabrication. An average efficiency of 19.7% was obtained by our simple “co-anneal” process. The solar cells were mainly limited by a low PFF which seems to be reduced by a contamination effect of the rear screen-printing paste. This issue could be solved in the case of the “separated anneals” process flow where the P-BSF is annealed at lower temperature. In this case, a more concentrated and shallower P-BSF profile is obtained, leading to lower J_{02} and higher FF. This second process yielded an average efficiency of 20.2% on a 15 cells batch with only one added step as compared to the “co-anneal” case.

One prospect to further optimize the “co-anneal” process remains the reduction of the global thermal budget of this annealing in order to solve the weakly concentrated P-BSF issue. However this optimization should go along with a decrease of the boron implantation dose in order to keep a low J_{0e} value.

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