

# Function Learning with Carbon Nanotube-based Synapses

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The principle of using nanoscale memory devices as artificial synapses in neuromorphic circuits is recognized as a promising way to build new circuit architectures tolerant to defects and variability. Yet, actual experimental demonstrations of neural network type of circuits based on non-conventional/non-CMOS memory devices and displaying function learning capabilities remain very scarce. We recently showed that carbon-nanotube based memory elements can be used as artificial synapses, combined with conventional neurons and trained to perform functions through the application of a supervised learning algorithm [1].

This work is based on photosensitive carbon nanotube transistors called OG-CNTFETs (optically gated carbon nanotube FETs) that we studied in details first as photo-detectors and then as memory devices [2,3]. We then showed that these devices can be used as resistive memory elements [4] and proposed ways to implement them to store synaptic weights in neural network circuits [5,6]. The proposed implementation is ideally suited for the parallel learning of multiple functions in a crossbar array of OG-CNTFETs as shown by simulations [6].

At the experimental level, using devices not scaled down, we also showed that the same ensemble of 8 devices can be trained multiple times to code successively any 3-input linearly separable Boolean logic function despite device-to-device variability. This work represents one of the very few demonstrations of actual function learning with synapses based on nano-scale building blocks [1]. The potential of such approach for the parallel learning of multiple and more complex functions will be discussed. Finally we explored the scalability of

such strategy by evaluating programming speed [7] and size issues [8] in single-nanotube based devices.

Such use of 3-terminal devices as resistive memory elements, while powerful from a function learning perspective, also presents limitations in terms of ultimate scaling. We thus turned to the study of 2-terminal memristors incorporating carbon nanotubes (not as switching medium, but as nano-scale electrodes) [9]. In this presentation, the pros and cons of both approaches will be compared.

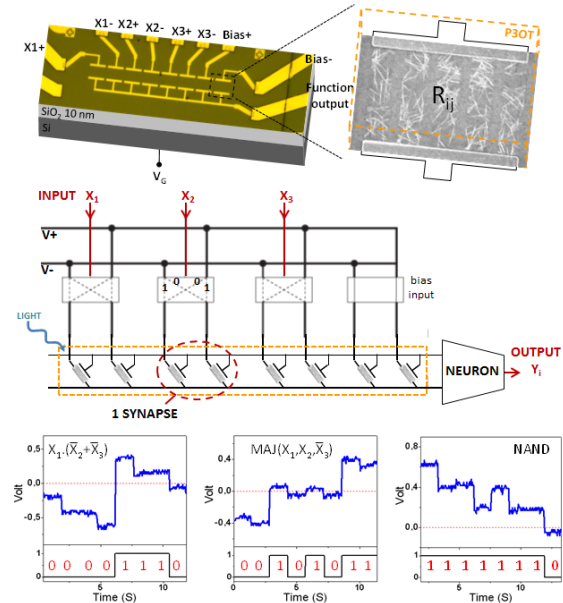


Fig. 1 (top) optical microscope image of a line of OG-CNTFETs based on carbon nanotube networks and SEM image of one such device. (middle) principle of the learning circuit with differential inputs and conventional electronics as neuron. (bottom) example of 3 particular 3-input logic functions learned successively by the same series of CNT-devices [1].

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- [1] K. Gacem et al., *Nanotechnology* **24**, 384013, (2013)
- [2] J. Borghetti et al., *Adv. Mater.* **18**, 2535 (2006)
- [3] C. Anghel et al., *Nano Lett.* **8**, 3619 (2008)
- [4] G. Agnus et al., *Adv. Mater.* **22**, 702 (2010)
- [5] W. Zhao et al., *Nanotechnology* **21**, 175202 (2010)
- [6] Liao et al, *IEEE Trans. Circ. Syst.* **58**, 2172 (2011)
- [7] G. Agnus et al., *Small* **6**, 2659 (2010)
- [8] D. Brunel et al., *Adv. Funct. Mater.* (2013), in press (10.1002/adfm.201300775)
- [9] Cabaret et al., *submitted*.

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