A novel insight of pBTI degradation in GaN-on-Si E-mode MOSc-HEMT

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***Abstract* — For the first time, ultrafast AC pBTI measurements are applied to GaN on Si E-mode MOSc-HEMT and compared to DC pBTI. Full recess Al_2O_3/GaN MOS gate is submitted to AC signals with various frequencies, duty factors and stress times. The degradation and relaxation characteristics are then modeled through a RC model combined to a CET map and fitted to experimental data. This map reveals the presence of two trap populations, also observed through ΔVth degradation kinetics. Acceleration factors (gate voltage and temperature) are estimated as well as TTF (Time to Failure) under AC conditions and show an extended lifetime compared to DC stress conditions. Finally dynamic variability is studied and indicates that our devices are ruled by normal distributions.**

***Index Terms* — pBTI, GaN on Si, E-mode GaN, AC pBTI, ultrafast pBTI**

I. INTRODUCTION

GaN-on-Si HEMT technology is now considered as a serious candidate for medium power applications (650V rated) [1,2] thanks to a combination of high breakdown field and high electron mobility. In the as grown material, buffer active defects are present in large numbers, inducing electron trapping during electrical stress resulting in the famous current collapse effect. Recently, current collapse free devices [2,3] have been demonstrated by fine tuning GaN on Si epitaxy as well as interfaces passivation. Buffer issues apart, gate instabilities and reliability are a major concern to increase lifetime of the transistors especially when submitted to high reverse bias stress ($V_{G,OFF}$ = 0V; $V_{DS,OFF}$ > 600V) and high forward gate voltage ($V_{G,ON}$ > 6V). Recent TDDB studies on E-mode p-GaN gate HEMTs [4,5] tend to show an important limitation in maximum ON-state gate voltage to ensure a 10 years lifetime at T = 150°C mainly due to a significant increase of the gate current at high V_G due to the p-GaN gate back to back diodes configuration. MIS gate structure is thus seen as a potential solution to overcome this maximum gate swing limitation. Nevertheless, in this very case, BTI degradation has to be assessed. This latter effect would severely impact the dynamic performance of the transistors over the time. D-mode MIS HEMTs, with either SiN or Al_2O_3 gate oxide, have been extensively studied through nBTI [6] and pBTI [7,8,9] studies and has shown a strong Vth shift related to border traps and oxide bulk traps. An advanced E-mode MOSc-HEMT (MOS-channel-HEMT) configuration [10,11] has recently been introduced on 200mm GaN on Si wafers and submitted to harsh gate conditions aging [12]. So far only DC BTI measurements have been reported while these transistors are supposed to operate only in AC conditions for ON-state mode. In addition, slow measurements (> 1ms) are generally reported which tend to modify the actual Vth drift during the stress phase. In this paper we present for the first time a comparison between AC and DC stress combined with ultra-fast pBTI measurements (< 10µs) on GaN-on-Si E-mode MOSc-HEMTs embedding an Al_2O_3 gate oxide.

II. DEVICE DESCRIPTION AND EXERIMENTAL SETUP

A. Device description

200mm GaN-on-Si wafers were grown using metal organic chemical vapor deposition (MOCVD). A structure consisting of "Transition Layers" is grown directly on a 1mm thick lightly doped (~ 10 Ω.cm) p-type Si substrate. A Carbon doped GaN (GaN:C) layer is then grown on top to ensure electrical insulation between the substrate and the top active layer while improving GaN breakdown voltage, and the GaN growth is finished with a thin unintentionally doped GaN layer (GaN:UID) which forms the channel. Next, a 0.6nm AlN spacer is grown, followed by a 24nm AlGaN barrier (25% in Al content) to form the 2DEG (2-D Electron Gas) at the GaN interface, before a final 5nm in-situ SiN passivation layer is grown. Fig.1 shows a schematic of the gate stack in the MOSc-HEMT configuration. The AlGaN barrier is removed by ICP RIE etching and GaN is recessed until depth reaches 35nm to cut the 2DEG. Finally, a 30nm ALD Al_2O_3 gate oxide is deposited on the etched cavity. TEM cross section (Fig.1) illustrates the full recess configuration where sidewalls are now a part of the electron conduction path under the gate.

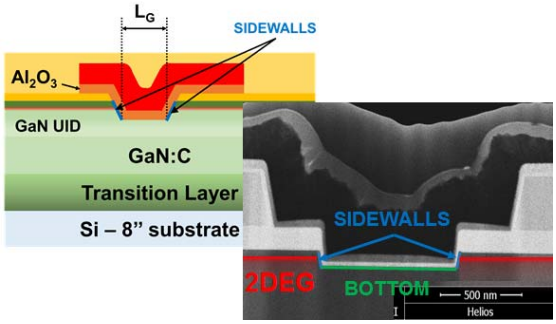

Figure 1. Schematic of the GaN-on-Si E-mode MOSc-HEMT gate stack and TEM cross section of a 0.5 µm long recessed gate.

The nominal width of the tested devices is set at 100µm to limit the measured current to 10mA with L_{GD} = 15µm, L_{GS} = 2µm. Fig. 2 demonstrates the E-mode (Vth>0V) operation for different gate length from L_G = 2µm down to 0.5µm. Vth is extracted at a fixed current level of $I_D = 10^{-5}$ A/mm.

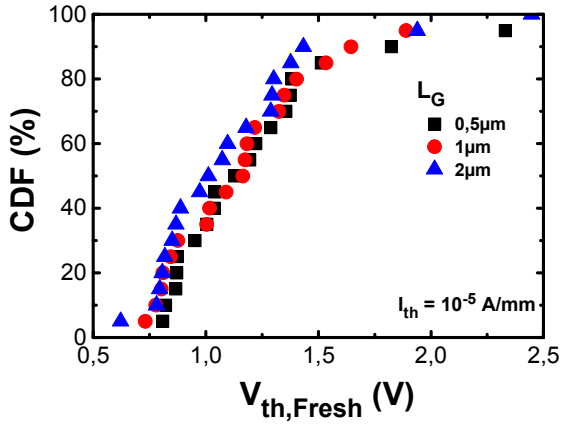

Figure 2. Cumulative distribution function of Vth for different L_G (0.5, 1 and 2µm) confirming the E-mode operation (Vth > 0V). Drain voltage is set at V_D = 0.1V.

B. Experimental setup

The principle of the fast pBTI technique under AC stress is highlighted in Fig.3 and is similar to the one used for [13]. A Keysight B1500 with ultrafast SMUs (B1530) is used to pulse the gate down to 100ns between two V_G values (0V for low state and +4V to +8V for high state). pBTI stress is applied at a given frequency (f = 100Hz to 1MHz) with a defined duty factor (DF = 1% to 99%) at a fixed $V_{G,Stress}$. A fast $I_D(V_G)$ (<10µs) is performed to record the ΔVth during the stress phase while minimizing the Vth recovery during a measurement phase. Consequently Vth recovery is measured with the same fast V_G ramp from 1µs to 100s at V_G = 0V. Note that V_D = 0V during stress & recovery phases while is fixed at 0.1V during fast $I_D(V_G)$ measurements. From the pattern in Fig.3, it is possible to study ΔVth drift as a function of DF, frequency or total stress time ($t_{Stress,max}$).

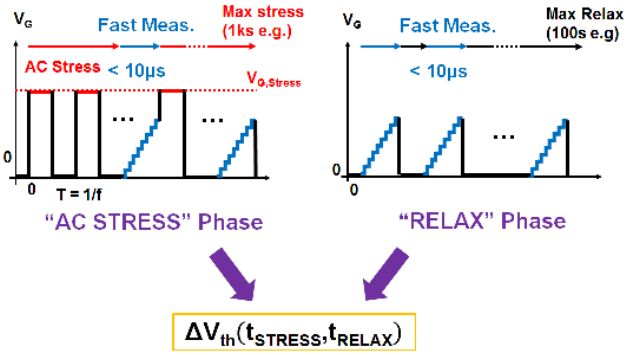

Figure 3. Principle of the AC pBTI measurement with ultra-fast Vth measurements minimizing unwanted Vth relaxation during the stress.

Fig.4 illustrates the influence of the $I_D(V_G)$ measurement time during a pBTI stress sequence. If the measurement is not fast enough (>10µs), unwanted relaxation can occur and consequently minimize the actual Vth drift in the device. This would lead to misinterpretations, especially for Time to Failure (TTF) extrapolation. Measurement time has been limited to 10µs in this study to minimize this effect.

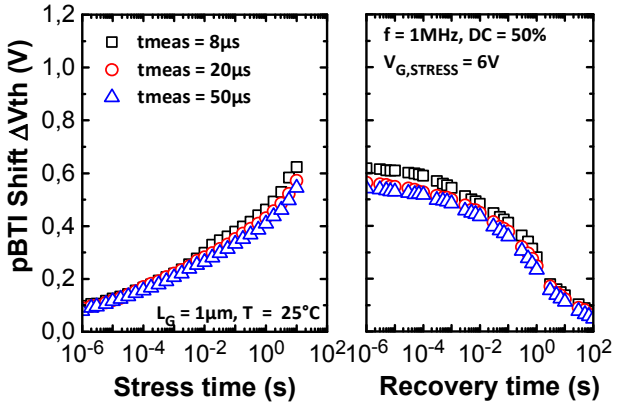

Figure 4. AC pBTI stress and recovery characteristics as a function of the $I_D(V_G)$ measurement time. L_G = 1µm and T = 25°C for this measurement.

III. DC VERSUS AC STRESS PBTI

Fig. 5 shows the pBTI stress and recovery transients for f = 100Hz to 1MHz at DF = 50% and $V_{G,Stress}$ = 7V compared to the DC stress case. A very large difference is observed comparing AC and DC stress, furthermore the ΔVth tends to increase with the frequency of the AC signal as already reported in Si CMOS technologies [13]. This dependence is related to the fact that the AC gate signal ends up with a low state (V_G = 0V) which enables the relaxation of defects compared to DC stress. This frequency effect will limit the actual Vth drift in GaN power transistor operating for instance at 100 kHz. Shape of the degradation AC pBTI shift is not monotonous and exhibits two regimes with a transition around t_{Stress} = 4-5s which might be related to multiple oxide trap populations.

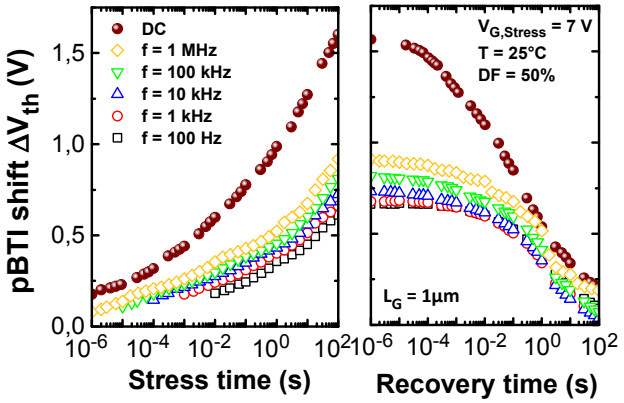

Figure 5. AC pBTI stress and recovery characteristics as a function of the signal frequency at DF = 50%. Filled symbols represent the DC pBTI case. L_G = 1µm and T = 25°C for this measurement.the stress.

The duty factor DF also modifies the Vth drift (See Fig. 6 plotted at a stress time of 100s under 10kHz AC stress). The S-curve behavior predicted by [15] is also found for our devices. Nevertheless, the global behavior differs from Si technologies where AC/DC Vth ratio tends to "0" for very low duty factor (< 1%) and to "1" for high duty factor (> 99%). Low DF induces

a significant degradation compared to DC case (~0.25) meaning that very fast capturing and slowly emitting traps are present in the devices ($\tau c/\tau e << 1$) for capturing time below $\tau c < 10\mu s$. Furthermore, the S-curve is centered on 0.55 for 50% DF, which accounts for a rather symmetrical defect distribution around $<\tau c> = <\tau e>$ (DF = 50%). It is expected to gain at least a factor 2 on the ΔVth for a fixed stress time. Fig. 6 also highlight that gate length L_G has merely no influence on these normalized S-curves, implying similar traps characteristics even for short gate length.

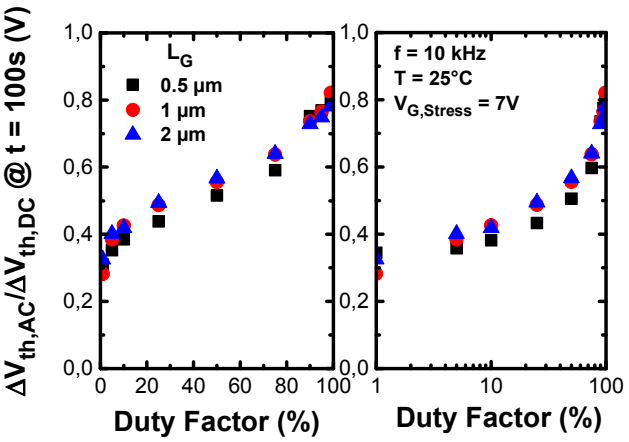

Figure 6. Variation of normalized $\Delta Vth_{AC}/\Delta Vth_{DC}$ degradation extracted at 100s with DF. No difference with respect to gate length is observed. Vg = 7V and f = 10kHz here.

For a recoverable degradation with a single oxide trap population, BTI modeling [14] foresees ΔVth to follow the model:

$$\Delta Vth = C_R . V_G^{\gamma} . exp\left(-\frac{qE_A}{k_B T}\right) . ln\left(1 + \frac{\tau c . t_S}{\tau e . t_R}\right) \qquad (1)$$

where C_R is a constant, γ is the voltage acceleration factor, E_A is the activation energy of the oxide traps, τc and τe the average time constant of the oxide traps inducing a recoverable degradation. Finally, t_S and t_R represent the stress and relaxation time used in the measurement.

Thus, it possible in the case of a single recoverable degradation, to normalize pBTI shift as a function of the t_S/t_R ratio for multiple t_S values. Figure 7 presents this approach for our 1µm long devices under a $V_{G,Stress}$ = 7V at f = 1MHz and DF = 50%, the redline representing the law (1). By plotting the recovery transients $\Delta Vth_{recovery}$ as a function of the maximum stress time vs recovery time ratio ($t_{Stress,max}/t_{recovery}$), we show a deviation from the analytical normalization. It suggests that our degradation is not related to single recoverable trap population but that multiple traps must be considered to understand BTI degradation in MOSc-HEMT devices.

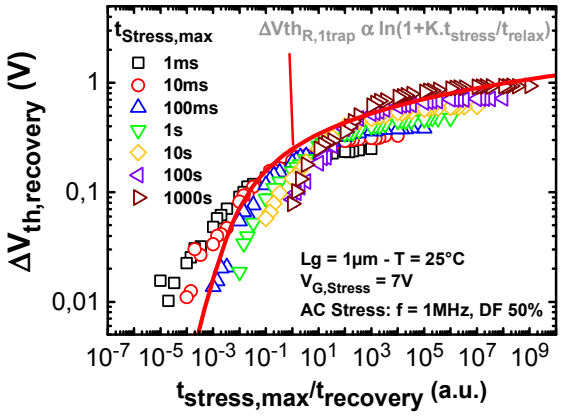

Figure 7. Recovery transients after an 1MHz AC stress plotted as a function of $t_{stress,MAX}/t_{recovery}$ showing no normalization, sign of multiple traps populations. $V_{G,Stress}$ = 7V and L_G = 1µm here.

IV. AC PBTI MODELING

To understand the degradation kinetics of our gate stack, we use a "RC model" combined with a CET (Capture Emission Time) map proposed in [13,15]. Fig. 8 illustrates the principle of the RC model where the oxide traps are modeled by a RC parallel network.

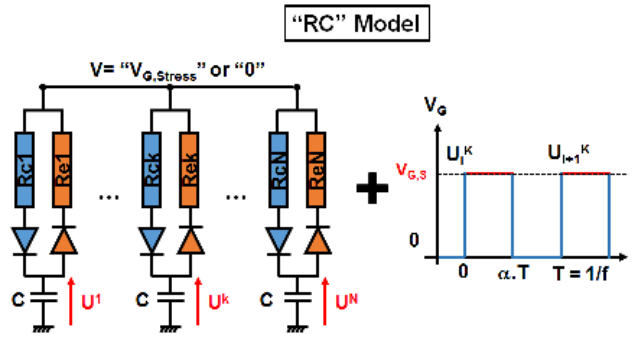

Figure 8. Schematic of the RC network used BTI modeling [13,15]. Each traps is represented by a combination of a capacitor C and by two resistances Re and Rc to set emission and capture time respectively. In the case of AC BTI, this circuit is studied under a Vg signal given by the chronogram (right) which gives access at the capacitor voltage U(t) after a given number of cycles.

For general AC signal ending with a relaxation phase (our case here), it is possible to have access to the voltage U after n stress cycles:

$$U_{n,low} = V_G \left[1 - e^{-nT.\delta}\right] . \frac{e^{-T.\beta} - e^{-T.\delta}}{1 - e^{-T.\delta}} \qquad (2)$$

where $\delta = \alpha\backslash\tau c + (1-\alpha)/\tau e$ and $\beta = (1-\alpha)/\tau e$. α is the duty factor in this analysis. τc and τe the average time constant of the oxide traps while V_G is the stress voltage applied on the gate during high state AC phase.

This RC model can be combined with a "CET" (Capture Emission Time) map which represents a traps occupancy map and giving a normalized traps density g(τc,τe) between 0 and 1. It enables the calculation of ΔVth as a function of t by summing the filling state of each traps "i":

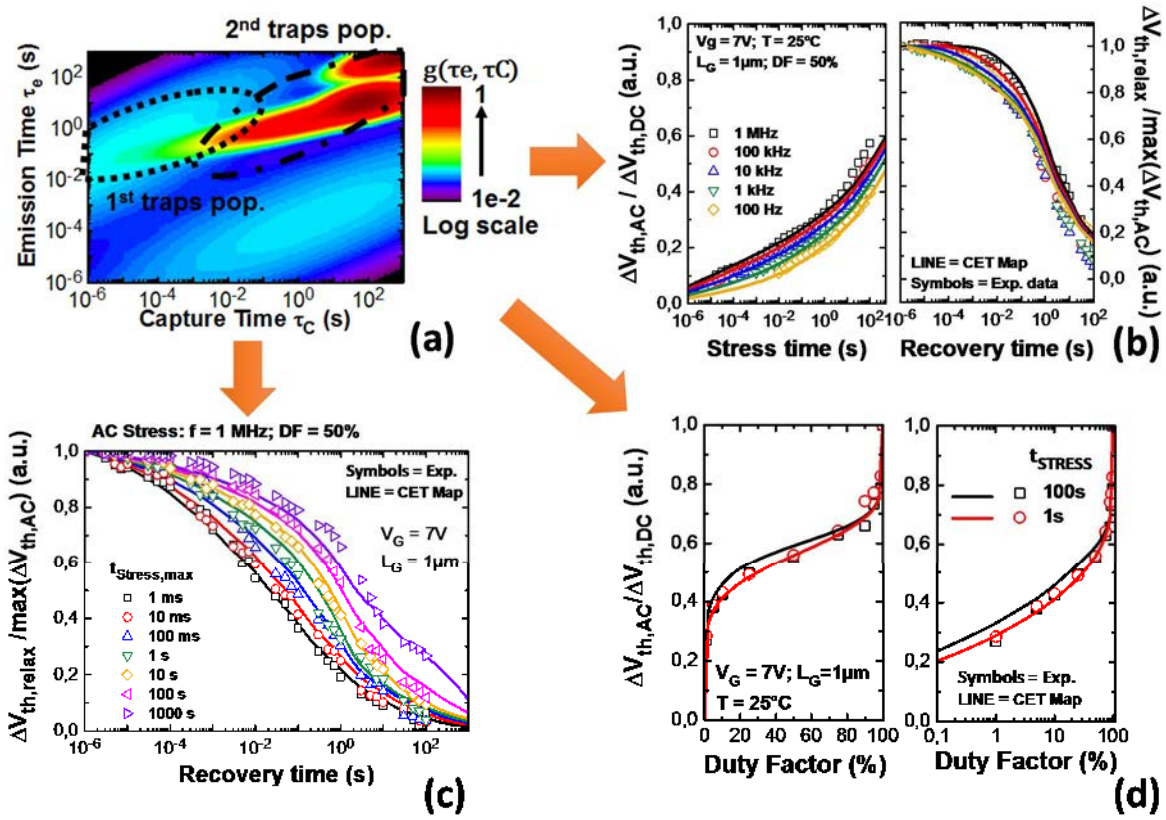

Figure 9. (a) Capture and Emission Time (CET) map giving the traps density g(τc,τe). This map shows two population, one for short time degradation and a second one for long time degradation with a very specific emission time around 4-5s. Comparison of experimental and modeled ΔVth (b) stress and recovery for increasing frequencies, (c) ΔVth recovery after increasing AC stress time (1ms to 1ks) and (d) ΔVth AC/DC degradation ratio as a function of DF.

$$\Delta Vth(t) = K.\sum_{i=1}^{N} g(\tau_c^i, \tau_e^i).U^i(t) \qquad (3)$$

where K is a technological constant and τe, τc, U the previously defined traps parameters. The CET map used to reproduce experimental data is presented in Fig. 9. , reproduces well several features of the experimental ΔVth degradation and recovery phase for our transistors. Frequency dependence at DF = 50% (Fig. 9.(b)) as well as ΔVth relaxation as function of total stress time (Fig. 9.(c)) under $V_{G,Stress}$ = 7V at f = 1MHz and DF = 50% are fitted with accuracy, providing a validation of our CET map in the case of τe > τc. The second part of the map (τe < τc) can be assessed by fitting the AC/DC S-curves (Fig. 9.(d)) as a function of the duty factor DF, which has been done at two stress times (1s and 100s). It can be seen that two trap populations have been used to fit our data. A first one at short capture time and moderate emission time, while a second one is used to model the long term degradation and relaxation transients observed experimentally between 1 and 100s. Still, no permanent degradation were considered here because every relaxation characteristics tend to reach 0 and no permanent degradation has been observed for measurements done a week after this study (not shown here). This CET map can be used to extrapolate a degradation or a recovery time for a given V_G (here 7V). TCAD simulations were performed to estimate the electric field distribution around the recessed MOS gate. Fig. 10 shows the simulated E-field undergone by the Al_2O_3 gate oxide (30nm here) in the recess configuration cited in section II.A. The electric field modulus represented in color scale indicates a uniform distribution all along the bottom part of the gate. However, non-uniformities appear at the gate corners and sidewalls, which would potentially lead to a different Vth degradation in these regions.

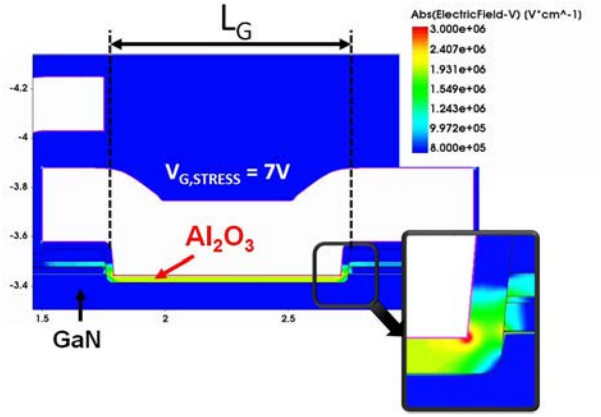

Figure 10. TCAD simulation of electric field distribution under $V_{G,Stress}$ = 7V on 30nm Al_2O_3/GaN MOS gate stack including gate field plate and GaN-UID recess introduced in section II-A. Gate length is set at L_G = 1µm here. Whiteout areas are related to metalic materials.

It has to be noted that these TCAD simulations do not embed the evaluation of interface traps which would be different in the sidewalls compared to the bottom of the etched cavity and thus imply a different Vth in these two regions.

This CET methodology provides a precise tool to deeply understand the degradation of our gate oxide in the case of fully recessed MOS gate where some fast degradations can occur and how the device would behave in AC mode which represents the actual operation when integrated into applications. Here the CET map has been evaluated at a given $V_{G,\,Stress}$ = 7V but must be reconsidered, or at least checked, when stress voltage is modified. Of course this approach does not take into account the ΔVth induced by an OFF state stress ($V_{G,OFF}$ = 0V; $V_{D,OFF}$ > 600V) and should be tested afterwards.

V. ACCELERATION FACTORS

The previous section allows us to revisit results established for standard DC stress. Besides, the classical voltage and temperature dependence have to be readapted in the case of GaN MOSc-HEMT technology. The voltage acceleration factor γ (see (1)) has been extracted for a 1µm gate length transistor at different stress times (1ms, 1s and 100s) under a 100kHz AC stress (DF = 50%) (see Fig. 11-left). Generally constant for high reliability CMOS technology, this factor varies here as a function of the stress time which clearly shows the two trap populations are not filled identically with V_G and that the CET map is not unique (to be recalculated for each $V_{G,Stress}$). Short capture time traps are more easily filled when V_G increases while the long capture time traps tend to be less sensitive to V_G. The activation energy of the ΔVth drift has been extracted (Fig. 11-right) and shows a constant value around Ea = 85meV as a function of the stress time, indicating that the 1st trap population of the CET map tends to governs the temperature dependence of the degradation.

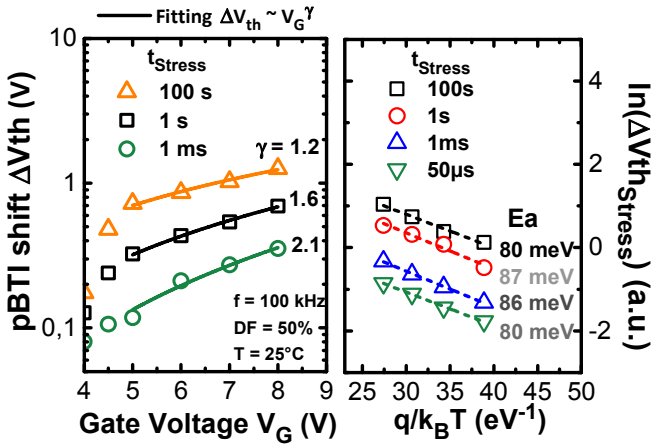

Figure 11. Voltage acceleration factor evaluation under AC stress (left) and activation energy extraction (right) extracted on MOSc-HEMT technology. Frequency is set at 100kHz to be close to operating conditions.

Time to Failure (TTF) is presented on Fig.12 for two criteria on ΔVth (0.3 and 0.75V) as a function of V_G for DC and AC stress (f = 100kHz, DF = 50%). It is pointed out that two different V_G dependence exist following the criteria. This latter effect can be related to the variation of γ with stress time (Fig. 11-left) because low ΔVth is achieved in the first regime of the Vth degradation spectrum, i.e. at low stress time as thus related to a high acceleration factor, whereas high ΔVth criteria is associated with the second regime that appears for stress time > 4-5s (see Fig. 5) which is correlated to lower γ. Meanwhile, for large $V_{G,stress}$ the TTF is considerably extended when HEMTs undergo an AC gate pattern. Plus, at low V_G, TTF tends to diverge from the standard DC power law (eq. (1)), which is consistent with the drop of γ observed at low voltage ($V_{G,Stress}$ < 5V) on Fig.11-left.

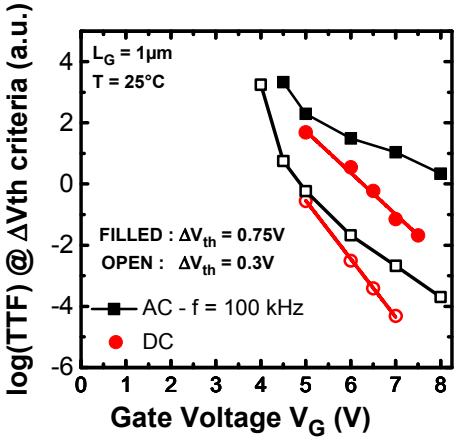

Figure 12. Time to Failure versus gate voltage at two criteria (0.3 and 0.75V) emphasizing the gain in lifetime under AC stress conditions.

VI. DYNAMIC VARIABILITY

Dynamic variability has also been studied (Fig. 13 & 14) at wafer level. Fig. 13 depicts that ΔVth follows a normal law generally expected for large area devices (Probability Distribution Function is a Gaussian in this case) and that standard deviation for ΔVth distribution increases all along the AC stress phase.

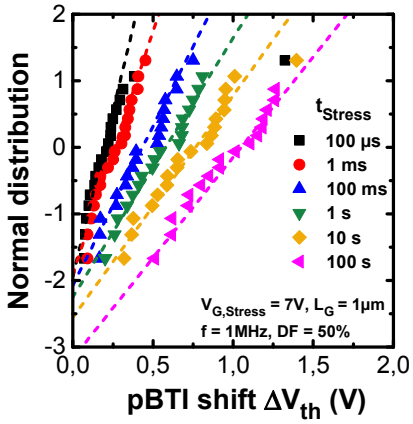

Figure 13. ΔVth distributions after increasing stress time. Normal law catches the behavior. V_G = 7V and L_G = 1µm here.

This feature is in agreement with a Poisson defect distribution in the gate oxide. Gate length influence on ΔVth distributions is presented on Fig. 14 extracted after 100µs and 100s of AC stress ($V_{G,Stress}$ = 7V, f = 1MHz and DF = 50%). Hardly no

difference between L_G = 0.5 and 1µm is observed which means that defect distribution is basically the same for both gate length. For L_G = 2µm on the opposite, a slight increase of the dynamic variability is observed, potentially due to a lower initial Vth distribution, which increases the gate overdrive $V_{G,ov}$ = $V_{G,Stress}$ - Vth and so the value of the electric field during the stress.

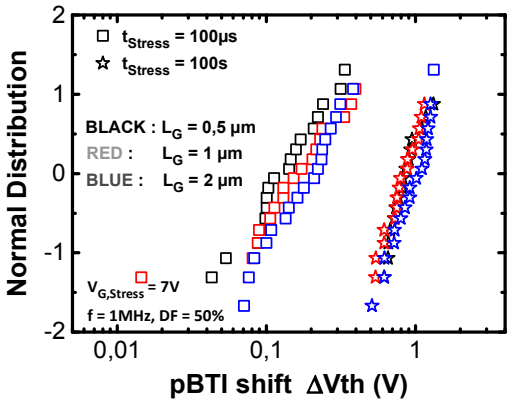

Figure 14. ΔVth distributions after two stress times (100µs and 100s). No visible difference is observed between 0.5 and 1µm gate length. f = 1MHz and $V_{G,Stress}$ = 7V here.

The strong standard deviation observed of the normal distributions used to fit experimental data indicates that this gate configuration must be optimized, whether in terms of material defectivity or through gate recessing uniformity all over the wafer. This is a key point to qualify the MOSc-HEMT technology for power applications, and to improve gate reliability of these promising devices.

CONCLUSIONS

A novel insight of the pBTI degradation of GaN power transistors has been presented allowing to assess the ΔVth shift during the actual operation of the device through AC stress phase and ultra-fast $I_D(V_G)$ characterization. CET map combined with an RC model enables to deeply understand the degradation kinetics of our devices. This methodology has been applied for the first time on E-mode GaN-on-Si MOSc-HEMT showing the presence of two trap populations in the oxide of the tested devices. Acceleration factors (voltage, temperature) have been extracted and tend to confirm the two degradation regimes. The Time to Failure is improved in the case of AC stress compared to DC stress implying an underestimation of this parameter in DC pBTI studies. The methodology presented in this paper has to be considered for the qualification of the MOS-c HEMT configuration and extended to assess the Vth degradation kinetics under harsh OFF state conditions (high V_{DS}, V_G = 0V).

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