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Phase-Change Memory: Performance, Roles and Challenges

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***Abstract*—In this paper we analyze recent progress in Phase-Change Memory (PCM) technology targeting both Storage Class Memory and embedded applications. The challenge to achieve a high temperature data retention without compromising the device programming speed can be addressed by material engineering. We show that volume and thermal confinement improvement of the phase-change material enables a high (10-fold) reduction of the programming current, achieved also by the optimization of the device architecture, in particular in the case of a confined structure. It leads to a higher cell efficiency proven by a 6x reduction of the programming current density wrt a standard PCM structure. Furthermore, we demonstrate the reduction of thermal losses by the tuning of the thermal conductivity of the dielectrics surrounding the phase-change material. Finally, we propose some considerations about the PCM ultimate scaling and the reliability at such dimensions, showing that the engineering of the bottom electrode/phase-change material interface can lead to a reduced variability in scaled devices.**

I. Introduction

Phase-Change Memory (PCM) is today the most mature among innovative back-end non-volatile memory technologies (NVM). Its recent commercialisation [1] to address stand-alone Storage Class Memory (SCM) applications demonstrates its advanced state in terms of industrialisation. In **Fig. 1**, we report the evolution along the last decade of the storage capacity (SC) of different embedded and stand-alone resistive memories [2]: PCM, up to now, has demonstrated the largest SC in both applications, confirming its high level of maturity [3]. PCM provides a wide set of interesting features such as fast read and write access, excellent scalability potential, and high endurance recently demonstrated up to $2x10^{12}$ programming cycles in highly confined PCM cells [4]. PCM technology is enough versatile to meet different applications' requirements [5]. We report here some recent progress in Phase-Change Memory technology in terms of data retention at high temperature and of programming speed. We show how current reduction can be addressed by phase-change material engineering, by cell architecture optimization and by thermal efficiency improvement of the device. Finally, the device scaling is discussed taking into consideration the reliability as an important target.

II. PCM High Temperature Data Retention and Programming Speed

Retention instability at high temperature has been the main challenge for PCM technology in the last decade, in particular to target Industrial and Automotive applications. Exploration and engineering of new alloys showed that PCM can retain the information up to temperatures higher than 200 °C. STMicroelectronics demonstrated the capability of a GeSbTe based material called "T-alloy" to grant a retention of one hour at 240 °C without data loss [6]. Being this result compatible with automotive specifications (~ 2 years at 150 °C) and soldering reflow thermal profile (peak temperature equal to 260 °C, according to JEDEC standard), it opens the way for PCM towards the embedded market. In **Fig. 2**, the retention performance for different phase-change materials reported in the literature [2] is put in correlation with the time required for the SET operation of the device (i.e. crystallization of the phase-change material). As a general trend, the higher the stability of the amorphous phase of the phase-change material, the slower and more energy consuming the recrystallization of the material becomes (i.e. longer SET time). Even if this correlation appeared insurmontable for many years, recently new classes of materials have been developed targeting at the same time data retention at high temperature and fast programming speed. Non-chalcogenide Ga-Sb-Ge alloys showed fast SET speed (~ 80 ns), excellent data retention (10 years at 220 °C) and solder bonding compatibility [7]. Moreover, the increasing interest in multilayered phase-change materials in order to explore new physics and new switching mechanisms in

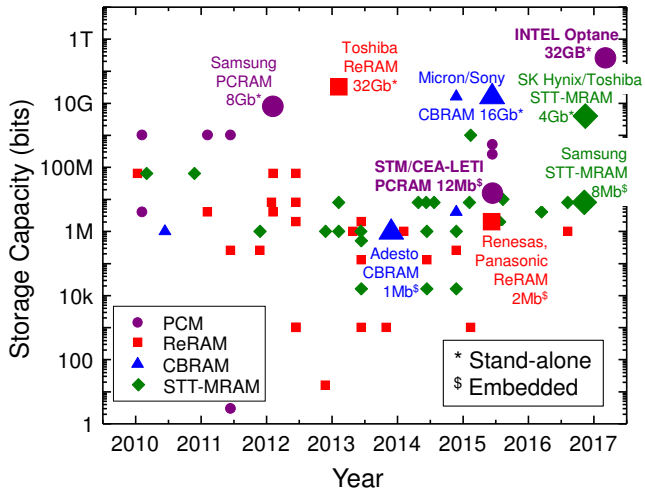

Fig. 1 Storage capacity evolution along the years of different embedded and standalone non-volatile resistive memory technologies [2]. Phase-Change Memory is today on the market as a stand-alone product with a storage capacity of 32GB [1] and it has been demonstrated in a test vehicle of 12Mb for embedded applications [3].

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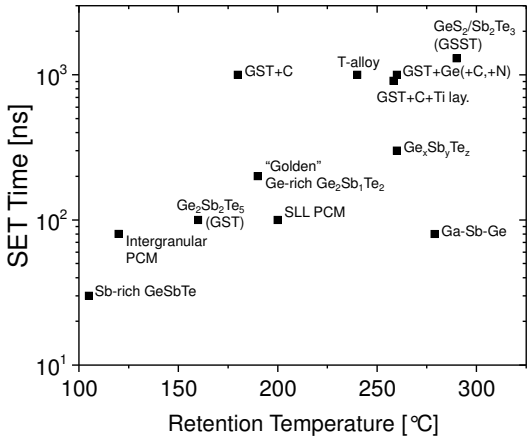

Fig. 2 SET time as a function of the retention temperature (to grant one hour of data retention) for different phase-change materials reported in the literature [2]. Material engineering showed the capability to achieve high temperature data retention up to almost 300 °C, at the expense of a lower SET speed. Some examples of innovative materials like non-chalcogenides (GaSbGe [7]) or superlattice-like (SLL PCM [8]) recently demonstrated the possibility even for PCM to target high programming speed still ensuring good retention performances.

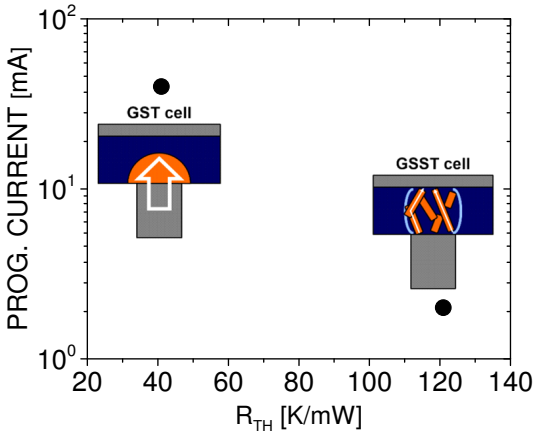

Fig. 3 Programming current as a function of the thermal resistance (R_{TH}) for PCM devices integrating standard $Ge_2Sb_2Te_5$ and optimized GeS_2/Sb_2Te_3 material (GSST) [12]. GSST composition shows a great reduction of the programming current (> 10x) thanks to the improvement of both the electrical and thermal confinement.

phase-change materials (e.g. phase change induced by charge injection instead of joule heating) led to the development of super-lattice like PCM (SLL-PCM) based on $GeTe/Sb_2Te_3$ periodic layers, featuring 18 hours of retention at 260 °C (not achievable by GeTe or Sb_2Te_3 single layers) preserving a SET speed of 100 ns [8].

A universal PCM suitable for both high temperature and high speed operations remains a big challenge. Indeed, PCM thermal stability relies on the magnitude of the activation energy of the crystallization, that results from the combination of crystals nucleation and growth phenomena, on which also the device programming speed relies. The nucleation and growth have to be hindered at storage temperatures (i.e. lower wrt the temperatures achieved during programming) in order to achieve good retention, while growth speed (mainly responsible for the SET operation speed) should be boosted, at the temperatures close to the melting one, to improve the device speed. Some recent material analyses, as an example, show that nucleation is almost absent in Sb-rich alloys [9], even if growth speed remains too high at low temperatures to prevent amorphous phase recrystallization that could be detrimental for the retention of the device. Material doping (i.e. C, N, O), on the contrary, was proposed to block grain growth and stabilize the amorphous phase.

These considerations suggest that even if a considerable material engineering has been done already in order to tune the device performance, recent findings, triggered by the strengthened interest in the PCM technology and in the phase change mechanism, after a trough of disillusionment, are opening new ways of optimization of the phase-change material.

III. PCM Current Reduction: Innovative Concepts and Optimization Challenges

Programming current reduction in PCM devices is fundamental to target high density memory products. This is due mainly to the reduction of the size of the selector element moving towards aggressive technology nodes. This problem has been addressed in standalone products (SCM) replacing the transistor selector with a back-end selector capable of higher current density, and scaling as much as possible the volume of the phase-change material in a so called 3D stackable architecture [1]. However, the increasing demand of data storage in low power portable applications still challenges PCM with charge based Flash memory making the current reduction a must for next generation of NVM.

Several solutions have been proposed to reduce the PCM programming current through the engineering of the phase-change material, such as using C doping [10, 11]. An other innovative approach relies on the reduction of the active volume of the phase-change material involved in the phase change transition [12, 13]. We demonstrated that the introduction of Sb_2Te_3 in a GeS_2 amorphous matrix (GSST) obtained by co-sputtering, leads to both an electrical (i.e. lower volume) and a thermal confinement improvement (i.e. a higher power efficiency) of the PCM device. It is shown in **Fig. 3** where we report the programming current as a function of the thermal resistance

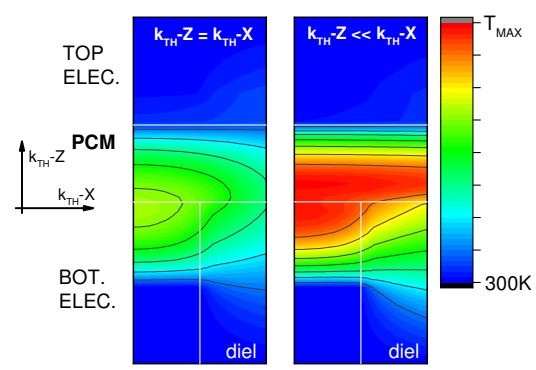

Fig. 4 Temperature profile for a fixed current density simulated in a device with a phase-change material featuring a symmetric thermal conductivity (left image, i.e. k_{TH}-Z = k_{TH}-X) and asymmetric (right image, i.e. k_{TH}-Z << k_{TH}-X). Same current density could achieve a higher and homogeneously distributed temperature at the bottom electrode/phase-change material interface in the "asymmetric k_{TH}" device. This allows a higher efficiency of the programming operations.

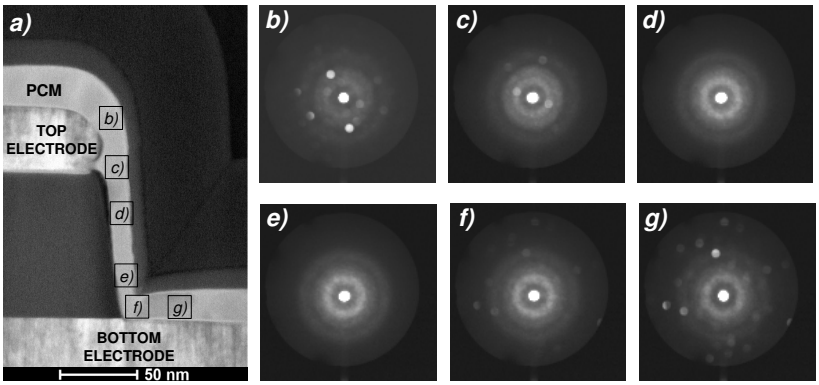

Fig. 5 Dark Field TEM image of a PCM "confined structure", where the phase-change material ($Ge_2Sb_2Te_5$) is deposited by PVD on the sidewall of the structure connecting the bottom and the top electrode (a). The device was programmed in the RESET state before the analysis. The nanodiffraction patterns acquired along the phase-change material show that the active region is well localized along the sidewall and it presents an amorphous phase (d,e), while outside of this region the material remains crystalline (b,c,f,g).

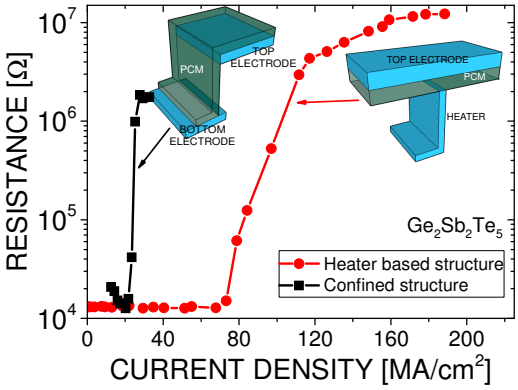

Fig. 6 Programming characteristics for a standard PCM device (heater based structure) and an optimized confined PCM. The current density reduction observed in the confined PCM, confirms the capability to achieve a better efficiency in a PCM device thanks to the cell structure engineering.

R_{TH} for both a standard $Ge_2Sb_2Te_5$ and a GSST based PCM cells.

Material engineering is not based only on alloy stoichiometry tuning, but also on new material arrangements such as SLL structures. New physical mechanisms are still under investigations in GeTe\Sb_2Te_3 based superlattice films such as topological phase transition [14] that could lead to strong current reduction since not based on joule heating of the phase-change material. However, new thermal properties can be involved in such layers that could lead to significantly reduce the programming current of the PCM device [15, 16]. In particular, the introduction of phonon scattering at interfaces between the layers along the current flow could break the thermal conductivity symmetry in the phase-change material creating a huge thermal confinement along the z-axis and a uniform thermalization along the x-axis of the cell. An electro-thermal simulation of such situation is reported in **Fig. 4**. In a standard phase-change material the symmetry of the thermal conductivity (i.e. k_{TH} uniform in the layer) leads to a temperature profile that is related to the geometry of the cell. In order to achieve the complete covering of the bottom electrode with an amorphised volume to program the PCM in its RESET state (high resistance state), a huge amount of material has to be involved in the phase transition, giving rise to the typical "mushroom" shape. On the contrary, an asymmetry in the thermal conductivity induced by a low k_{TH} along the z-axis of the PCM, can localize the phase transition at the surface between the phase-change material and the bottom electrode improving the efficiency of the cell. Indeed, a higher R_{TH} can be achieved leading to a higher temperature for an equivalent value of current density flowing into the device.

The PCM cell structure optimization is another way explored to reduce the programming current, in particular targeting the phase-change material volume and thermal confinement. We implemented an optimized PCM "confined structure" based on standard $Ge_2Sb_2Te_5$, in order to study the impact of both these confinements on the performance of the device. In **Fig. 5**, we report the TEM analysis performed on a RESET device, showing through the nanodiffraction patterns the strong localization of the amorphous region along the sidewall of the structure. The comparison between this structure and a standard one (i.e. based on a heater or bottom electrode), in terms of programming characteristics, is reported in **Fig. 6**, where the programmed resistance is monitored as a function of the programming current density. The 6x reduction of the current density needed to achieve the RESET programming in the confined structure, is significative of a higher efficiency of the device. Moreover, as soon as the injected current is capable to achieve the melting temperature in the phase-change material (i.e. in the middle of the sidewall as shown in Fig. 5), the active region can be fully amorphised at once. This can explain the abrupt transition between the SET and the RESET state, which appears on the contrary more gradual in the standard structure.

A better thermal confinement to reduce the RESET energy in PCM can be achieved preventing heat losses in the materials (i.e. dielectrics) surrounding the device [17]. In **Fig. 7** we report the programming characteristics for two $Ge_2Sb_2Te_5$ based PCM devices in which we integrated different encapsulation layers (i.e. the dielectric layer surrounding the phase-change material, as schematically described in the inset). The lower thermal conductivity of layer B wrt layer A allows a RESET operation at lower current (~ 30% of reduction).

IV. PCM Scaling and Reliability

Ultimate scaling of the PCM device has to deal with the preservation of the phase change mechanism that consists on very small atomic displacements that make possible the creation (and dissolution) of the resonant bonding typical of the crystalline phase (that once dissolved gives rise to a purely covalent system typical of the amorphous phase) [18, 19]. Demonstration of phase change capability in PCM was already achieved down to sub-10 nm scale [20]. However, the fact that the long-range order is crucial to achieve resonant bonding (i.e. crystallization) and that vacancies have a key role in the phase-change material structure stability,

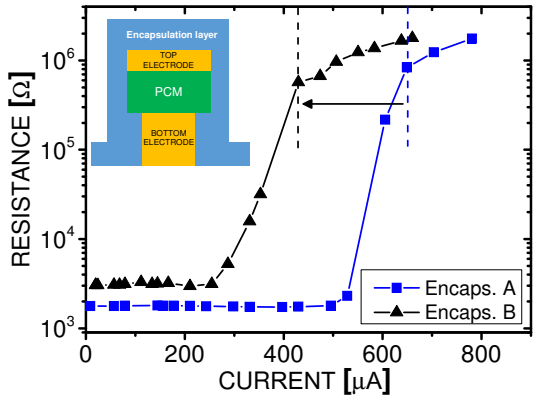

Fig. 7 Programming characteristics of two PCM devices integrating two different encapsulation layers. The devices integrating layer B show a RESET current reduced by ~ 30% compared to the ones integrating layer A (reduction highlighted by the arrow).

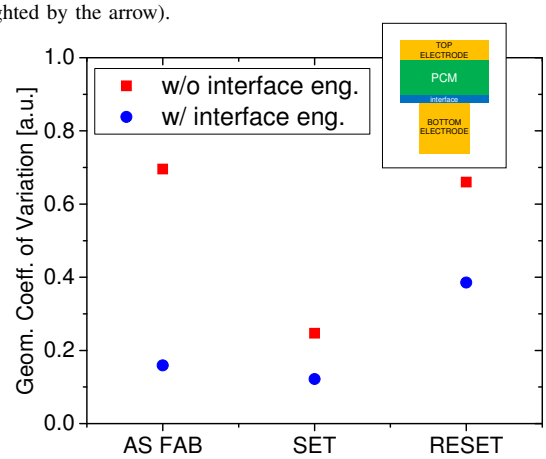

Fig. 8 Geometric coefficient of variation for the as-fabricated, SET and RESET resistances of two different population of PCM devices, w/ and w/o an optimized interface between the bottom electrode and the phase-change material. Less variability of the data is ensured by a proper engineering of this interface.

highlight the need of an increasing control of the material arrangement (i.e. down to atomic level) at smaller volumes [21]. Indeed, this has a direct impact on the memory yield. As an example, the reduction of the interface between the bottom electrode and the phase-change material (BE/pcm) in a scaled PCM device implies less atoms involved in the phase transition (amorphous/crystalline/melted). Therefore this interface can play a huge role on the final behaviour of the cells. In **Fig. 8** we report the result of an interface engineering performed on analytical $Ge_2Sb_2Te_5$ based devices. The as-fabricated PCM cells w/o interface engineering present already a higher resistance dispersion (i.e. higher geometric coefficient of variation) wrt the devices in which we optimized the BE/pcm surface. Moreover, this trend is preserved in SET and RESET resistance distributions after ~ hundreds of cycles. High endurance capability towards more than 10^{12} cycles is another challenge for PCM [4]. Atomic displacement, phase segregation and density change in the layer during cycling are detrimental for the preservation of the phase change mechanism. Recent works show that volume-change-free (i.e. in optimized GeTeN compounds [22]) and single-phase (i.e. in Sb-rich GeSbTe alloys [9]) amorphous-crystalline transition is achievable engineering the composition of the active material. Demonstration of the integration of these innovative alloys in ultra-scaled PCM will provide new insights on the failure mechanisms in PCM, enabling further optimization to address even DRAM endurance performances.

V. Conclusions

Phase-Change Memory already passed the step of being an emerging technology and today is playing a role in the market, in particular in Storage Class Memory applications. The strengthened interest and research/developement in this technology revealed the possibility to move further the frontiers given by the stability of the amorphous phase at high temperature, making PCM a valid candidate also for next generation of embedded applications. New phase-change alloys (e.g. non-chalcogenide materials) and new physics (e.g. in SLL structures) are under investigation and they are opening new roads towards current reduction, improved programming speed and ultimate scaling. This process of further optimization of the phase-change material in order to achieve high performance memory devices has to be supported by the engineering of the cell structure and of the materials surrounding the PCM. Indeed, with the increase of the surface-over-volume ratio in highly scaled cells, interfaces become more and more important for the energy efficiency of the cell and their interaction with the phase change dynamics. In a NVM arena where different innovative and standard Flash technologies are competing, and in a market context that is evolving and differentiating fast in terms of applications and storage needs, PCM has started a revolution of the memory concept and of the system architecture that already represents a real breakthrough.

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