# Solderless Leadframe Assisted Wafer-Level Packaging Technology for Power Electronics

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***Abstract* - This paper presents a wafer-level pre-packaging technology for power devices. The concept consists in the implementation of a thick 3D patterned copper leadframe ensuring the interconnections of the power devices among them or with the other components of the converter. The metallic leadframe is bonded between two wafers of semiconductor devices enabling the 3D power module integration by the 3D stacking of one or multiple switching cells. Specific technology developments are introduced, practical realizations of the concept are presented and the electrical characterizations of the first prototypes are discussed.**

**Keywords- 3D power module, wire bondless module, solderless module, power electronics, wafer-level packaging, die-level packaging, metallic leadframe, direct copper bonding**

## I. INTRODUCTION

The constantly growing needs of the power electronics industry are motivating recent researches and developments on faster and more efficient power devices that promise higher power density and efficiency [1]. At system level, an appropriate package for these devices is required to maximize the power converter performances. The main weak points of the standard packaging and interconnection technologies are the wire bondings on the topside contacts and the solder materials on the backside contact [2-4]. Offering an alternative solution for one or both, the top and backside contacts, is motivating recent developments and researches in power electronics packaging in order to improve the electrical, thermal, thermomechanical and EMC performances of the power modules. In addition, the packaging must maximize the reliability of the assembly. The deployment of wire bonding alternatives [5] or the development of new joining techniques and materials [6] are proposed to optimize the package characteristics but it remains difficult to improve all of the above mentioned packaging performance parameters at the same time.

This paper presents our work towards the improvement of power electronic devices packaging. The proposed concept consists in the implementation of a thick and patterned copper leadframe preparing and assuring the interconnections of the power devices of the switching cells among them or with the other components of the converter. The metallic frames are patterned with high precision perforations and pad landing areas which can have a different design on each side and can be used for contact and/or thermal exchange surface extensions. The thick and double side patterned copper leadframe is bonded between two semiconductor wafers, replacing the wire bondings by massive copper interconnections. No solder or other material is needed to assemble the metallic substrate with the semiconductor wafer(s) since a thermocompression bonding technique is developed and used in this case. Our approach is developed for a wafer-level integration allowing to benefit from reproducible and precise collective integration processes. Realizing the assembly at wafer-level allows to assemble multiple switching cells at the same time, making possible the 3D power module integration of multiple power devices used in interleaved converters or multiphase power conversion structures [7-8].

## II. CONCEPT

The concept is presented with the example of two stacked vertical power devices, corresponding to the high side and low side components of a switching cell. This approach, called the 3D switching cell stacking, based on the implementation of one device on top of the other, allows to optimize the interconnections between the two devices by minimizing the parasitic interactions compared to traditional packages. As presented in [9], the true 3D power device stacking allows to minimize the parasitic inductance of the switching cell as well as the common mode capacitance between the switching cell middle point and the ground. As a consequence, when considering the 3D stacking of two power devices, the increased assembly constraints must be addressed, especially in terms of reliability. Furthermore, the materials and the technological processes required for a 3D stack of power devices are extremely crucial as well as the power devices architectures. Fig. 1 shows a schematic view of a MOSFET based switching cell and a cross section of its physical implementation based on the 3D stacking of the two power devices.

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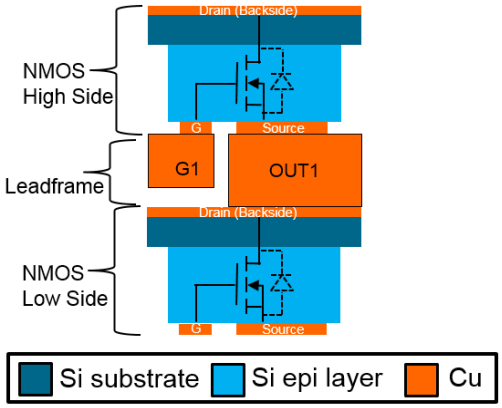



Figure 1. MOSFET based switching cell schematic and corresponding cross section of its 3D physical implementation

The resulting configuration is symmetrical but highly heterogeneous. A heterogeneous assembly may be an issue increasing the sensibility of the assembly to thermal cycling which may affect its reliability over time. However, in our case, the 3D assembly of the power devices and the metallic leadframe is realized by a solderless, thermocompression bonding step. No solder or other jointing material is needed to perform the bonding. Also, as mentioned above, our 3D switching cell stack is based on an almost perfect symmetry allowing to compensate the thermo-mechanical stress induced by the mismatch of the Coefficient of Thermal Expansion (CTE) between the copper and the semiconductor. Of course, local stresses are not canceled by the symmetric package architecture.

Another important issue when considering the 3D stacking of power devices concerns the proper interconnections of the front side electrodes of the high side switch. The switching cell middle point electrode and the Gate electrode must be isolated and accessible to be interconnected with the other components such as the gate driver. These interconnections assured by the metallic leadframe should not affect the edge termination of the high side power device in order to keep optimal its electrical performances. There are two possible solutions: either the metallic frame is patterned in 3D in order to raise the height between the frame and the planar terminations of the power device or the edge termination of the device should be adapted in order to remove the constraint as shown in [10] with the implementation of a vertical edge termination. Fig. 2 illustrates these two possible solutions that were investigated for the implementation of the proposed packaging technology and are discussed in the following sections.

After the wafer level bonding, the assembly of interconnected stacked wafers of components is diced revealing one or more already interconnected switching cells ready to be implemented and encapsulated to form a very compact and high performance single or multi-phase power module.

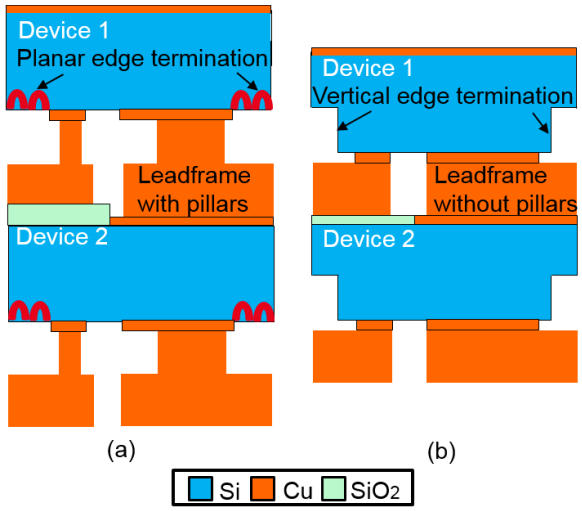



Figure 2. 3D Stacking of power devices (a) planar power devices with 3D metallic frame including large pillars and (b) stacking of vertical edge terminated power devices with planar metallic frame without pillars

## III. Design Considerations and Realizations

Die or wafer stacking relies on effective bonding technologies and adapted interconnections. Planar implementations based on wire-bonding are not suitable for the 3D stacking of dies because of the impossibility to provide access to the terminals of the components located inside the stack. Indeed, in true 3D stacks of voltage inverter switching cells, implemented with two identical bidirectional current power devices, such as N type Si or SiC MOSFETS or JFETS, the middle point power electrode as well as the high side power device gate electrode are trapped between the two dies as illustrated in Fig.1. The most efficient way to access those terminals is to insert a metallic frame between the two dies. Nevertheless, the challenge in this case relies on the ability to access and interconnect the Drain of the low side switch with the Source of the high side switch and to access and isolate the high side switch Gate electrode from the Drain of the low side switch. There are two possible solutions for that issue: the first one concerns the 3D patterning of the metallic frame in order to reach the pad areas of the corresponding power devices' electrodes. The second solution is to provide a specifically located electrical isolation with e.g. a $SiO_2$ thick layer. Both two solutions were explored for our 3D implementation.

### *A. The metallic leadframe at wafer-level*

A 4 inches, 400 µm-thick copper bulk substrate was used for the realization of the 3D patterned leadframe. Starting with a 400 µm-thick standard copper foil, we worked on it in order to define a round 4 inches wafer with both perforations throughout the thickness of the foil and relief patterns on both the topside (Fig. 3) and the backside of the copper wafer (Fig. 4). The final patterned leadframe including perforations is intended to be stacked and assembled between two wafers with SiC JFET power devices as represented on Fig. 5. As it

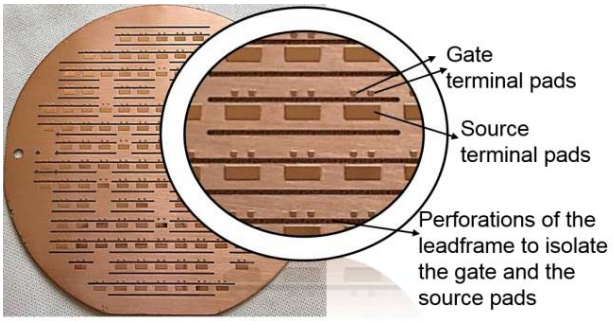



Figure 3. Front side of the copper leadframe including Gate and Source terminal pads

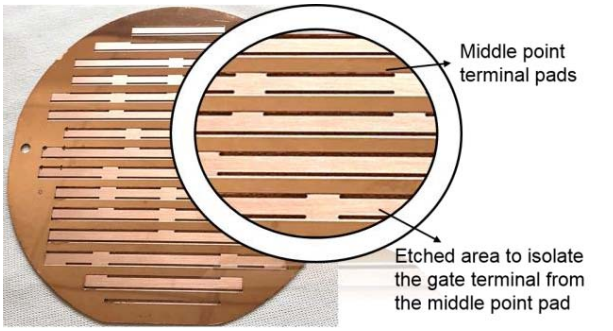



Figure 4. Backside of the copper leadframe with the middle point pads

can be seen on Fig. 3, flat cuts were included on two sides of the leadframe to assist the alignment of the wafers during the final assembly.

For the adaptability of the approach to any power device, we have made the choice to create the copper pillars on the metallic substrate and not on top of the devices. In such a way, the planarity of the interfaces to be bonded is guaranteed over the large wafer surface. Copper pillars with 50 µm height were realized by a chemical etching step on both sides of the metallic substrate. This height is required to cross over the edge termination of the high side device and to prevent this massive electrode from modifying the electric field distribution around the edge termination of the device (Fig. 2). Thanks to the pillars, high side and low side devices can be interconnected, even if their respective pad areas and regions are not exactly superposed. If there are several neighboring contacts, the leadframe is locally perforated to separate them (Fig. 4). In such a way, the Gate electrode of the high side switch can be separated from its source electrode as shown on Fig. 3. The perforations are also realized by chemical etching.

Four mask levels are required for the realization of the perforations and the pillars on both sides on the leadframe. One on each side is required to perform the perforation with the best possible resolution. The two other masks are required to define the pillars shapes and areas on both sides.

Once the metallic substrate and the two wafers of power devices are stacked and bonded together, the switching cells can be diced individually or per vectors or matrices of

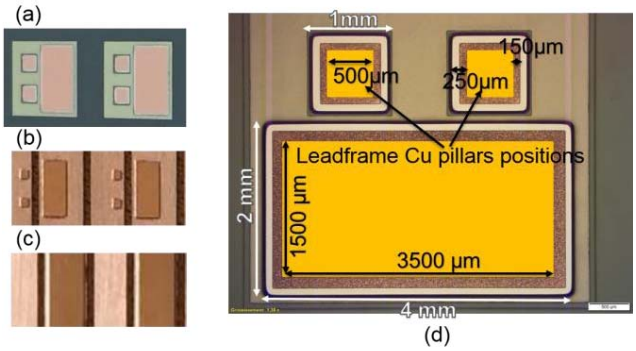



Figure 5. Details of the 3D assembly.(a) top-view photograph of the SiC JFET devices (b) top view photograph of the topside Cu leadframe (c) of the backside Cu leadframe and (d) top-view photograph of the SiC JFET with the future leadframe Cu pillars positions in yellow

several switching cells. If necessary, a passivation layer can be deposited.

The heterogeneous structure of the stack makes complex the dicing process. A special care for the design of the metallic substrate is required in order to simplify the dicing of the assembly by minimizing the copper dicing regions. After dicing the middle point electrodes are accessible on the edges of the 3D switching cell stack.

### *B. The metallic leadframe at die level*

The metallic leadframes can also be designed to interconnect two single or multiple 3D switching cells, a vector or a matrix of 3D switching cells. Die-level stacking is made after the dies have been diced individually or in matrices as it is presented in Fig. 6 below. The metallic leadframe is designed accordingly to interconnect pair of middle point electrodes. Fig. 6 presents two examples of metallic leadframes, one for a single switching cell 3D stack and one for a four switching cells 3D stack. As it can be seen on Fig. 6 the leadframes in this case are patterned with only perforations and no pillars. In order to assure insulation between the Gate and the middle point terminal of the high side device an insulation layer is deposited on the power

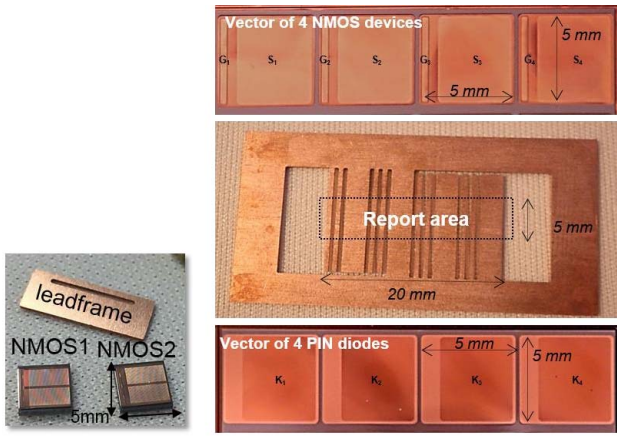



Figure 6. Photographs of the leadframes at die-level (a) for a single switching cell and (b) for four switching cells

devices as described in the following section. Once the 3D stack assembly is done, the frame edges are diced to separate each electrode. The 3D stack is then ready for further packaging stages – interconnection of the bottom, middle and top electrodes with the environment.

### C. *The power devices*

Specific devices have been designed and fabricated for the validation of the concept [11]. In order to allow the 3D implementation, Si NMOS and PIN diodes with large pad areas and specific contact architecture were manufactured. Copper material is used for the topside and the backside metallization of the devices required for the direct bonding process with the leadframe. Moreover, in our approach, it is essential to consider the coupled design of the components and the leadframe layouts in order to take into account the wafer-level assembly. To simplify the leadframe layout, the Gate electrode of the NMOS devices is positioned at one side of the device as shown on Fig. 9(a).

The edge termination of the devices was adapted in order to allow the 3D stacking of the devices. In this case, 50 µm high peripheral deep trenches (Fig. 7) are realized by Deep Reactive Ion Etching (DRIE) process. This edge termination allows to island devices for arrays implementations while maximizing their voltage handling capability. In order to protect and passivate the 50 µm high peripheral trenches a double $Si_3N_4/SiO_2$ liner was deposited (Fig. 8).

For the die level 3D integration, we are using a non-patterned leadframe comprising only perforations. In this case we added an insulation layer on the backside of the devices to guarantee isolation between the leadframe and the Drain contact of the low side transistor. A 2 µm-thick $SiO_2$ layer was deposited in our case on all the concerned regions of the low side components as shown in Fig. 9(b).

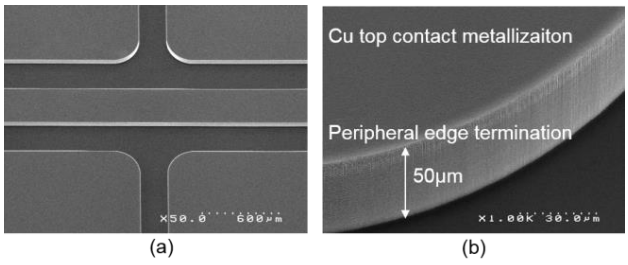



Figure 7. DRIE voltage termination of the devices (a) top view of the corner region of four devices and (b) peripheral view

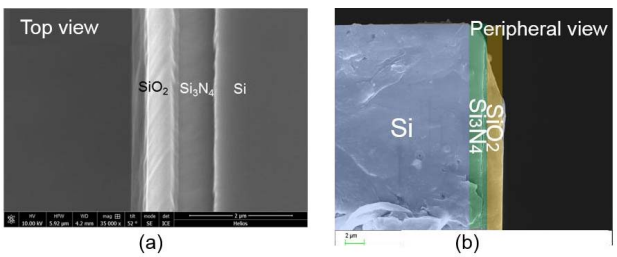



Figure 8. $Si_3N_4/SiO_2$ passivation layers of the peripheral trenches (a) top view and (b) peripheral view

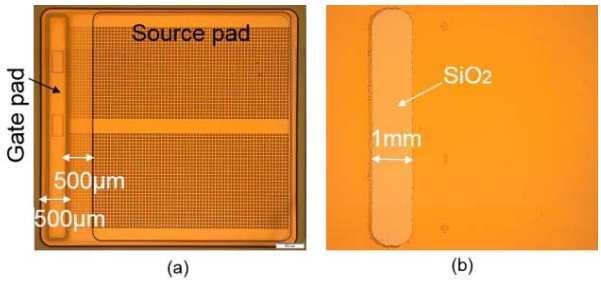



Figure 9. Detailed view of the Si NMOS device (a) top side view of the Gate and Source pads and (b) backside view of the device – Drain contact and 2µm thick $SiO_2$ insulation layer

## IV. RESULTS AND DISCUSSION

### A. *Wafer-level bonding*

Wafer-level assembly with the patterned and perforated Cu leadframe (Fig. 3 and 4) was tested both with Si wafers (Fig. 10) and with SiC wafers (Fig. 11). The Si wafers are unpatterned and covered with 50 nm-thick TiN layer as a diffusion barrier layer and 200 nm-thick PVD Cu layer as a bonding layer. The three wafers are simultaneously bonded using a thermocompression (TC) bonding [12]. When considering a direct metallic bonding step the surface roughness is a major parameter. To mitigate this constraint the process can be assisted by thermocompression. In this process, a combination of a thermal budget and uniaxial pressure are classically used in order to limit surface preparation. A [300-400] °C temperature and a pressure of a few MPa are applied on the assembly. This assures a bonding with relatively rough Cu surfaces. Indeed, if we do not polish the Cu surfaces, we measure a surface roughness of 7 nm RMS on the top of the Cu pillars. It is possible to polish both Cu surfaces before bonding using Chemical Mechanical Polishing (CMP) which reduces the roughness by a factor of 10. Fig 10 shows the Scanning Acoustic Microscopy (SAM) images of the Cu-Cu bonding interfaces (between the unpolished leadframe and the top Si wafer in Fig. 10(a) and with the bottom Si wafer in Fig 10(b)). The correctly bonded areas are the black areas and have been represented by a thick black line in the schematics of Fig 10. We observe that the Gate pad is not bonded using this integration scheme. This result indicates that only the areas that have a corresponding bonding surface at the top and the bottom interfaces can be efficiently bonded. This is confirmed by the SiC/Cu leadframe/SiC assembly shown in Fig. 11. In this experiment the top SiC wafer is patterned with JFET devices; the Cu leadframe is perforated and patterned only on the frontside. The backside is left without any patterns and only perforations which means that all topside bonding areas have a corresponding bottomside bonding areas. Fig. 11(a) shows the corresponding SAM images at the top interface. The bonding quality is not homogenous on the whole wafer (probably due to an important bow on the Cu leadframe), but on the periphery where the bonding quality is good it can be clearly seen that both the Gate and Source contacts are correctly bonded. Our

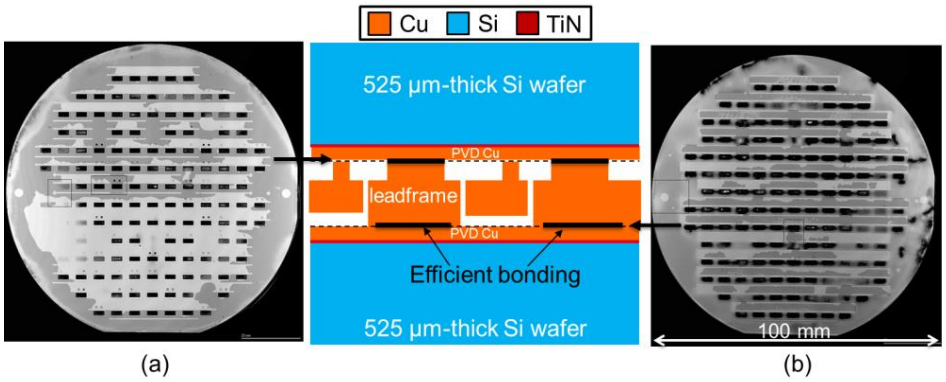



Figure 10. Schematics of the assembly with 2 Si wafers covered with Cu layer and the patterned and perforated Cu leadframe (described in Fig.3 and Fig.4). Scanning Acoustic Microscopy images of the Cu-Cu bonded interfaces (a) at the top interface and (b) at the bottom interface.

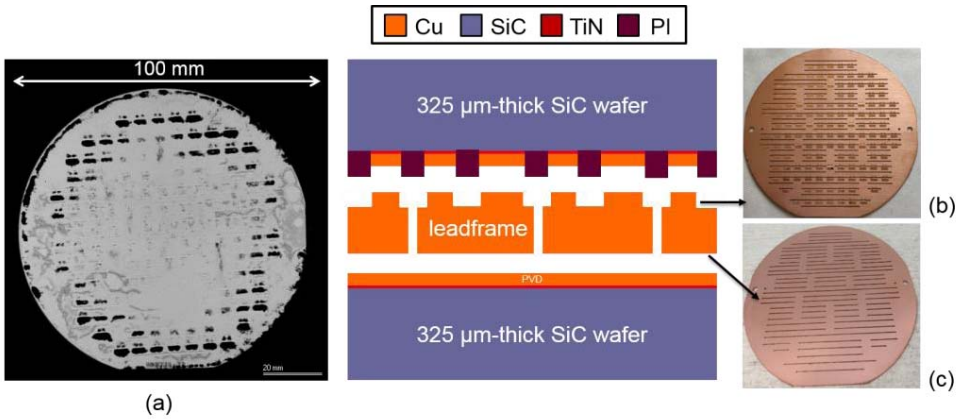



Figure 11. Schematics of the assembly with 2 SiC wafers and the Cu leadframe The top SiC wafer has devices (b). The Cu leadframe has Cu pillars on the top surface (c) and only perforations on the bottom surface. (a) Scanning Acoustic Microscopy image of the Cu-Cu bonded top interface

future work will consist on optimizing the process parameters for the manufacturing of the leadframe with the aim to reduce the bow of the metallic substrate. Reducing the Cu pillars surface roughness will also be the purpose of future investigations.

Fig. 12 shows a SEM cross section of the Cu-Cu bonding interface of another case of study with a polished leadframe and two Si wafers. The Cu leadframe was capped with 5 µm thick Cu layer deposited using electrochemical deposition (ECD) directly on the Cu bulk. On the Si wafers, a 20 nm thick TiN layer followed by a 200 nm thick PVD Cu layer are deposited before the 2 µm-thick ECD Cu layer. In this case the Cu surfaces are activated using CMP to decrease the surface roughness. A thermocompression direct bonding is performed with the three wafers simultaneously. The zoom in Fig. 12 shows small defects located on the bonding interface and at the TiN-Cu interfaces. This well-known voiding phenomena in copper bonded layers is a stress-driven vacancy diffusion mechanism [12]. The "zig-zag" interface (dashed line) means that the copper surfaces are completely sealed. This specific shape is due to the copper interdiffusion. In the case of non polished copper surface, the created voids are much larger but the bonding interface is also perfectly sealed as shown in [13].

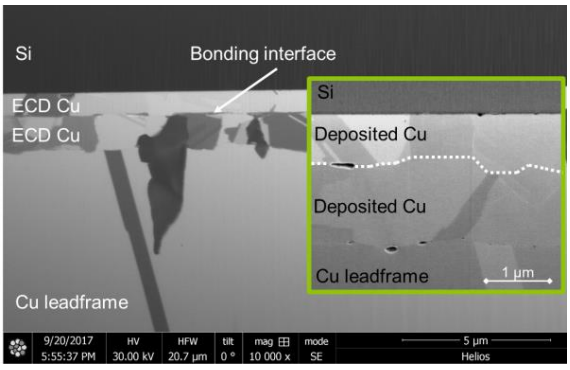



Figure 12. FIB SEM cross section of the Cu-Cu bonding interface. Insert with green lines: zoom on the Cu-Cu- bonding interface

### *B. 3D switching cell stacking*

3D switching cells at die-level were realized for the practical validation of the concept. Fig. 13 shows the

photographs of the 3D assembly of one and four switching cells. Si power devices were used for this implementation. The bonding step was performed with a thermocompression bonding equipment adapted for die level integration. As it is for the process parameters the same temperature as for the wafer level bonding was defined. The pressure force was adapted to fit the bonding surface in this case. A good bonding quality was observed as shown on Fig. 14.

After the bonding of the Si devices on both sides of the die level leadframe the electrodes contacts are accessible at the edges of the assembly. The frame edges are diced as shown with the dotted red line on Fig. 13(a). to separate the different electrodes. After this step the 3D power module is ready to be implemented in a PCB support. The leadframe comprises three interconnection electrodes for each switching cell. As shown on Fig. 13(b) $V_G$ is for the Gate interconnection, $V_{SW}$ is for the power signal and $V_S$ is the Kelvin connection of the Source pad in order to assure a better immunity for the driver.

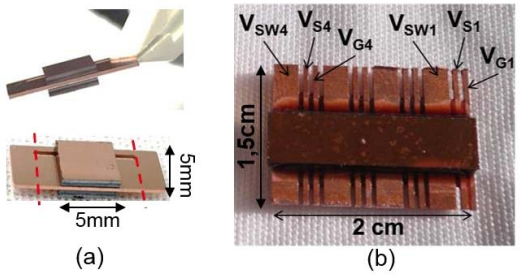



Figure 13. Photographs of the assembly of (a) one and (b) four switching cells realized at die level

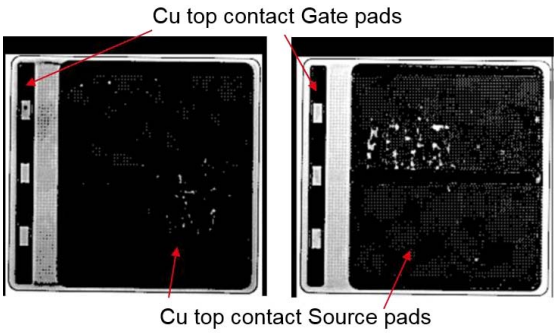



Figure 14. SAM view of the Cu-Cu bonded interfaces of two NMOS devices: good bonding quality in black, not good bonding quality in white

## C. *Electrical characterizations*

The vector of 3D stacked switching cells presented in the previous section has been implemented in order to validate its functionality. This prototype is based on the implementation of four switching cells with high side MOSFET transistors and low side freewheeling diodes. It is important to mention that, at this stage of our developments, we were not able to implement the components in real operating conditions, under high voltage and high current while driving the device for fast switching speeds. The main reasons for that is the prototypes yield that we are currently able to reach. Fig. 15(a) and (b) present the voltage and current waveforms obtained for one of the switching cell of the prototype. The tested conditions are $V_{BUS}$= 100 V, $I_{SW(DC)}$=$I_{LOAD}$=0,5 A average with a ripple current of about 1 A. Especially these testing conditions enable to operate the switching cell at first under reduced recovery current because the produced diodes are not ultra fast diodes and their turn off is not satisfactory for high switching speed operation. DC bus voltage is reduced to 100 V because after dicing and assembly the prototype presented a significant leakage current above 100 V. Switching frequency is reduced down to 3.75 kHz.

Fig. 15(b) presents a zoom on the power switch turn OFF. $V_{SW}$ represents the voltage at the switching cell middle point which corresponds to the voltage across the freewheeling diode. $V_T$ corresponds to the voltage across the high side power device while $I_{SW}$ is the load current. $V_{GS}$ is the voltage between Gate and Source of the power device. Please note that we were not able to insert a current probe within the switching cell. The waveforms are satisfactory although, the switching speed is relatively low. Indeed, the implementation of the prototyped 3D power module lacks from adapted DC bus decoupling capacitor. This is presented in Fig. 16(a) and (b) with a set of turn ON and turn OFF switching waveforms. In these time domain measurements,

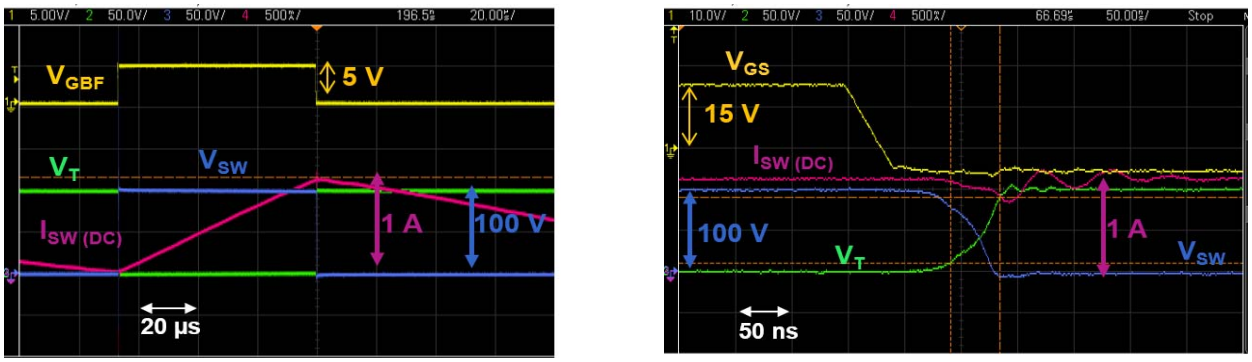
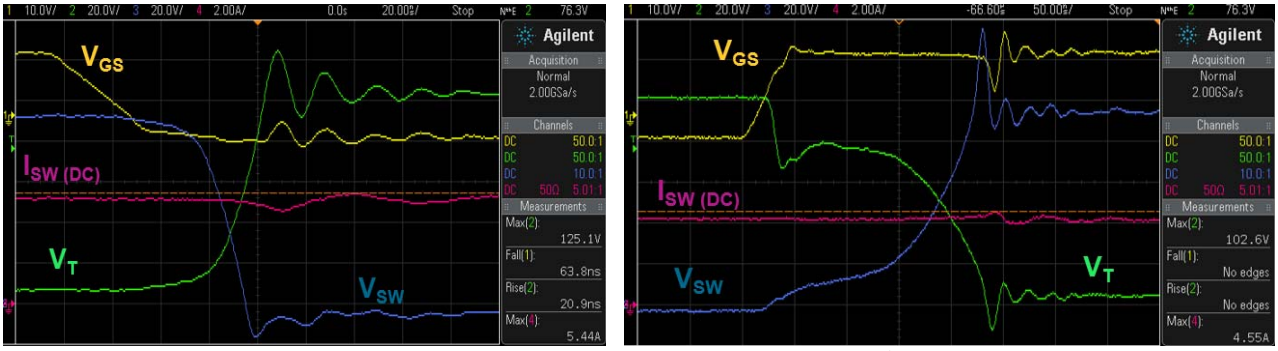



Figure 15. Dynamic characteristics of the realized 3D stack assembly at die level – $V_{BUS}$=100 V $I_{LOAD}$=0,5 A




(a) (b)

Figure 16. Dynamic characteristics of the realized 3D stack assembly at die level – $V_{BUS}$=100 V $I_{LOAD}$=5 A

obtained under 100 V DC Bus and 5 A average load current, the switching speed is increased to 10 V/ns and a 20 V significant overshoot is visible across the power transistor Drain to Source terminals under nominal current switching conditions. We think that this non optimized component implementation is responsible for the remaining voltage overshoot in the switching cell. The presence of this voltage overshoot is mainly due to the parasitic inductance introduced by the PCB traces to interconnect the switching cells' vector with the DC Bus decoupling capacitor. A 20 V overshoot under 100 V switched voltage seems significant but it would be reasonable if the power device was switching at 400 V under identical switching current conditions.

While these characterization waveforms are not fully demonstrative of advanced switching performances, they still demonstrate the feasibility and the interest of such an assembly. We are currently working on increasing the production yield of our prototypes and on improving the implementation conditions of the 3D assembly.

## V. CONCLUSION

This paper presented the direct copper bonding technology of a 3D patterned metallic leadframe between two semiconductor wafers as a possible technology to interconnect power devices without the addition of solder joints and allowing to replace the wire bondings by massive copper interconnections. The proposed concept enables the 3D stacking of power devices allowing the implementation of one or multiple switching cells pre-packaged at wafer level.

The presented results are partial and we are currently working on optimizing the process parameters for the wafer-level bonding and for the production yield of the power devices in order to fully demonstrate the benefits of the approach.

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