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Radio-Frequency Capacitive Gate-Based Sensing

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Developing fast, accurate, and scalable techniques for quantum-state readout is an active area in semiconductor-based quantum computing. Here, we present results on dispersive sensing of silicon corner state quantum dots coupled to lumped-element electrical resonators via the gate. The gate capacitance of the quantum device is placed in parallel with a superconducting spiral inductor resulting in resonators with loaded Q factors in the 400–800 range. We utilize resonators operating at 330 and 616 MHz, and achieve charge sensitivities of 7.7 and 1.3 $\mu e/\sqrt{\text{Hz}}$, respectively. We perform a parametric study of the resonator to reveal its optimal operation points and perform a circuit analysis to determine the best resonator design. The results place gate-based sensing on a par with the best reported radio-frequency single-electron transistor sensitivities while providing a fast and compact method for quantum-state readout.

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I. INTRODUCTION

The spins of isolated electrons in silicon are one of the most promising solid-state systems on which to implement quantum-information processing. With the recent demonstrations of long coherence times [1,2], high-fidelity spin readout [3], and one- and two-qubit gates [4–8], the basic requirements to build a quantum computer have been fulfilled [9]. Scaling the technology to a number of qubits sufficiently large to perform computationally relevant calculations is key for applications. Several proposals have been put forward for integrating a large number of qubits to build a full-fledged quantum computer [10–12]. In this respect, developing quantum-state readout techniques that are fast and accurate while also being compact has become an active area of research. Conventionally, readout in semiconductor gate-defined qubits is achieved using sensitive external electrometers. The most prominent example is the single-electron transistor (SET). Its radio-frequency version, the rf SET [13], sets the standard as the most sensitive electrometer with the best charge sensitivity reported

to date (0.9 $\mu e/\sqrt{\text{Hz}}$ [14]). The enhanced performance is based on reflectometry techniques that use lumped-element LC circuits to match the high resistance of the detector to the 50 Ω of the line [15]. However, mesoscopic electrometers, such as the rf SET, need to be placed in close proximity to the qubits adding complexity to the circuit architecture.

Circuit quantum electrodynamics (QED) offers an alternative method for the state readout of a quantum system. In this case, the qubit is embedded in a high- Q factor on-chip microwave resonator. This can be to the point of strong coupling, where the qubit and microwave photon dynamics become hybridized. In the dispersive limit, when the resonator and the quantum system are detuned, the state of the qubit can then be directly inferred from the oscillatory state of the resonator. This has been used to read superconducting [16] and more recently semiconductor qubits [17–19].

The same principle of dispersive readout has also been applied to rf reflectometry matching circuits [20–24]. This compact readout technique, namely, gate-based readout, uses existing gate electrodes coupled to off-chip lumped-element resonators for sensing [20,21]. This method alleviates the burden of external electrometers and reduces the

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complexity of the qubit architecture. Typically, gate-based sensing has been performed using low- Q factor resonators inspired by the matching networks developed for rf SETs [20–24] and has not been optimized for reactive changes in device characteristics, such as the quantum or tunneling capacitance [25–28].

Here, we bridge the gap between circuit QED-type measurements and lumped-element reflectometry techniques, by optimizing external matching circuits for capacitive changes. We show that significant improvements in sensitivity are possible by changing the circuit topology to enhance the Q factor of the resonator. While in one sense this brings rf reflectometry towards conventional circuit QED, the fact that we keep the microwave circuitry separate means that it can be fabricated separately from the nanodevice. This allows independent nanofabrication strategies for the resonator and the qubit. In particular, devices can be optimized to have a large gate coupling to the quantum system, which is an important ingredient for sensitive dispersive readout. This is where complementary metal-oxide-semiconductor (CMOS) technology, that for decades has been optimizing the gate coupling to the channel, can give an advantage over other qubit platforms. In this paper, we report gate-based dispersive readout of silicon-based CMOS few-electron quantum dots (QDs) [29,30] using lumped-element classical resonators with loaded quality factors, Q_L , in the 400–800 range. The enhancement in Q_L is achieved by configuring the device gate capacitance in parallel with a superconducting spiral inductor and coupling via a coupling capacitor to a printed-circuit-board (PCB) coplanar waveguide. We find charge sensitivities of 7.7 and 1.3 $\mu e/\sqrt{\text{Hz}}$ for resonators operating at 330 and 616 MHz, respectively. The latter represents an improvement of a factor of 30 over previous gate-based sensors [21] and sets gate-based reflectometry on a par with the best ever reported rf SETs. Finally, following a circuit analysis, we summarize the key requirements for sensitive capacitive gate-based readout: large Q_L resonators, well matched to the line, with low parasitic capacitance and large gate coupling to the quantum system. Our results pave the way for time-resolved dispersive readout of electron-spin dynamics.

II. DEVICE AND RESONATOR

The device investigated is a CMOS silicon nanowire field-effect transistor (NWFET) with channel length $l = 30$ nm, width $w = 60$ nm, and height $h = 11$ nm similar to the one shown in Fig. 1(a). The top-gate (TG) wraps around three faces of the n -type channel between the highly doped source (s) and drain (d); see Appendix A. At low temperatures, when the NWFET is biased below threshold ($V_{\text{TG}} \approx 0.5$ V), few-electron QDs form in the NW channel [29,31]. The transistor's multigate geometry, combined with a small equivalent gate oxide thickness

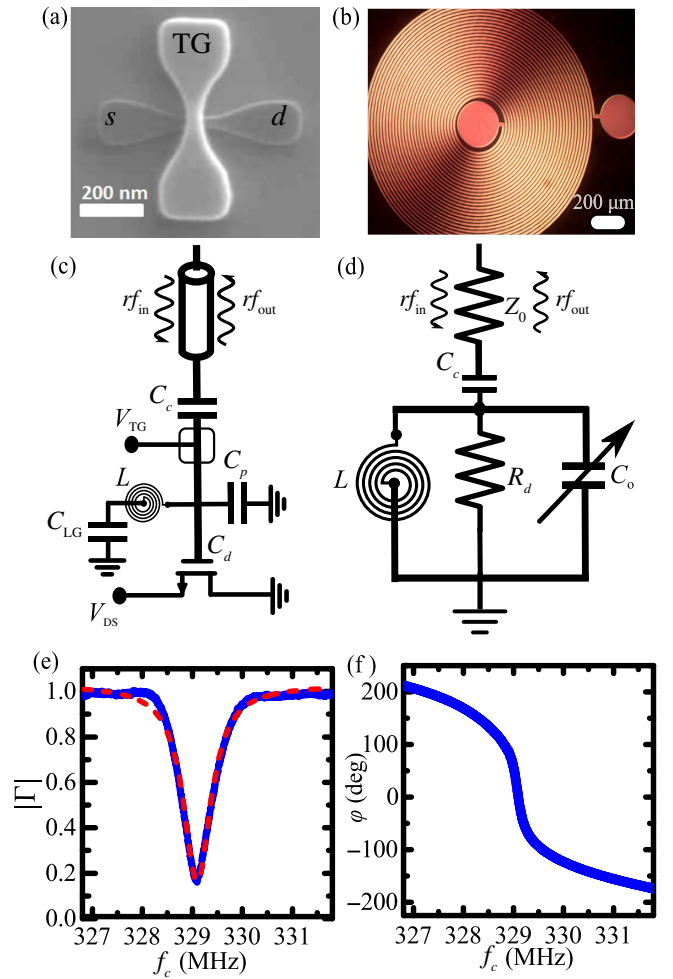


FIG. 1. Device and resonator. (a) A scanning electron micrograph of a NWFET showing source (s), drain (d), and top-gate (TG) terminals. (b) Optical image of a superconducting NbN spiral inductor. Spiral track width and track spacing are both 8 μm . (c) Circuit diagram for rf reflectometry. The NbN inductor L is connected in parallel with the top gate of the NWFET. The circuit has a parasitic capacitance of C_p to the ground. V_{DS} and V_{TG} are the bias voltages. $C_{\text{LG}} = 100$ pF. (d) Model for the parallel resonator coupled to external line impedance $Z_0 = 50 \Omega$ through C_c . The resistor R_d represents the losses in the resonator. (e) Magnitude $|\Gamma|$ and (f) phase $\varphi = \arg(\Gamma)$ as a function of the carrier frequency f_c . Data in blue and fit in dashed red.

of 1.3 nm, results in QDs with large gate couplings $\alpha = C_{\text{TG}}/C_{\Sigma} = 0.85\text{--}0.89$ since the total capacitance C_{Σ} is mostly given by its capacitance to the gate electrode C_{TG} .

The device is embedded in an electrical resonator containing a polycrystalline NbN superconducting planar spiral, which provides a low-loss and low-self-capacitance inductor L [20,32,33]. The 80-nm NbN films are grown in unheated c -plane 430- μm -thick sapphire substrates by dc magnetron sputtering. The deposition is performed in an Ar- N_2 atmosphere with 28% N_2 at 1.5 Pa. The spiral is defined using optical lithography and etching; see

Fig. 1(b). We wirebond the inductor in parallel with the device gate capacitance to the ground, C_d , and the circuit parasitic capacitance, C_p , and couple to the Z_0 line via a coupling capacitor C_c , as shown in Fig. 1(c). This differs from the series configuration explored in Refs. [20–24] and, as we shall see later, leads to enhanced sensitivity to capacitance changes. A simple equivalent model for the resonator, as in Fig. 1(d), consists of L , the circuit losses R_d and the variable capacitor $C_0 = C_p + C_d$ placed in parallel and coupled to the line by C_c . R_d represents dielectric losses in the device and the PCB and can contain dissipative terms arising from Sisyphus processes [21,26,27,34]. The parasitic capacitance, C_p , combines contributions from the device and the PCB.

In order to characterize the resonant frequency f_0 , bandwidth BW, and Q_L , we measure the complex reflection coefficient $\Gamma = |\Gamma|e^{i\varphi}$ as a function of the carrier frequency f_c . In Fig. 1(e), we show the magnitude $|\Gamma|$ (in blue) and a fit (in red). From this we estimate $L = 405$ nH, $C_c = 90$ fF, $C_p = 480$ fF, $R_d = 800$ k Ω . This gives us $f_0 = 1/[2\pi\sqrt{L(C_c + C_0)}] = 329.33$ MHz, $Q_L \approx 400$, and BW = 0.82 MHz. The large depth of the resonance $|\Gamma|_{\min} = 0.168$ indicates that the resonator is close to matching. The loaded Q contains contributions from the external Q factor, $Q_e = (C_c + C_0)/2\pi f_0 Z_0 C_c^2 = 680$, and the unloaded Q factor of the resonator, $Q_0 = 2\pi f_0 (C_c + C_0) R_d = 943$. In this particular design, external losses dominate Q_L but its value is increased by an order of magnitude when compared to series resonator gate-based approaches [20–24]. We operate in the overcoupled regime confirmed by the 180° phase shift, $\varphi = \arg(\Gamma)$, as a function of carrier frequency in Fig. 1(f).

III. DISPERSIVE REGIME

Gate-based sensing is a resonant technique that allows probing the complex admittance of a quantum device [20, 26,35,36]. Here, we couple a single QD in the NW channel to the resonator and probe its impedance using gate-based radio-frequency reflectometry at 40 mK [37,38]. We use this to probe susceptance changes when adiabatic single-electron tunneling occurs between the QD and the source or drain reservoirs. At resonance, variations in φ capture changes in the device capacitance ΔC that can be attributed to tunneling or quantum capacitance [28]. Since the resonator is overcoupled, $\Delta\varphi = -2Q_L\Delta C/(C_c + C_0)$.

In our system, the origin of ΔC can be explained by considering an uncoupled two-level system (TLS) described by a QD with zero (E_0) or one excess electron (E_1). Particles are exchanged with the source or drain reservoirs. If the TLS is driven by an external sinusoidal excitation at f_0 and the relaxation rate ν between levels is comparable, Sisyphus dissipation occurs [21,27]. However, if $\nu \gg f_0$, electrons tunnel adiabatically and out of phase with the drive. This results in a purely dispersive signal

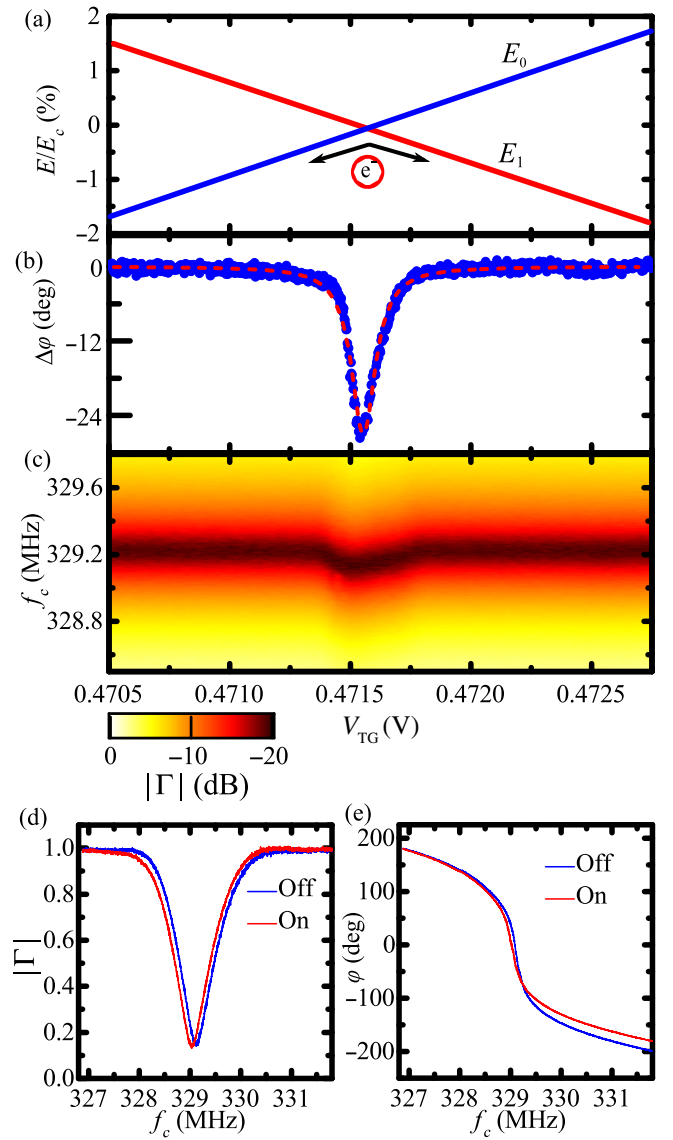


FIG. 2. Dispersive regime. (a) Energy diagram of a fast driven TLS, E_0 and E_1 , across a charge-degeneracy point. The energy is normalized to charging energy E_c of the QD. (b) Data (blue dots) and Lorentz fit (red dashed curve) for the phase change $\Delta\varphi$ of the resonator as a function of V_{TG} . (c) $|\Gamma|$ as a function of carrier frequency f_c and V_{TG} . Experimental data for (d) $|\Gamma|$ and (e) φ at two different V_{TG} voltages—away from and at the charge degeneracy, blue and red traces, respectively.

manifesting as a tunneling capacitance contribution C_t [22]. In Fig. 2(a), we show schematically a TLS driven across a charge degeneracy point where E_0 and E_1 cross each other at a fixed top-gate voltage point V_{TG}^0 . In the regime $\nu \gg f_0$, the electron always stays in the ground state and the tunneling capacitance is given by

$$C_t = \frac{(\alpha e)^2}{\pi} \frac{h\nu}{(h\nu)^2 + (\alpha e \Delta V_{TG})^2}, \quad (1)$$

where h is Planck's constant, e is the electron charge, and $\Delta V_{TG} = V_{TG} - V_{TG}^0$ [22,39]. This voltage-dependent

C_t produces a phase shift in the resonator, as can be seen in Fig. 2(b), where $\Delta\varphi$ is plotted as the V_{TG} is swept across the charge-degeneracy point. We measure a maximum phase shift $\Delta\varphi = 28^\circ$ at the degeneracy point. Using Eq. (1), we fit $\Delta\varphi$ (red curve) and extract $\nu = 26$ GHz ($\gg f_0$) from the full width at half maximum (FWHM). C_t loads the resonator pulling down its resonant frequency as shown in Fig. 2(c). Finally, in Figs. 2(d) and 2(e), we compare $|\Gamma|$ and φ on and off the degeneracy point. From these measurements, we extract a dispersive shift $\Delta f = 88$ kHz, which corresponds to an effective change in capacitance given by $\Delta C = 2(C_c + C_0)\Delta f/f_0 = 0.3$ fF. This agrees well with the expected maximum tunneling capacitance 0.37 fF, calculated from Eq. (1).

IV. CHARGE SENSITIVITY

We use the technique in Ref. [13] to measure the charge sensitivity of the capacitive gate-based sensor: A small sinusoidal voltage is applied to the top gate of the device with a root-mean-square charge equivalent amplitude Δq and frequency f_m . This produces an amplitude modulation of the carrier that results in sidebands appearing in the power spectrum of the reflected signal at $f_c \pm f_m$, as can be seen in Fig. 3(a) along with the rf carrier. The height of the sideband measured from the noise floor defines the power signal-to-noise ratio (SNR). The charge sensitivity is then calculated from the definition, $\delta q = \Delta q / (\sqrt{2\text{RBW}} \times 10^{\text{SNR}/20})$, where RBW is the resolution bandwidth of the spectrum analyzer [14]. A separate figure of merit is the modulation depth dBc, given by the sideband height relative to the carrier in dB. This figure indicates how much of the input signal is modulated by the device. Figure 3(a) shows the power spectrum at the optimal working point of the resonator (identified by measurements described below). The spectrum is obtained using a modulation signal with $f_m = 511$ Hz and $\Delta q = 6.98 \times 10^{-4}e$ and a RBW = 10 Hz. We measure a SNR = 26.1 dB, resulting in $\delta q = 7.7 \mu e/\sqrt{\text{Hz}}$. This result represents a charge sensitivity improvement of a factor of ~ 5 with respect to previous reports [21] and demonstrates the advantage of adopting the parallel circuit configuration of the capacitive gate sensor. Given the charging energy of the QD in this device, $E_c = 31$ meV, the gate sensor has an energy sensitivity $\delta\epsilon$ of $1395\hbar$ [40].

We now discuss the parametric study of the gate-based sensor's sensitivity in terms of V_{TG} , f_c , and carrier power P_c to find the optimal working point. In Fig. 3(b), we show the lower sideband SNR as a function of V_{TG} and P_c . For a fixed P_c , the SNR shows two maxima whose separation in V_{TG} increases as P_c is increased. The position of the maxima corresponds to the V_{TG} points of maximum slope at either side of the charge transition in Fig. 2(b). The dependence of the separation with increasing P_c indicates that the transition is being broadened by the rf voltage

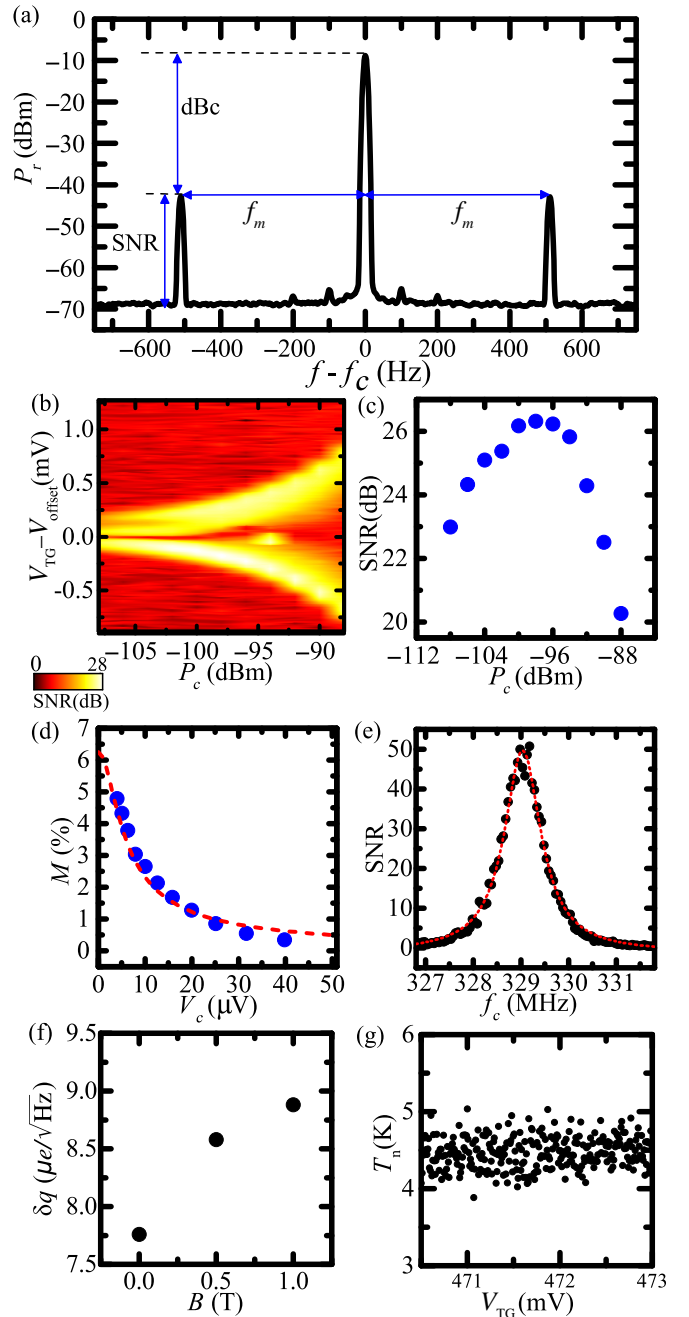


FIG. 3. Measuring and optimizing charge sensitivity. (a) Reflected power P_r spectrum showing the sidebands at $f_c \pm f_m$ due to gate-voltage modulation. (b) SNR in dB as a function of V_{TG} and P_c ($V_{offset} = 472.23$ mV). (c) Sideband SNR as a function of P_c . (d) Modulation index M (blue dots) and fit (red dashed curve) as a function of input rf carrier voltage V_c . (e) Sideband power SNR in linear scale vs rf carrier frequency f_c measured at $P_c = -115$ dBm. (f) Measured charge sensitivity as a function of the magnetic field B . (g) Noise temperature T_n as a function of V_{TG} measured at f_0 with RBW = 300 kHz.

V_c . Only at the lowest values of P_c , where the separation between peaks remains constant, is the transition lifetime limited.

To find the optimal carrier power for sensing, we extract the maximum SNR at each P_c (blue dots) as shown in Fig. 3(c). The SNR peaks at $P_c = -98$ dBm when the transition is still power broadened, as opposed to the expectation that the maximum SNR would be achieved when the transition is lifetime broadened. To understand why, we define the modulation index $M = 10^{\text{dBc}/20}$ and note that the sideband SNR can be expressed as $\text{SNR} = MP_c$. M decreases as the rf carrier voltage V_c increases [blue dots in Fig. 3(d)]. This dependence can be modeled as a convolution of two competing processes: lifetime broadening and power broadening. The transition is lifetime broadened by ν to produce a linewidth V_ν ($h\nu = e\alpha V_\nu$) and power broadened by applied rf carrier power with a linewidth proportional to V_c . The dependence of M on V_c can be approximated by $1/\sqrt{V_\nu^2 + V_c^2}$, which decreases with increasing V_c , as shown in Fig. 3(d) (red dashed curve). The maximum SNR occurs when the increase in input power is compensated by the decrease in M .

Next, we find the optimal carrier frequency. We plot the sideband power SNR (in linear scale) at $f_c - f_m$ as a function of rf carrier frequency f_c when swept across a frequency range containing f_0 [see Fig. 3(e)]. The SNR shows a Lorentzian profile with center frequency f_0 , and BW and Q_L matching the values obtained from Fig. 1(e). To avoid power broadening, the input rf power is kept at -115 dBm during this measurement.

Additionally, we study the dependence of the sensor's charge sensitivity on in-plane magnetic field, given our use of a superconducting material (NbN) for the lumped-element inductor, and the fact that for typical spin-qubit systems, an external magnetic field is used to Zeeman-split the spin-degenerate energy levels [3,4,41]. We measured $\text{SNR} = 24.9$ dB at 1 T, which gives a charge sensitivity $\delta q = 8.8 \mu e/\sqrt{\text{Hz}}$, as shown in Fig. 3(f). This result demonstrates that our gate-sensor sensitivity only deteriorates by 15% at 1 T and hence is robust against moderate magnetic fields used to operate Si spin qubits.

Finally, in Fig. 3(g), we measure the noise temperature T_n of the system at the resonance frequency as a function of V_{TG} . As we sweep V_{TG} across the charge-degeneracy point, T_n stays constant 4.5 ± 0.4 K, which matches with the noise temperature of our cryogenic amplifier (Quinstar QCA-U350-30H). Hence we conclude that charge sensitivity is limited by the thermal noise of the cryoamplifier and not by Sisyphus noise, which can be orders of magnitude smaller [21]. In this study, we emphasize the importance of improving the resonator design to increase the signal of gate-based approaches. Improving the noise floor by using, for example, a Josephson parameter amplifier (JPA) will lead to additional enhancements on the experimental sensitivity of the capacitive gate-based sensor.

V. RESONATOR OPTIMIZATION

In this section, we explore the resonator design analytically to highlight ways to optimize the circuit and understand the ultimate performance of capacitive gate-based charge sensing. We consider the circuit in Fig. 1(d) and its reflection coefficient:

$$\Gamma = \frac{Z - Z_0}{Z + Z_0}, \quad (2)$$

where Z is the complex impedance of the coupling capacitor C_c in series with the parallel combination of the inductor L , the circuit resistance R_d , and circuit variable capacitance C_0 . Gate-based reflectometry is sensitive to changes in the reflection coefficient. In this work, we are concerned with capacitance changes in the circuit due to single-electron tunneling that can manifest in the form of quantum or tunneling capacitance [28]. Therefore, we calculate the absolute value of the differential change in the reflection coefficient with C_0 ,

$$|\Delta\Gamma| = \left| \frac{\partial\Gamma}{\partial C_0} \Delta C \right| = \frac{2R_{\text{eq}}Z_0}{(R_{\text{eq}} + Z_0)^2} Q_0 \frac{\Delta C}{C_c + C_0}. \quad (3)$$

Here, $R_{\text{eq}} = L(C_c + C_0)/R_d C_c^2$, is the equivalent resistance of the circuit at $f = f_0$, as depicted in Fig. 4(a). The charge sensitivity is inversely proportional to $|\Delta\Gamma|$ and hence a study of this magnitude yields an estimate of the relative sensitivity level [42,43].

Equation (3) provides the guidelines to optimize the sensitivity of gate-based sensing approaches. First, exemplified in Fig. 4(b), where we plot both $|\Delta\Gamma|$ and $|\Gamma|$ as a function of C_c , we observe that $|\Delta\Gamma|$ is maximum when the coupling capacitor is chosen to give perfect matching ($|\Gamma| = 0$), i.e., $R_{\text{eq}} = Z_0$. Second, increasing R_d , and in turn the unloaded Q factor, leads to an increase in sensitivity. The effect on $|\Delta\Gamma|$ of increasing R_d can be seen in Fig. 4(c) where the maximum $|\Delta\Gamma|$ increases as R_d is increased from 200 k Ω (blue) to 2 M Ω (black). Note the change in optimal C_c as R_d is varied. $|\Delta\Gamma|_{\text{max}}$ increases linearly with R_d as can be seen in the inset. Third, a reduction of the circuit capacitance, by reducing C_p , leads to an enhanced sensitivity. This can be observed in Fig. 4(d) where we plot $|\Delta\Gamma|$ as a function of C_c and fixed L and R_d for three different values of C_p , 0.2 pF (black), 0.48 pF (red), and 0.8 pF (blue). $|\Delta\Gamma|_{\text{max}}$ decreases as $C_p^{-1/2}$, as can be seen in the inset. Finally, the change in device capacitance, ΔC , needs to be maximized. This can be achieved by maximizing the gate-coupling factor α , which has a quadratic effect on $|\Delta\Gamma|$, as can be seen in Eq. (1).

Ultimately, Eq. (3) can be expressed in much simpler terms when the resonator is matched to the line, $|\Delta\Gamma| = \pi R_d f_0 \Delta C$. In this case, we see that the optimal device should have as low dissipation as possible (large R_d).

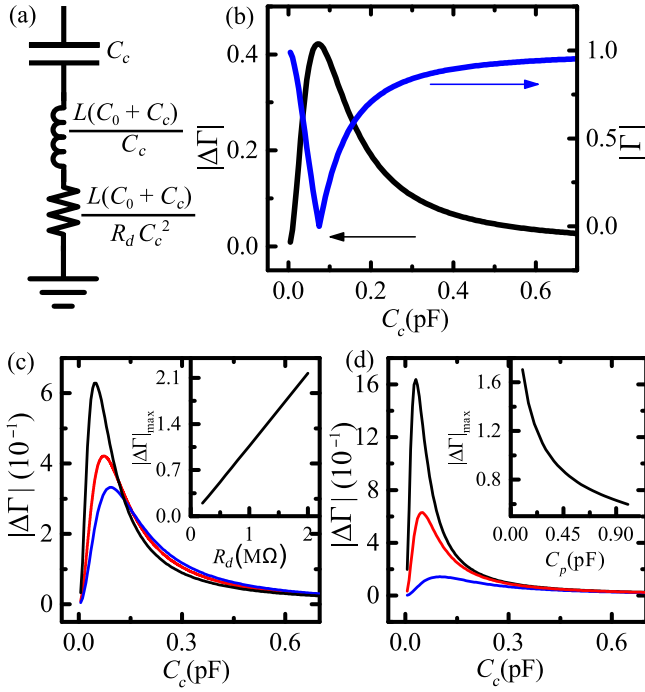


FIG. 4. Resonator optimization. (a) Equivalent circuit at resonance. (b) $|\Delta\Gamma|$ (black) and $|\Gamma|$ (blue) as a function of C_c for the experimental values $R_d = 800$ k Ω , $C_p = 0.48$ pF, $L = 405$ nH, and $Z_0 = 50$ Ω . We consider $\Delta C = 1$ fF. (c) Dependence on R_d . $|\Delta\Gamma|$ as a function of C_c for $R_d = 200$ k Ω (blue), 800 k Ω (red), and 2 M Ω (black). Inset: Maximum $|\Delta\Gamma|$ as a function of R_d . (d) Dependence on C_p . $|\Delta\Gamma|$ as a function of C_c for $C_p = 0.8$ pF (blue), 0.48 pF (red), and 0.2 pF (black). Inset: Maximum $|\Delta\Gamma|$ as a function of C_p .

Moreover, gate-based sensing benefits from operating at high frequency as we demonstrate in the next section.

VI. HIGHER-FREQUENCY OPERATION

To assess the advantage of operating the capacitive gate-based sensor at higher frequencies, we perform a second set of experiments on a nominally identical device but narrower channel, $w = 30$ nm, and a resonator with resonant frequency $f_0 = 616.18$ MHz. We use a NbN inductor, $L = 134$ nH. In Figs. 5(a) and 5(b), we see the magnitude $|\Gamma|$ and phase φ of the reflection coefficient. The resonator has a BW = 0.78 MHz and hence a loaded Q factor $Q_L = 790$, is close to matching $|\Gamma|_{\min} = 0.1$ and overcoupled $Q_e < Q_0$.

We characterize the gate-based sensor in terms of charge sensitivity following the procedure explained in Sec. IV and obtain an optimized charge sensitivity of $1.3 \mu e/\sqrt{\text{Hz}}$ at $P_c = -120$ dBm. For this measurement, we use $\Delta q = 1.48 \times 10^{-4} e$ and RBW = 20 Hz. The sensitivity improvement is 30 times when compared to previous reports [21] and places the charge sensitivity of the capacitive gate-based sensors on a par with the best reported rf SET

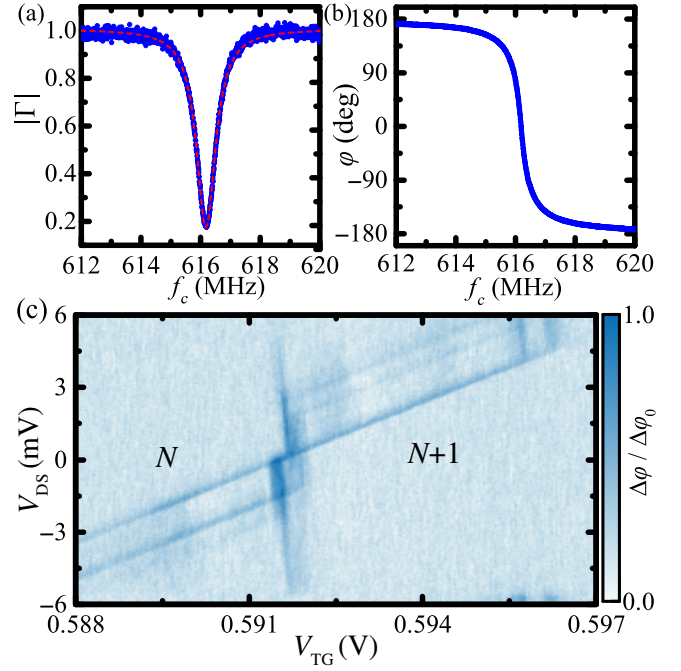


FIG. 5. High-frequency resonator. Magnitude (blue dots) and a Lorentz fit (red dashed curve) (a) and phase (b) of the reflection coefficient Γ as a function of carrier frequency f_c . (c) Fast data acquisition of a dot to reservoir transition. V_{DS} is ramped at 4 kHz while V_{TG} at 7 Hz. Each trace is averaged five times. The total measurement time is 700 ms.

sensitivities [14,40]. In this case, the energy sensitivity $\delta\epsilon$ is $36\hbar$ since the charging energy $E_c = 28$ meV [40].

We demonstrate the advantage of the improved sensitivity by acquiring a charge-stability map of the device containing 512×256 data points in just 700 ms, see Fig. 5(c). Here, we use a double ramp scheme [44] where we ramp the drain voltage, V_{DS} at 4 kHz (sawtooth) while slowly ramping V_{TG} at 7 Hz (triangular). The frequency of the ramp is limited in this measurement by the low-pass filtering in our lines (cutoff frequency 5 kHz). The 2D map is composed of traces of the demodulated phase response. In Fig. 5(c), we see the characteristic signature of Coulomb blockade measured dispersively with the gate-based sensor. The combination of the data quality and short acquisition time demonstrates the potential of this new gate-based sensor design for fast readout of semiconductor nanostructures. Given the integration time of $5 \mu\text{s}$ per point, capacitive gate-based sensing may enable performing single-shot readout of electron-spin dynamics in silicon.

VII. CONCLUSION

We demonstrate an optimized design for gate-based sensing for which the charge sensitivity is a factor of 28 better than the best reported gate sensor [21] and it is comparable to the best sensitivities ever demonstrated for

the rf SET [14]. In the case of the rf SET, the experimental sensitivity is limited by shot noise whereas in the case of our gate sensor it is limited by the noise of the cryogenic amplifier. If a JPA, located at the mixing chamber of a dilution refrigerator (~ 10 mK), were to be used instead of a more standard cryogenic amplifier ($T_n \sim 4$ K), one should expect a reduction of the charge sensitivity by a factor of 20. For the resonator in Sec. VI., it would imply a charge sensitivity of $\delta q = 65 ne/\sqrt{\text{Hz}}$, making the gate sensor the most sensitivity electrometer. However, the ultimate sensitivity of this dispersive sensor remains to be explored and a study should consider additional sources of noise such as the Sisyphus noise [21] and the Johnson-Nyquist noise of the resonator, which can be orders of magnitude lower than shot noise at millikelvin temperatures and radio frequencies. Additionally, the charge sensitivity demonstrated combined with the bandwidth of the resonators results in a few microsecond detection with a rms charge noise ($\Delta Q = \delta q \times \sqrt{BW}$) well below $1e$. Therefore, capacitive gate-based sensing could allow single-shot readout of electron spins in silicon double QDs where the relaxation and coherence times are typically larger than a microsecond [1,2]. In the future, devices with additional gates such as CMOS transistors in series [45] or split-gate CMOS transistors [46,47] should provide access to experiments in which the resonator couples to interdot charge transitions, and Pauli spin blockade is used for electron-spin readout.

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APPENDIX A: DEVICE DESCRIPTION

The device used in this paper is a silicon nanowire field-effect transistor (NWFET) fabricated in fully depleted

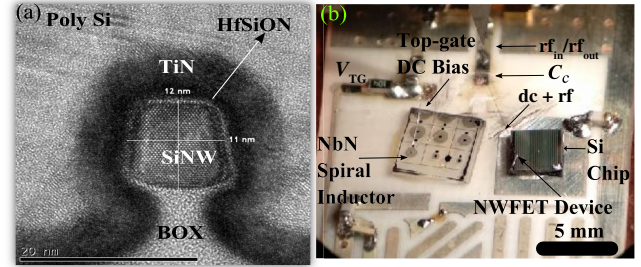


FIG. 6. (a) Transmission electron micrograph (TEM) of silicon NWFET cross section perpendicular to the direction of transport of a narrower device similar to the ones measured in this paper. (b) Measurement PCB showing the NbN spiral inductor on sapphire and the NWFET chips.

silicon-on-insulator (SOI) following CMOS rules [29]. In Fig. 6(a), we present a transmission electron micrograph (TEM) of a similar device to the ones measured in this paper showing a cross section of the nanowire perpendicular to the direction of current transport. The 11-nm-thick NW channel is patterned on SOI above the 145-nm buried oxide (BOX). The gate oxide consists of 0.8 nm SiO_2 and 1.9 nm HfSiON resulting in an equivalent gate oxide thickness of 1.3 nm. The top gate (TG) is formed using 5-nm TiN and 50-nm polycrystalline silicon. In square-cross-section silicon NWs, QDs form at the topmost corners of the device [21,29–31].

APPENDIX B: MEASUREMENT PCB

We explain the circuit used for measurements presented in this manuscript. A 5×5 mm² sapphire chip contains spiral NbN inductors of different turn numbers as shown on the left in Fig. 6(b). The 3×3 mm² Si chip on the right contains many similar NWFET devices with different channel length l and width w . We wire bond the NbN inductor and the top gate of the NWFET to a PCB pad capacitively coupled to the rf line via C_c (bond pad size 70×70 μm^2 ; device dimensions, $h = 11$ nm and $l = 30$ nm, $w = 30$ nm) as can be seen in Fig. 6(b) using an ultrasonic wire bonder (wedge dimension 17 μm). The top gate of the NWFET is biased from the DC bias line through the NbN inductor.

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