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Bruna Cardoso Paz, Mikaël Cassé, Sylvain Barraud, Gilles Reimbold, Maud Vinet, et al.. New method for individual electrical characterization of stacked SOI nanowire MOSFETs. 2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Oct 2017, Burlingame, United States. 10.1109/S3S.2017.8309237 . cea-01974212

**HAL Id: cea-01974212**

**<https://cea.hal.science/cea-01974212>**

Submitted on 8 Jan 2019

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# New method for individual electrical characterization of stacked SOI nanowire MOSFETs

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**Abstract**—A new systematic procedure to separate the electrical characteristics of advanced stacked nanowires (NWs) with emphasis on mobility extraction is presented. The proposed method is based on I-V measurements varying the back gate bias ( $V_B$ ) and consists of three basic main steps, accounting for  $V_B$  influence on transport parameters. Lower mobility was obtained for the top GAA NW in comparison to bottom  $\Omega$ -NW. Temperature dependence of carrier mobility is also studied through the proposed method up to 150°C.

**Keywords**—stacked nanowires; mobility; back gate bias; SOI

## I. INTRODUCTION

Aggressively scaled multiple-gate transistors, such as nanowire MOSFETs, have demonstrated excellent performance and strong immunity against short channel effects, due to improved electrostatics [1]. Thanks to advances in fabrication process steps, such structures can be vertically stacked in order to fulfill higher drive current requests [2]–[4]. Reducing the intrinsic parasitic capacitances and boosting carriers' mobility are considered two of the main challenges to implement stacked NWs for future technological nodes. Aiming to step up into the solution of these problems, vertically stacked p-NWs combining both inner spacers and SiGe S/D have been recently fabricated [3]. Overall performance and transport of these stacked NWs have been investigated in [5], but still no individual electrical characterization of each NW level is available, which could be valuable for technology optimization. A methodology to separate the channels conduction was firstly proposed and applied to Multi-Gate devices using the effect of the applied back bias  $V_B$  [6]. However this method does not take into account the low field effect mobility ( $\mu_0$ ) dependence on  $V_B$  [7]. In this work, we improved the methodology in [6] by including explicit expressions for  $\mu_0$  and mobility degradation coefficients ( $\theta_1$  and  $\theta_2$ ) dependence on  $V_B$ , based on measurements and modelling. The proposed method is applied to advanced narrow stacked NWs from room to high temperature for a better understanding of their electrical characteristics.

## II. DEVICES AND MEASUREMENTS

Two levels vertically stacked SOI NWs MOSFETs have been fabricated at CEA-LETI with a replacement metal gate

process, integrating inner spacers and  $\text{Si}_{0.7}\text{Ge}_{0.3}\text{:B}$  raised S/D (Fig.1). Further fabrication details can be found in [3]. The bottom NW presents  $\Omega$ -shaped gate and depends electrostatically on  $V_B$ , while the top wire is GAA (Gate-All-Around) and independent of  $V_B$ . The proposed methodology uses this  $V_B$  dependence to dissociate  $\Omega$ - and GAA-NWs electrical properties.

Fig. 2 presents the drain current ( $I_{DS}$ ) and its second derivative ( $\delta g_m / \delta V_{GS}$ ) as a function of the front gate voltage ( $V_{GS}$ ) for narrow NW varying  $V_B$ . From the logarithmic I-V

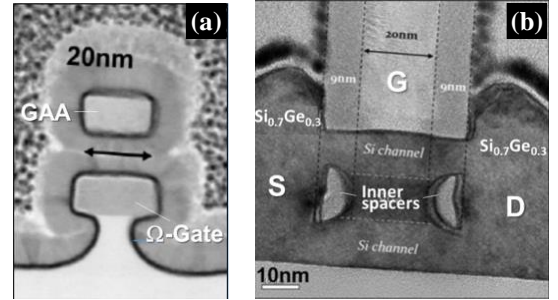


Fig. 1. TEM images of vertically stacked SOI NW cross section (a) and longitudinal section (b). Both top and bottom Si channels are 10nm thick. BOX thickness is 145nm. Gate stack is composed by  $\text{HfO}_2/\text{TiN}/\text{W}$  (EOT  $\sim 1.2\text{nm}$ ).  $W_{\text{FIN}}$  indicates the top width of the NWs.

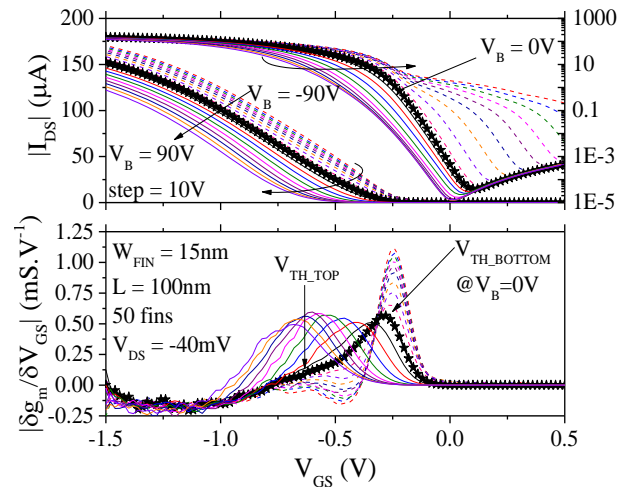


Fig. 2.  $|I_{DS}|$  and  $|\delta g_m / \delta V_{GS}|$  vs.  $V_{GS}$  for stacked NW,  $W_{\text{FIN}} = 15\text{nm}$ ,  $L = 100\text{nm}$ ,  $V_{DS} = -40\text{mV}$  and  $V_B$  from -90 to 90V.

curves, it is observed that back conduction (BC) appears for negative  $V_B$ . The derivative of the transconductance ( $g_m$ ) shows two distinguished peaks: one constant and insensitive to  $V_B$ , related to the threshold voltage ( $V_{TH}$ ) of the top NW ( $V_{TH\_TOP}$ ), and another one sensitive to  $V_B$ , corresponding to bottom  $\Omega$ -NW threshold voltage ( $V_{TH\_BOTTOM}$ ). No peak is observed due to BC because its contribution is almost negligible, as expected in narrow  $\Omega$ -NWs. Fig. 3 shows both  $V_{TH}$  extracted from  $\delta g_m / \delta V_{GS}$  peaks and the subthreshold slope (S). For  $V_B < -10V$  there is BC, so  $V_{TH\_BOTTOM}$  is constant and S degrades with  $V_B$  reduction. For  $V_B > -10V$   $V_{TH\_BOTTOM}$  decreases with  $V_B$  increase. Due to thin silicon layer, the bottom NW never reaches accumulation [8]. Applying high positive  $V_B$  ( $>50V$ ),  $V_{TH\_BOTTOM} < V_{TH\_TOP}$  and  $V_{TH}$  and S are determined by the GAA-NW.

### III. ANALYSIS AND DISCUSSION

By applying the Y-function method [9] to the measured  $I_{DS}$ , it is possible to extract the overall parameters related to the sum of  $\Omega$ - and GAA-NW contributions. The proposed method uses 3 steps.

Step 1.– As the GAA-NW is  $V_B$  independent, if the region of main interest where the Y-function is applied is carefully chosen (Fig.4-a), the extracted  $\theta_1(V_B)$ ,  $\theta_2(V_B)$  and  $\mu_0(V_B)$  can be exclusively attributed to the bottom  $\Omega$ -NW. A linear behavior is verified between the transport parameters and  $V_B$ . The same linear behavior has been observed for reference wafers with non-stacked TriGate (TG) NWs with similar dimensions, as indicated in Fig.6. Linear fittings of  $\theta_1(V_B)$ ,  $\theta_2(V_B)$  and  $\mu_0(V_B)$  lead to the extraction of corresponding slope and intercept, i.e.  $\theta_{1,\Omega G} = A\theta_1 + a\theta_1 \times V_B$ ,  $\theta_{2,\Omega G} = B\theta_2 + b\theta_2 \times V_B$  and  $\mu_{0,\Omega G} = C\mu_0 + c\mu_0 \times V_B$ . Fig. 4-a shows measurements and fitted lines of  $g_m$  as a function of  $V_{GS}$ . The peak variation with  $V_B$  clearly indicates its influence on the mobility parameters of the  $\Omega$ -NW, which is the reason why this region was selected for applying the Y-function in this step. Negative  $V_B$  values are chosen because  $V_{TH\_BOTTOM}$  is constant and  $\Omega$ -NW current shift does not affect the extraction.

Step 2.– For  $V_B \geq 0$ , there is no BC and  $I_{DS}(V_B \geq 0) = I_{DS,\Omega G}(V_B) + I_{DS,GAA}$  (1), where  $\Omega$ - and GAA-NWs drain

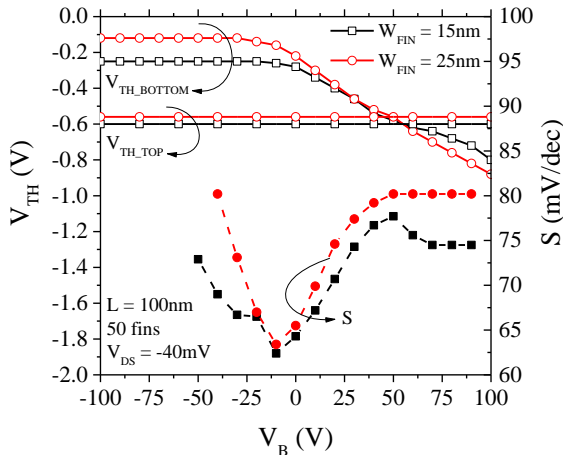


Fig. 3.  $V_{TH}$  and S vs.  $V_B$  for NWs with  $W_{FIN} = 15$  and  $25nm$ ,  $L = 100nm$  and  $V_{DS} = -40mV$ .

currents (at low  $V_{DS}$ ) are given by:

$$I_{DS,\Omega G}(V_B) =$$

$$\frac{W_{eff,\Omega G} \times C_{OX}}{L} \frac{\mu_{0,\Omega G}(V_B) \times V_{GT,\Omega G}(V_B) \times V_{DS}}{1 + \theta_{1,\Omega G}(V_B) \times V_{GT,\Omega G}(V_B) + \theta_{2,\Omega G}(V_B) \times V_{GT,\Omega G}^2(V_B)} \quad (2)$$

$$I_{DS,GAA} = \frac{W_{eff,GAA} \times C_{OX}}{L} \frac{\mu_{0,GAA} \times V_{GT,GAA} \times V_{DS}}{1 + \theta_{1,GAA} \times V_{GT,GAA} + \theta_{2,GAA} \times V_{GT,GAA}^2} \quad (3)$$

$V_{GT}$  is the gate voltage overdrive ( $V_{GT} = V_{GS} - V_{TH}$ ). Considering that mismatches of  $W_{FIN}$  and  $t_{Si}$  between  $\Omega$ - and GAA-NWs are negligible, as suggested in Fig.1, the effective channel widths are  $W_{eff,\Omega G} = (2t_{Si} + W_{FIN})$  and  $W_{eff,GAA} = (2t_{Si} + 2W_{FIN})$ . The linear behavior with  $V_B$  is attributed to mobility parameters of the  $\Omega$ -NW. The subtraction of total drain currents at different  $V_B \geq 0$  leads to an expression that only depends on  $I_{DS,\Omega G}$ :

$$\Delta I_{DS}(V_B) = I_{DS}(V_{B1} \geq 0) - I_{DS}(V_{B2} > V_{B1}) =$$

$$I_{DS,\Omega G}(V_{B1}) - I_{DS,\Omega G}(V_{B2}) \quad (4)$$

As indicated in Fig.4-b, the fitting procedures of (4) allow to determine  $A\theta_1$ ,  $B\theta_2$  and  $C\mu_0$ .

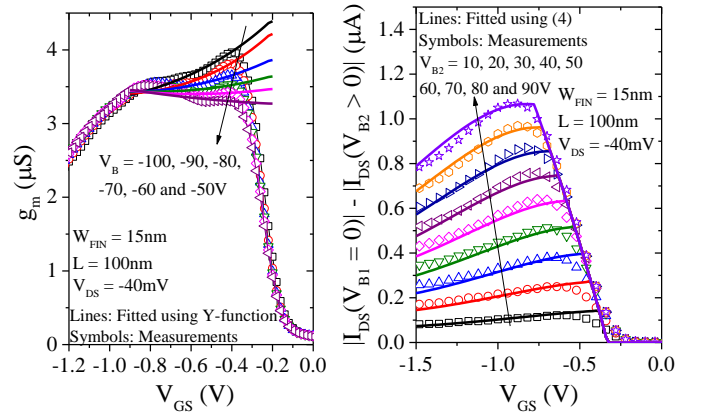


Fig. 4. (a) Step 1. Measurements and model results of  $g_m$  vs.  $V_{GS}$  for NW with  $W_{FIN} = 15nm$ ,  $L = 100nm$  and  $V_{DS} = -40mV$ . (b) Step 2. Measurements and model results of  $\Delta I_{DS}$  vs.  $V_{GS}$  for NW with  $W_{FIN} = 15nm$ ,  $L = 100nm$  and  $V_{DS} = -40mV$ .

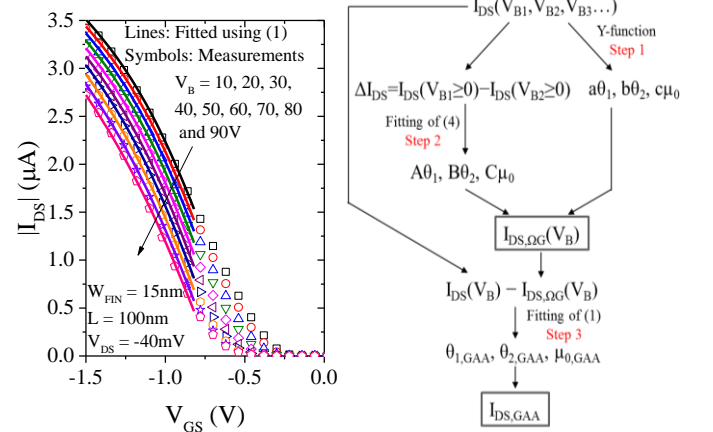


Fig. 5. (a) Step 3. Measurements and model results of  $I_{DS}$  vs.  $V_{GS}$  for NW with  $W_{FIN} = 15nm$ ,  $L = 100nm$  and  $V_{DS} = -40mV$ . (b) Schematic representation of the proposed method highlighting steps 1 to 3.

Step 3.– Once all parameters for the  $\Omega$ -NW are determined,  $I_{DS,\Omega G}$  can be calculated and, by fitting  $I_{DS}$  measurements to (1), it is possible to extract  $\mu_{0,GAA}$ ,  $\theta_{1,GAA}$  and  $\theta_{2,GAA}$ . This last step of the proposed methodology is presented in Fig. 5-a.

The schematics of the entire procedure is shown in Fig. 5-b. Fig. 6 indicates the obtained parameters for both  $\Omega$ - and GAA-NWs of the stacked structure. Similar  $\mu_0$  and  $(1 + \theta_1 V_{GT} + \theta_2 V_{GT}^2)$  behavior with  $V_B$  is found by comparing the stacked  $\Omega$ -NW and the non-stacked TG NW corroborating with the validity of the proposed method.

The proposed method has been applied in stacked NWs, varying  $T$  from 25°C up to 150°C. The  $\mu_{0,\Omega G}$  increases with  $V_B$  decrease, evidenced in Figs. 6 and 7, is in agreement with previous reported work in literature [7]. It is mainly explained by the inversion charge distribution in the NW channel modulated by  $V_B$ , and the position from Si/insulator interface. At  $V_B = 0V$ , Fig.7-b shows that both  $\Omega$ - and GAA-NWs present similar  $\mu_0$  slope varying  $T$ , -0.12 and -0.11cm<sup>2</sup>/V.s.°C,

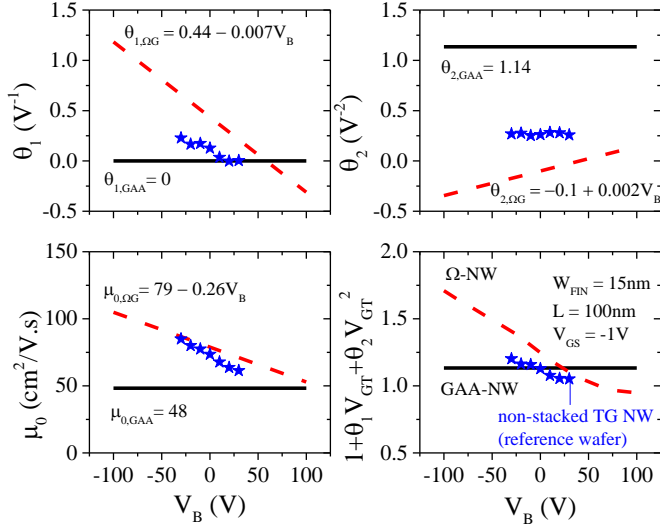


Fig. 6. Extracted parameters through the proposed methodology for NWs with  $W_{FIN} = 15nm$  and  $L = 100nm$ .

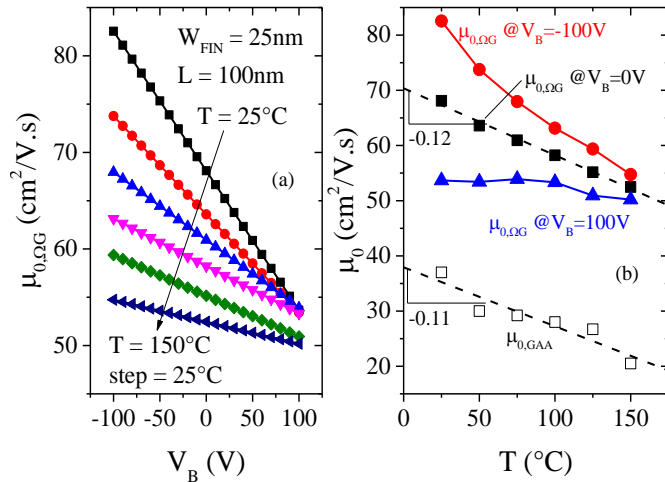


Fig. 7.  $\mu_{0,\Omega G}$  vs.  $V_B$ , varying  $T$  (a) and  $\mu_0$  for both top GAA and bottom  $\Omega$ -NWs vs.  $T$  (b), varying  $V_B$  for NW with  $W_{FIN} = 25nm$  and  $L = 100nm$ .

respectively. The linear mobility decrease with  $T$  increase is dominated by phonon scattering. However, Fig. 7 shows a strong increase of  $\mu_0$   $T$ -dependence by decreasing  $V_B$ , in agreement with reduced surface roughness contribution and higher phonon scattering contribution at negative  $V_B$ .

#### IV. CONCLUSIONS

The improved method for separating the contributions of each NW on stacked NW SOI MOSFETs by means of back bias variation has shown to be a powerful tool for electrical parameters extraction. The proposed method allows for accurate description of the measured trends in a wide range of  $V_B$  and temperature. The linear behavior between mobility parameters and  $V_B$ , which has also been evidenced in non-stacked TG NWs, must be taken into account in order to correctly describe the drain current of narrow NW SOI MOSFETs. Lower mobility values extracted to GAA-NWs are in agreement with results in literature, due to lower hole mobility of (100)/[110] surface conduction and stronger surface roughness degradation. The proposed method also revealed that the mobility dependence on  $T$  for  $\Omega$ -NW remarkably vary with  $V_B$  in the studied range.

#### ACKNOWLEDGMENT

This work was partially carried out thanks to the French Public Authorities from NANO 2017 program, CNPq and São Paulo Research Foundation (FAPESP) grants 2015/10491-7 and 2016/06301-0.

This work is also partially funded by the SUPERAID7 (grant N° 688101) project.

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