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TID Response of Various Field Programmable Gate Arrays and Memory Devices

J. M. Armani, J. L. Leray, *Fellow, IEEE,* R. Gaillard, *Senior Member, IEEE,* and V. Iluta

***Abstract*—The Total Ionizing Dose (TID) tolerance of some FPGAs and memory devices has been evaluated. Two FPGAs and five memories of various types and technologies have been irradiated. Results show that the total dose tolerance of the tested FPGAs is around 200 Gy. The SRAM is the most tolerant device with a failure dose level over 2.4 kGy. Two Flash memories were still well-functioning after 1 kGy.**

***Index Terms*—CMOS, Field Programmable Gate Array, Flash, MRAM, SRAM, Total Ionizing Dose**

I. Introduction

FIELD programmable gate arrays (FPGAs) are widely used in digital systems for industrial applications or consumer electronic equipment. In the nuclear industry, FPGAs are gaining increased attention worldwide for application in nuclear power plant I&C systems since old analog and microcontroller-based systems are becoming obsolete and need to be replaced. Nuclear Power Plant operators and equipment suppliers see many advantages of FPGA-based I&C systems as compared to microprocessor-based ones. Demonstrating the reliability and safety of software-based systems in the licensing process is indeed difficult and laborious. FPGAs can provides flexibility and capability similar to software but with lower complexity, simpler system architecture, and improved performance of hardware.

However, in the nuclear industry and particularly in power plants or irradiated fuel reprocessing facilities, there has been for years a conservative approach that has limited the use of such components for safety critical missions. Although radiation hardened FPGAs are available, they are much more expensive than Commercial off the Shelf (COTS) devices and their availability may be restricted. As a consequence, situations where an FPGA is effectively used in irradiating areas with potential exposure to high total dose levels are not so common. Nevertheless, there is also in this domain a growing interest in the use of intelligent devices in hazardous zones.

Many studies have already been made for assessing the total dose tolerance of commercial FPGAs and memory devices (particularly flash-based devices) for aerospace usages ([1][2] as an example). Most of these works involve low total dose levels, typically few kilograys. However, the robustness of electronic systems has to be several orders of magnitude higher for a use in nuclear environment. In this context, it is therefore interesting to test these kinds of component at higher dose levels.

In this work we have tested the Total Ionizing dose (TID) response of several FPGAs and memory devices from different vendors for evaluating their resistance. The purpose was to identify candidate components for the design of a hardened FPGA-based system intended for nuclear applications.

II. Objectives of this Work

We started recently the development of a FPGA-based denoising system for a hardened digital video camera. The camera itself has been designed during the past years and it is now produced industrially. It uses a CMOS VGA color sensor and is hardened up to a dose of 50 kGy. When exposed to gamma rays, this camera produces images that are affected by the "snow" noise like many others. This effect is generated by the interaction of energetic photons with the sensor's electronic circuitry. It is dose rate dependent and may affect the analysis of images. Real-time noise reduction techniques could therefore improve the image quality.

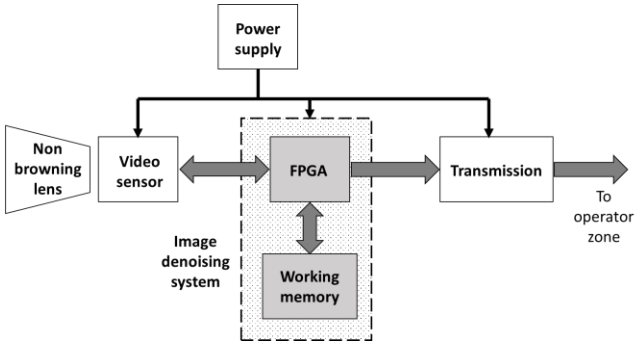

Fig. 1. Architecture of the hardened camera including the image denoising system.

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The denoising system will be added to the next version of the video camera. A radiation tolerant FPGA will ensure the real-time digital filtering of images. For a better integration, this system will be included in the camera, avoiding this way a two parts architecture and high bit rate transmission over a lengthy cable between the video sensor and the FPGA. Another possible application could be the serialization of the sensor's video stream in case of parallel outputs for reducing cable size (which can be a critical aspect in a nuclear plant).

Fig. 1 shows the proposed architecture including the noise suppression system. In this work, we firstly focus on the fundamental components: the FPGA and the working memory that stores the settings and the computing results. The existing transmission block will be modified later in order to adapt to the output of the chosen FPGA.

III. Previous studies

A review of previous papers concerning TID testing of FPGAs and memory devices was done in a view to help in selecting the components for the study.

We report in Table I some references of Flash-based and SRAM-based FPGAs that have already been tested [3]-[7]. In these papers SRAM-based FPGAs seem to be more robust than Flash-based ones.

TABLE I
Previous radiation tests of FPGAs

Vendor	Type	Reference	Feature Size	Dose* (kGy)
Microsemi	Flash	A3PE3000L	130 nm	1.25
Microsemi	Flash	A2F200-FG484	130 nm	0.79
Microsemi	Flash	M2S050	65 nm	0.70
Altera	SRAM	EP1C6Q240C8	130 nm	2.5
Xilinx	SRAM	XC6SLX45	45 nm	0.30

*: dose reached at the end of the test.

The number of papers that describe total dose testing of memory devices is significant. Table II presents part numbers of memories that were tested in some of these studies [8]-[13]. FeRAM and MRAM appear generally more resistant than Flash memories.

TABLE II
Previous radiation tests of memories

Vendor	Type	Reference	Size	Feature Size	Dose* (kGy)
-	SRAM[a]	-	-	130 nm	2-4[b]
Samsung	Flash	K9G8G08U0A	8 Gb	51 nm	6.0
Micron	Flash	MT29F32G08CBA	32 Gb	32 nm	1.0
Micron	Flash	MT29F32G08ABA	32 Gb	25 nm	0.70
Ramtron	FeRAM	FM20L08	1 Mb	-	0.35
Ramtron	FeRAM	FM25L04	4 kb	-	2.0
Everspin	MRAM	PR0A08BCYS35	1 Mb	130 nm	1.5
Freescale	MRAM	MR2A16A	4 Mb	90 nm	1.1

*: dose reached at the end of the test.

[a]: For the SRAM devices, [8] makes a comparison of different foundries without giving part numbers or manufacturers.

[b]: In this case, 'Dose' is the TID failure level that was observed.

IV. Test description

A. Selected components

In this experiment we have selected two models of FPGA and five models of memory. The devices were selected taking into account the noise suppression system specifications such as the FPGA working frequency and number of elements or the size of the working memory.

The first selected FPGA is Lattice ECP3 family part number LFE3-35EA-6FTN256C. This SRAM-based device was chosen to represent the current device family of the manufacturer. The ECP3 family is fabricated in a 1.2V, 65 nm process, and features densities up to 149k Look Up tables (LUTs) and up to 6.85 Mbit of RAM [14]. The component chosen for this test contains 33k LUTs, 1 Mbit of dedicated RAM, 2 phase-locked loops (PLLs), a quad 3.2Gbps SerDes and 32 Hard DSP. The device is packaged in a 256 pins ftBGA and has 133 I/O pins available.

The second FPGA is the A3PE1500-PQG208 that belongs to the Microsemi ProASIC3E Flash family. This family is based on a 1.5V 130 nm CMOS process. It has up to 3M system gates and 504 kbit of SRAM [15]. The A3PE1500 device contains 38400 VersaTiles, 270 kbit of RAM, 2 PLLs and has 147 I/O pins available for the user. The part is in a PQ208 package.

Regarding the memories, we have selected one SRAM, one MRAM and three Flash devices. The 23LC1024-I/SN is a 1 Mbit CMOS SRAM fabricated by Microchip. The MR25H40CDC is a 4 Mbit MRAM manufactured by Everspin in a 180 nm CMOS process. There are two 16 Mbit Flash memories fabricated with a 110 nm CMOS technology. The first one is the EPCS16SI8N from Altera and the second is the M25PX16-VMN6P from Micron (former Numonyx). The third Flash memory is the N25Q128A13ESE40E from Micron. It has 128 Mbit capacity and is manufactured with a 65 nm CMOS process.

B. Irradiation facilities

Irradiation of the components was performed at the CEA Saclay research center (France) where several facilities are available. Two irradiation facilities were used for the experiment. The first irradiator, IRMA, has four high activity sealed Cobalt 60 sources (total activity of 270 TBq). This 24 m^3 irradiation cell is used to study the effects of gamma rays on materials. In this facility, the dose rate ranges from 1 Gy/h to 1 kGy/h. The second one, PAGURE, is a gamma irradiator equipped with six Cobalt 60 sources (total activity of 740 TBq) placed in a 25 m^2 room. It allows radiation testing of equipment in a dose range from 10 Gy/h to 25 kGy/h. In these irradiators, the tested devices are placed in the irradiation chamber before the experiment at positions determined by a preliminary dose rate measurement. In both facilities, the ambient temperature is not controlled. As a result, temperature may fluctuate by several degrees between night and day.

C. Experimental conditions

The FPGAs were irradiated in the PAGURE facility with a dose rate of 25 Gy/h at room temperature in December 2014. To measure the TID effects on the devices, a specific design was used during the irradiation. This design implements a chain of AND-gates to measure the propagation delay degradation and a chain of D-type flip-flops configured as a ripple clock divider to evaluate the degradation of the clock propagation delay in the flip-flops. Both chains have a length of 800 stages in the two FPGAs. During the experiment, a function generator provided the low frequency signal injected at the inputs of the two chains. Propagation delays were measured with a digital oscilloscope. Moreover, the stability of a 31.25 kHz PLL and the supply currents of the FPGAs (core and I/O) were monitored during the test. The programmability of the devices through the JTAG interface was also periodically checked.

Memory devices were tested in the IRMA facility with a dose rate of 60 Gy/h at room temperature in September 2014. The test methodology of the memories was defined as follow:

a. Erase, write, and read to validate programmed data.
b. Irradiate DUTs with static bias.
c. Stop irradiation.
c. Read data to ensure data retention.
d. Write complement of read data in the DUT.
e. Read data to ensure write capability.
f. Repeat steps a to e until complete failure of the device.

During the experiment, the memories were tested in a static mode to evaluate their data retention and writing capabilities. Several irradiation steps have been used to measure the devices. Eight pre-defined patterns (00, FF, AA, 55, CC, 33, 66 and 99) were stored manually in the devices before each irradiation increment. In each memory, these patterns were stored at four different places: bottom, quarter, half and three quarters of the memory range. The state of the memories was evaluated at each irradiation stop.

V. Results

A. Results of the FPGA test

Due to a failure of the test bench, we have unfortunately no data concerning the propagation delay of the AND-gates chain for the Lattice and Microsemi FPGAs. Fortunately the other records are usable.

Fig. 2 shows the evolution of the clock propagation delay in the flip-flop chain for Microsemi and Lattice FPGAs. For the A3PE1500, the delay starts to rise slowly after a cumulated dose of 40 Gy (the growth is limited to +17% at 370 Gy). Then the delay increases sharply and saturates at 2.5 µs (+210%) when a complete failure of the FPGA occurs after a cumulated dose of 500 Gy. The LFE3-35EA exhibits a steady rise of the flip-flop delay before its failure. We note an increase of +87% (from 380 to 710 ns) at 440 Gy just before the total failure of the FPGA.

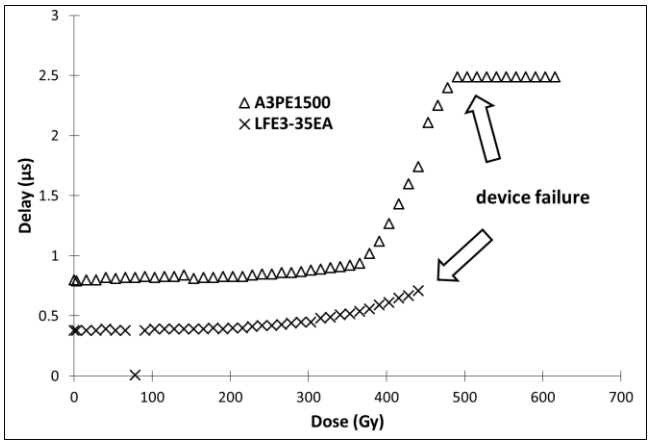

Fig. 2. Evolution of the flip-flop chain propagation delay for the Microsemi A3PE1500 and Lattice LFE3-35EA FPGAs during irradiation.

The evolution of the power supply currents for the Lattice FPGA confirms the degradation observed with the flip-flop chain delay. On Fig. 3 we can see the evolution of the currents plotted as a function of the total dose.

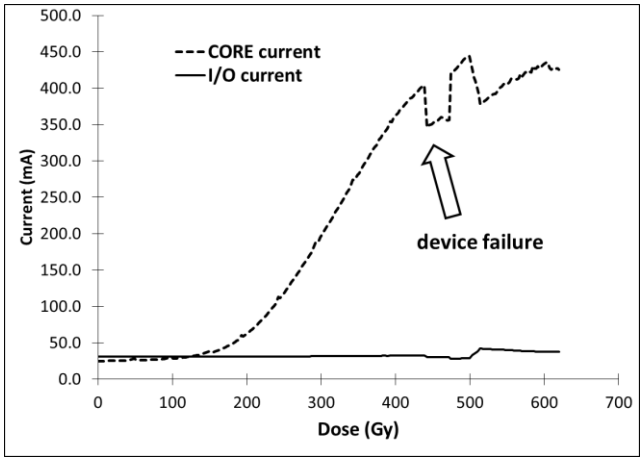

Fig. 3. Behavior of Core and I/O supply currents for the Lattice LFE3-35EA FPGA during the experiment.

The core supply current of the LFE3-35EA begins to rise after 50 Gy. Starting from 150 Gy, the increase accelerates until the core supply current reaches 400 mA (+1190%) at 430 Gy. At that dose level the FPGA is hardly damaged and stops working suddenly. After the failure, the core current behavior becomes somewhat inconsistent. On the other hand, the I/O power supply current of the Lattice FPGA remains stable until the breakdown.

We can see on Fig. 4 the plot of power supply currents of the Microsemi A3PE1500 as function of the cumulated dose. After the beginning of the test, the core current rises slowly until 130 Gy. It then decreases and at 180 Gy a step appears unexpectedly. At that moment, the FPGA is already damaged but it is still functioning. Then the core current of the FPGA

behave erratically and starts increasing again after the device breakdown at 450 Gy. On the other hand, the I/O supply current of the A3PE1500 remains stable during all the experiment, even after the failure.

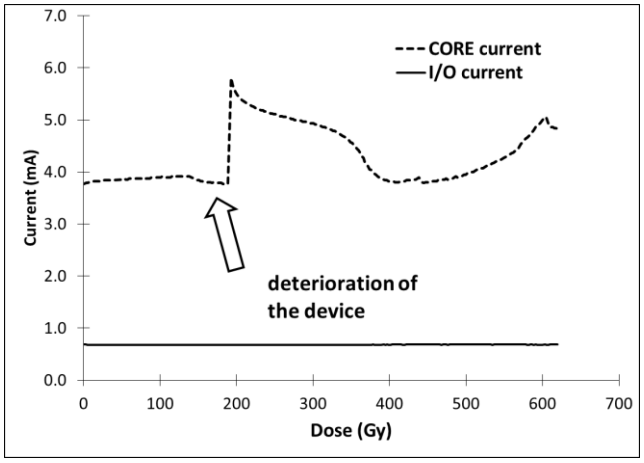

Fig. 4. Core and I/O supply currents as a function of the total dose for the Microsemi A3PE1500 FPGA.

B. Results of the memory test

The memory devices showed similar symptoms after their failure: a huge increase of the power supply current (more than ten times the value of a fresh device) and incorrect read data (all bytes equal to 00). We can see on Fig. 5 the failure dose level for the different devices. M25PX16 Flash memory broke down early before 1 kGy. The other two Flash devices were still functional at 1050 Gy, but failed before 2 kGy as the MRAM component. The SRAM was still functional at 2400 Gy but failed before 6600 Gy. It is the most resistant of the tested devices.

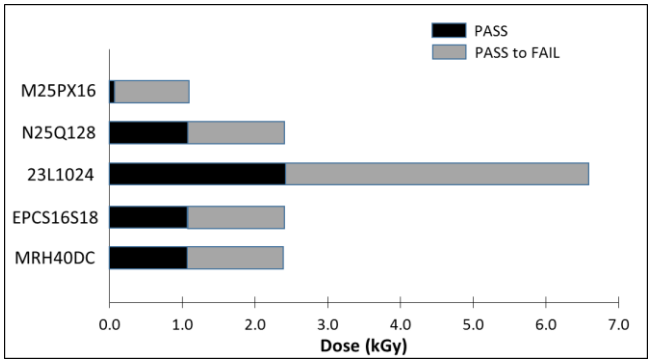

Fig. 5. TID response of the memory devices tested in this work.

The total dose failure level that was found for Flash devices is consistent with the usually observed limit (300 to 700 Gy) for this kind of memory.

VI. Conclusion

The work presented in this paper is a preliminary study. The objective was to assess the TID response of several FPGAs and memory devices from different vendors in a view to identify candidate components for the design of a hardened FPGA-based system. Two FPGAs and five memories of various types and technologies have been irradiated.

Results show that the total dose tolerance of the tested FPGAs is around 200 Gy. The SRAM memory is the most tolerant device with a failure dose level over 2.4 kGy. Two Flash memories were still well-functioning after 1 kGy.

These levels are not sufficient for our objectives. For this reason, a new irradiation campaign with other components should be planned at the end of the year.

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